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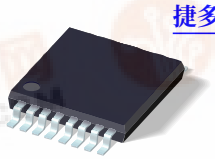


TPS40060
TPS40061
SLUS543D–DECEMBER 2002–REVISED SEPTEMBER 2004

WIDE-INPUT SYNCHRONOUS BUCK CONTROLLER

FEATURES

- Operating Input Voltage 10 V to 55 V
- Input Voltage Feed-Forward Compensation
- < 1% Internal 0.7-V Reference
- Programmable Fixed-Frequency, Up to 1-MHz Voltage Mode Controller
- Internal Gate Drive Outputs for High-Side P-Channel and Synchronous N-Channel MOSFETs
- 16-Pin PowerPAD™ Package (θ_{JC} = 2°C/W)
- Thermal Shutdown
- Externally Synchronizable
- Programmable High-Side Sense Short Circuit Protection
- Programmable Closed-Loop Soft-Start
- TPS40060 Source Only/TPS40061 Source/Sink

DESCRIPTION

The TPS40060 and TPS40061 are high-voltage, wide input (10 V to 55 V) synchronous, step-down converters.

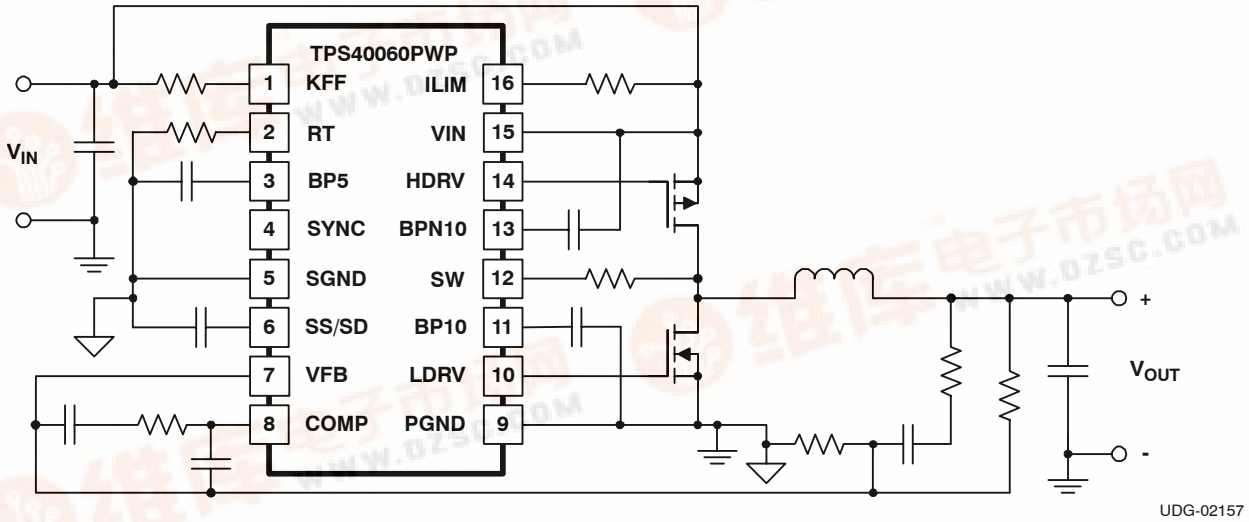
This family of devices offers design flexibility with a variety of user programmable functions, including; soft-start, UVLO, operating frequency, voltage feed-forward, high-side current limit, and loop compensation. These devices are also synchronizable to an external supply.

The TPS40060 and TPS40061 incorporate MOSFET gate drivers for external P-channel high-side and N-channel synchronous rectifier (SR) MOSFETs. Gate drive logic incorporates anti-cross conduction circuitry to prevent simultaneous high-side and synchronous rectifier conduction.

APPLICATIONS

- Networking Equipment
- Telecom Equipment
- Base Stations
- Servers

SIMPLIFIED APPLICATION DIAGRAM



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	LOAD CURRENT	PACKAGE(1)	PART NUMBER
–40°C to 85°C	SOURCE(2)	Plastic HTSSOP (PWP)	TPS40060PWP
	SOURCE/SIN(2)	Plastic HTSSOP (PWP)	TPS40061PWP

(1) The PWP package is alsoavailable taped and reeled. Add an R suffix to the device type (i.e.,TPS40060PWPR). See the application section of the data sheet for PowerPADdrawing and layout information.
(2) See ApplicationInformation section.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

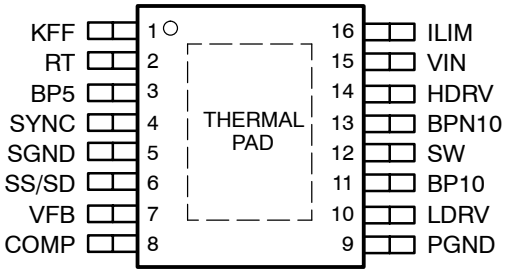
			TPS40060 TPS40061
V_{IN}	Input voltage range	VIN	60 V
		VFB, SS/SD, SYNC	–0.3 V to 6 V
		SW	–0.3 V to 60 V or VIN+5 V (whichever is less)
		SW. transient < 50 ns	–2.5 V
V_{OUT}	Output voltage range	COMP, RT, KFF, SS	–0.3 V to 6 V
I_{IN}	Input current	KFF	5 mA
I_{OUT}	Output current	RT	200 μA
T_J	Operating junction temperature range		–40°C to 125°C
T_{stg}	Storage temperature		–55°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond thoselisted under "absolute maximum ratings" may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the deviceat these or any other conditions beyond those indicated under "recommendedoperating conditions" is not implied. Exposure to absolute-maximum-ratedconditions for extended periods may affect devicereliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	10		55	V
T_A	Operating free-air temperature	–40		85	°C

PWP PACKAGE (1)(2)
(TOP VIEW)



(1) For more information on the PWP package, refer to TI Technical Brief (SLMA002).
(2) PowerPAD™ heat slug must be connected to SGND (Pin 5), or electrically isolated from all other pins.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 165 kΩ, I_{KFF} = 113 μA, f_{SW} = 300 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range, VIN		10		55	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching		1.5	2.5	mA
5-V REFERENCE						
V_{BP5}	Input voltage		4.5	5.0	5.5	V
OSCILLATOR/RAMP GENERATOR(1)						
f_{OSC}	Frequency		270	300	330	kHz
V_{RAMP}	PWM ramp voltage(2)			2		V
V_{IH}	High-level input voltage, SYNC		2			
V_{IL}	Low-level input voltage, SYNC				0.8	
I_{SYNC}	Input current, SYNC			5	10	μA
	Pulse width, SYNC	Pulse amplitude = 5 V	50			ns
V_{RT}	RT voltage		2.32	2.50	2.68	V
	Maximum duty cycle	V_{FB} = 0 V, 100 kHz ≤ f_{SW}≤ 1 MHz	85%		98%	
	Minumum duty cycle	V_{FB} ≥ 0.75 V			0%	
V_{KFF}	Feed-forward voltage		3.35	3.50	3.65	V
I_{KFF}	Feed-forward current operating range(3)		20		1100	μA
SS/SD (SOFT START)						
I_{SS}	Soft-start source current		1.8	2.3	2.9	μA
V_{SS}	Soft-start clamp voltage		3.1	3.7	4.0	V
t_{DSCH}	Discharge time	C_{SS} = 220 pF	1.8	2.2	2.8	μs
t_{SS}	Soft-start time	C_{SS} = 220 pF, 0 V ≤ V_{SS} ≤ 1.6 V	120	155	190	
SS/SD (SHUTDOWN)						
V_{SD}	Shutdown threshold voltage		90	120	145	mV
V_{EN}	Device action threshold voltage		160	210	260	mV
10-V REFERENCE						
V_{BP10}	Input voltage		9.0	9.7	10.7	V
ERROR AMPLIFIER						
V_{FB}	Feedback regulation voltage	T_A = 25°C	0.698	0.700	0.704	V
		0°C ≤ T_A ≤ 85°C	0.690	0.700	0.707	
			0.690	0.700	0.715	
G_{BW}	Gain bandwidth		3	5		MHz
A_{VOL}	Open loop gain		60	80		dB
I_{OH}	High-level output source current	V_{COMP} = 2.0 V, V_{FB} = 0 V	1.5	4.0		mA
I_{OL}	Low-level output sink current	V_{COMP} = 2.0 V, V_{FB} = 1 V	2.5	4.0		
I_{BIAS}	Input bias current	V_{FB} = 0.7 V		100	300	nA
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA, V_{FB} = 0 V	3.25	3.45	3.60	V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 mA, V_{FB} = 1 V	0.050	0.215	0.350	

(1) KFF current(I_{KFF}) increases with SYNC frequency(f_{SYNC}) and decreases with maximum dutycycle (D_{MAX}).
(2) Ensured by design. Notproduction tested.
(3) Ensured by design. Notproduction tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 165 kΩ, I_{KFF} = 113 μA, f_{SW} = 300 kHz, all parameters at zero power dissipation (unless otherwise noted)

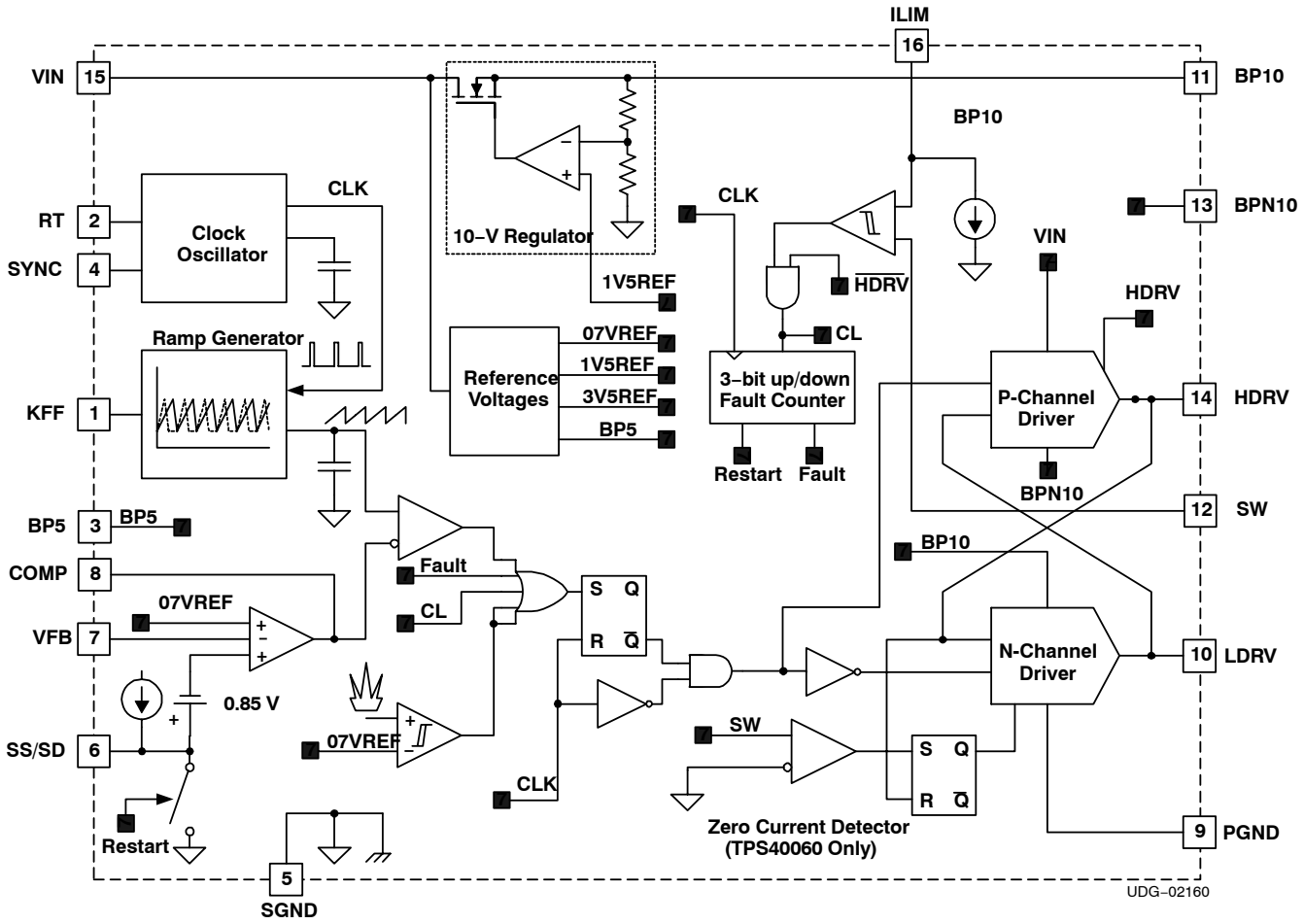
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{SINK}	Current limit sink current		8.3	10.0	11.5	μA
t_{DELAY}	Propagation delay to output	V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM}– 0.5 V)		330	500	ns
		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM}– 2 V)		275	375	
t_{ON}	Switch leading-edge blanking pulse time (4)		100			
t_{OFF}	Off time during a fault			7		cycles
V_{OS}	Overcurrent comparator offset voltage		-200	-60	50	mV
OUTPUT DRIVER						
t_{HFALL}	High-side driver fall time (4)	C_{HDRV} = 2200 pF, (V_{IN}– V_{BPN10})		48	96	ns
t_{HRISE}	High-side driver rise time (4)	C_{HDRV} = 2200 pF, (V_{IN}– V_{BPN10})		36	72	
t_{LFALL}	Low-side driver fall time (4)	C_{LDRV} = 2200 pF, BP10		24	48	
t_{LRISE}	Low-side driver rise time (4)	C_{LDRV} = 2200 pF, BP10		48	96	
V_{OH}	High-level ouput voltage, HDRV	I_{HDRV} = 0.1 A , (V_{IN}– V_{HDRV})		1.0	1.4	V
V_{OL}	Low-level ouput voltage, HDRV	I_{HDRV} = 0.1 A , (V_{HDRV}– V_{BPN10})			0.75	
V_{OH}	High-level ouput voltage, LDRV	I_{LDRV} = 0.1 A, (V_{BP10}– V_{LDRV})		1.0	1.5	
V_{OL}	Low-level ouput voltage, LDRV	I_{LDRV} = 0.1 A			0.5	
	Minimum controllable pulse width			100	150	ns
BPN10 REGULATOR						
V_{BPN10}	Output voltage	Outputs off	–7.5	–8.5	–9.5	V
RECTIFIER ZERO CURRENT COMPARATOR (TPS40060 ONLY)						
V_{SW}	Switch voltage	LDRV output OFF	–6	0	6	mV
SW NODE						
I_{LEAK}	Leakage current (4)				1	μA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature (4)			165		°C
	Hysteresis (4)			25		
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold voltage, BP10	R_{KFF} = 10 kΩ	6.25	6.5	7.5	V
	Undervoltage lockout hysteresis			0.4		
V_{KFF}	KFF programmable threshold voltage	R_{KFF} = 82.5 kΩ	9	10	11	

(4) Ensured by design. Notproduction tested.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BP5	3	O	5-V reference. This pin should be bypassed to ground with a 0.1-μF ceramic capacitor. This pin may be used with an external DC load of 1 mA or less.
BP10	11	O	10-V reference used for gate drive of the N-channel synchronous rectifier. This pin should be bypassed by a 1-μF ceramic capacitor. This pin may be used with an external DC load of 1 mA or less.
BPN10	13	O	Negative 8-V reference with respect to VIN. This voltage is used to provide gate drive for the high side P-channel MOSFET. This pin should be bypassed to VIN with a 0.1-μF capacitor
COMP	8	I	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the VFB pin to compensate the overall loop. The comp pin is internally clamped above the peak of the ramp to improve large signal transient response.
HDRV	14	O	Floating gate drive for the high-side P-channel MOSFET. This pin switches from VIN (MOSFET off) to BPN10 (MOSFET on).
ILIM	16	I	Current limit pin, used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VIN. The voltage on this pin is compared to the voltage drop (VIN -SW) across the high side MOSFET during conduction.
KFF	1	I	A resistor is connected from this pin to VIN to program the amount of voltage feed-forward. The current fed into this pin is internally divided and used to control the slope of the PWM ramp.
LDRV	10	I	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
PGND	9		Power ground reference for the device. There should be a low-impedance connection from this point to the source of the power MOSFET.
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator ramp charging current and switching frequency.
SGND	5		Signal ground reference for the device.
SS/SD	6	I	Soft-start programming pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 2.3 μA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. The output voltage begins to rise when $V_{SS/SD}$ is approximately 0.85 V. The output continues to rise and reaches regulation when $V_{SS/SD}$ is approximately 1.55 V. The controller is considered shut down when $V_{SS/SD}$ is 125 mV or less. All internal circuitry is inactive. The internal circuitry is enabled when $V_{SS/SD}$ is 210 mV or greater. When $V_{SS/SD}$ is less than approximately 0.85 V, the outputs cease switching and the output voltage (V_{OUT}) decays while the internal circuitry remains active.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing. This pin is used for zero current sensing in the TPS40060.
SYNC	4	I	Synchronization input for the device. This pin can be used to synchronize the oscillator to an external master frequency.
VFB	7	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage, 0.7 V.
VIN	15	I	Supply voltage for the device.

SIMPLIFIED BLOCK DIAGRAM



APPLICATION INFORMATION

The TPS40060/61 family of parts allows the user to optimize the PWM controller to the specific application.

The TPS40061 is the controller of choice for synchronous buck designs which will include most applications. It has two quadrant operation and will source or sink output current. This provides the best transient response.

The TPS40060 operates in one quadrant and sources output current only, allowing for paralleling of converters and ensures that one converter does not sink current from another converter. This controller also emulates a standard buck converter at light loads where the inductor current goes discontinuous. At continuous output inductor currents the controller operates as a synchronous buck converter to optimize efficiency.

SW NODE RESISTOR

The SW node of the converter will be negative during the *dead time* when both the upper and lower MOSFETs are off. The magnitude of this negative voltage is dependent on the lower MOSFET body diode and the output current which flows during this dead time. This negative voltage could affect the operation of the controller, especially at low input voltages.

Therefore, a 10-Ω resistor must be placed between the lower MOSFET drain and pin 12 (SW) of the controller as shown in Figure 13 as R_{SW}.

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS40060 and TPS40061 have independent clock oscillator and ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. The switching frequency, f_{SW} in kHz, of the clock oscillator is set by a single resistor (R_T) to ground. The clock frequency is related to R_T, in kΩ by Equation 1 and the relationship is charted in Figure 2.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23 \right) k\Omega \tag{1}$$

PROGRAMMING THE RAMP GENERATOR CIRCUIT

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations since the PWM does not have to wait for loop delays before changing the duty cycle. (See Figure 1).

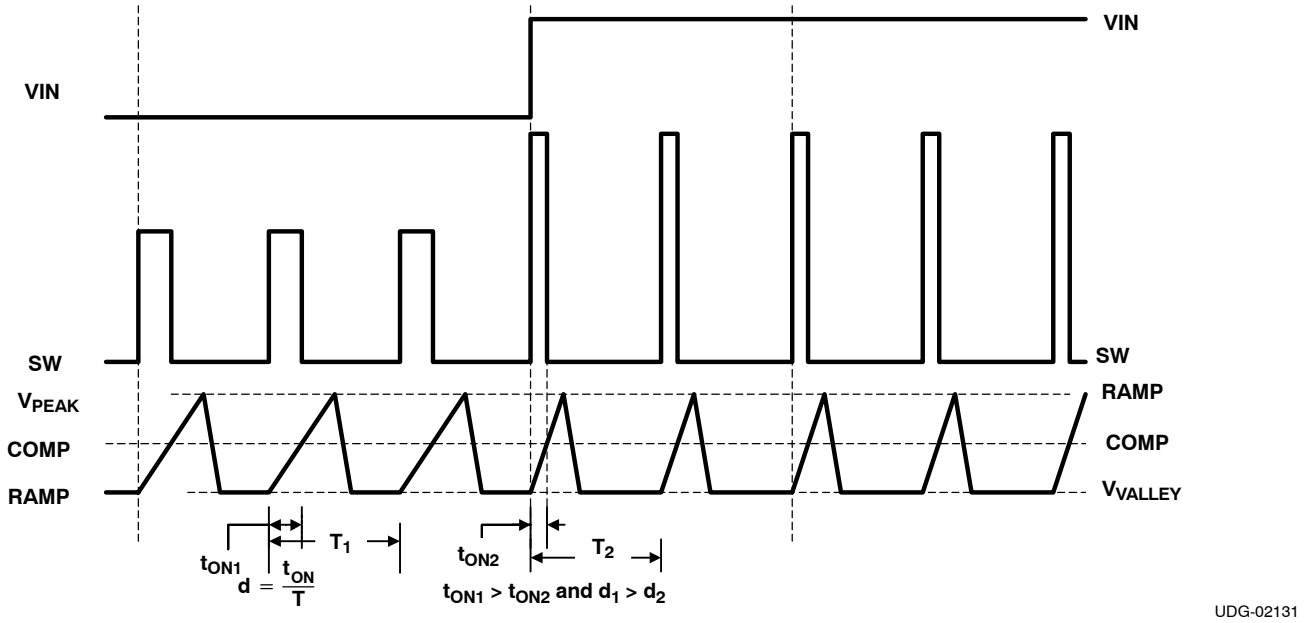


Figure 1. Voltage Feed-Forward Effect on PWM Duty Cycle

APPLICATION INFORMATION (continued)

The PWM ramp must be faster than the master clock frequency or the PWM is prevented from starting. The PWM ramp time is programmed via a single resistor (R_{KFF}) pulled up to V_{IN}. R_{KFF} is related to R_T, and the minimum input voltage, $V_{IN(min)}$ through the following:

$$R_{KFF} = \left(V_{IN\,(min)} - 3.5\right) \times \left(65.27 \times R_T + 1502\right)\ (\Omega) \tag{2}$$

where:

- V_{IN} is the desired start-up (UVLO) input voltage
- R_T is the timing resistor in kΩ

See the section on UVLO operation for further description.

The curve showing the feedforward impedance required for a given switching frequency, f_{SW}, at various input voltages is shown in Figure 3.

For low input voltage and high duty cycle applications, the voltage feed-forward may limit the duty cycle prematurely. This does not occur for most applications. The voltage control loop controls the duty cycle and regulates the output voltages. For more information on large duty cycle operation, refer to Application Note (SLUA310).

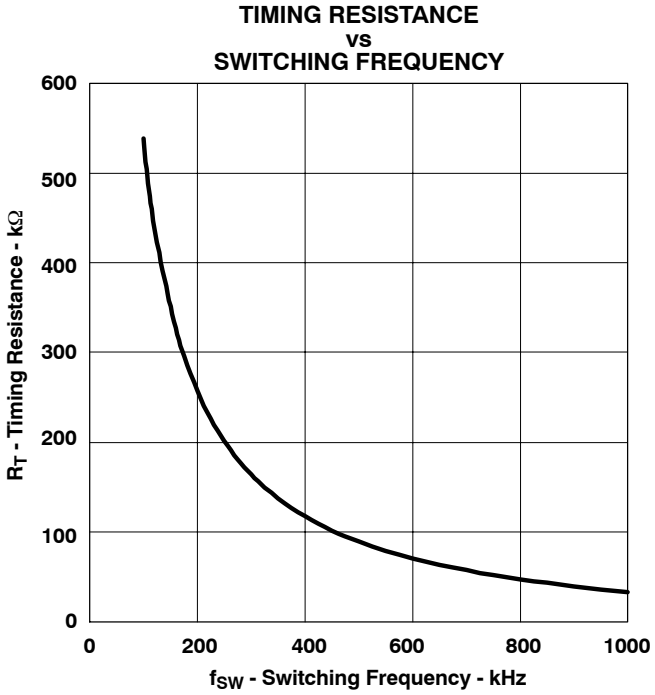


Figure 2.

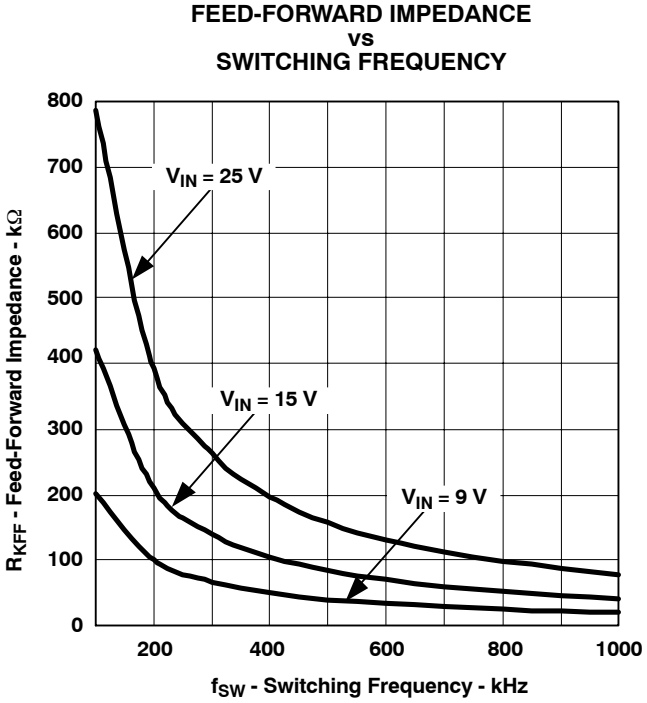


Figure 3.

UVLO OPERATION

The TPS40060 and TPS40061 use both fixed and variable (user programmable) UVLO protection. The fixed UVLO monitors the BP10 and BP5 bypass voltages. The UVLO circuit holds the soft-start low until the BP5 and BP10 voltage rails have exceeded their thresholds and the input voltage has exceed the user programmable undervoltage threshold.

The TPS40060 and TPS40061 use the feed-forward pin, KFF, as a user programmable low-line UVLO detection. This variable low-line UVLO threshold compares the PWM ramp duration to the oscillator clock period. An undervoltage condition existis if the device receives a clock pulse before the ramp has reached 90% of its full amplitude. The ramp duration is a function of the ramp slope, which is directly related to the current into the KFF pin. The KFF current is a function of the input voltage and the resistance from KFF to the input voltage. The KFF resistor can be referenced to the oscillator frequency as descibed in Equation 3:

APPLICATION INFORMATION (continued)

$$R_{KFF} = \left(V_{IN\ (min)} - 3.5\right) \times \left(65.27 \times R_T + 1502\right) \quad (\Omega) \tag{3}$$

where:

- V_{IN} is the desired start-up (UVLO) input voltage
- R_T is the timing resistor in kΩ

The variable UVLO function utilizes a 3-bit full adder to prevent spurious shut-downs or turn-ons due to spikes or fast line transients. When the adder reaches a total of seven counts in which the ramp duration is shorter the clock cycle a powergood signal is asserted, a soft-start initiated, and the upper and lower MOSFETs are turned off.

Once the soft-start is initiated, the UVLO cicruit must see a total count of seven cycles in which the ramp duration is longer than the clock cycle before an undervoltage condition is declared (See Figure 4).

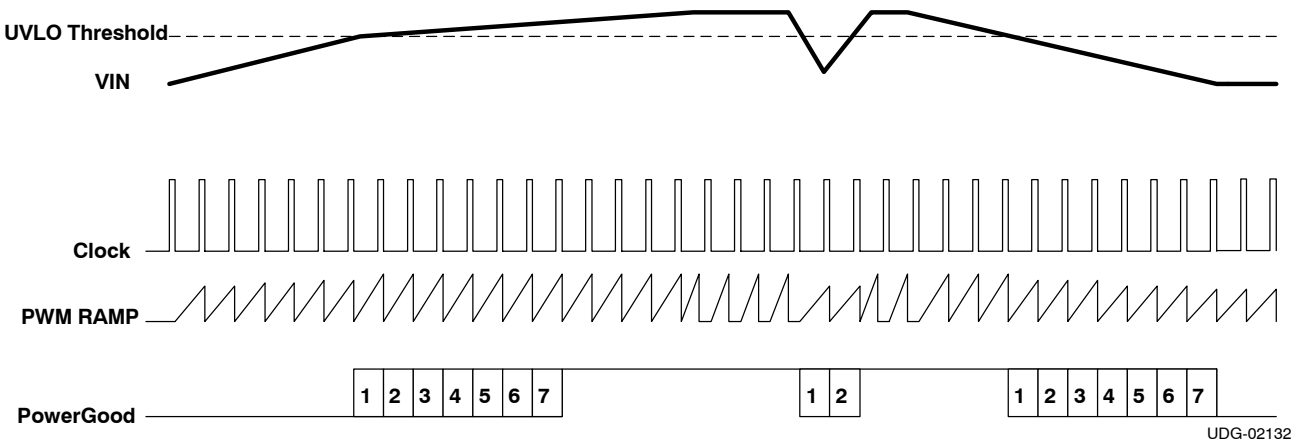


Figure 4. Undervoltage Lockout Operation

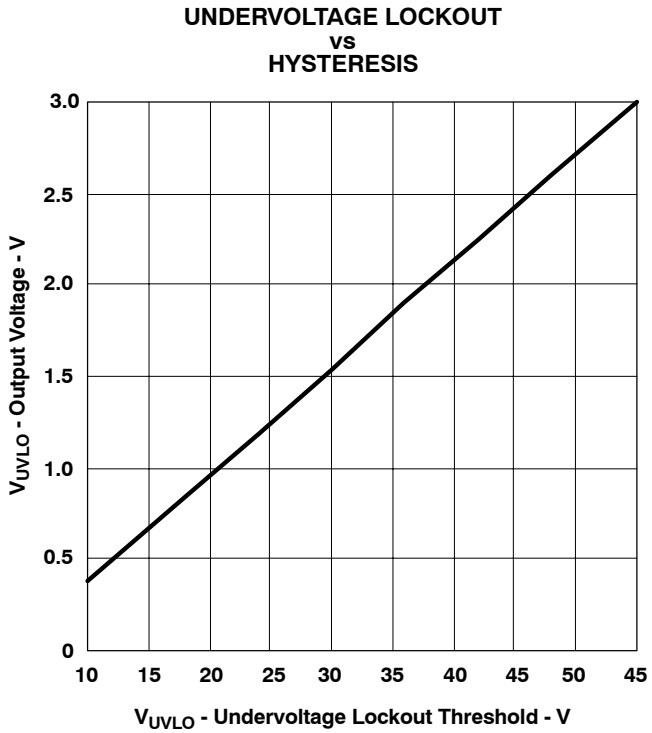


Figure 5.

APPLICATION INFORMATION (continued)

The impedance of the input voltage can cause the input voltage, at the TPS4006x, to sag when the converter starts to operate and draw current from the input source. Therefore, there is voltage hysteresis that prevents nuisance shutdowns at the UVLO point.

With RT chosen to select the operating frequency and RKFF chosen to select the start-up voltage, the amount of hysteresis voltage is shown in Figure 5.

PROGRAMMING SOFT START

TPS4006x uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by charging an external capacitor (C_{SS}) via an internally generated current source. The voltage on C_{SS} minus 0.85 V, is fed into a separate non-inverting input to the error amplifier (in addition to FB and 0.7-V V_{REF}). The loop is closed on the lower of the (C_{SS}– 0.85 V) voltage or the internal reference voltage (0.7-V V_{REF}). Once the (C_{SS}– 0.85 V) voltage rises above the internal reference voltage, regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage the soft-start time should be greater than the L-C_O time constant as described in Equation 4.

$$t_{START} \geq 2\pi \times \sqrt{L \times C_O} \quad \text{(seconds)} \tag{4}$$

There is a direct correlation between t_{START} and the input current required during start-up. The faster t_{START}, the higher the input current required during start-up. This relationship is describe in more detail in the section titled, *Programming the Current Limit* which follows. The soft-start capacitance, C_{SS}, is described in Equation 5.

For applications in which the V_{IN} supply ramps up slowly, (typically between 50 ms and 100 ms) it may be necessary to increase the soft-start time to between approximately 2 ms and 5 ms to prevent nuisance UVLO tripping. The soft-start time should be longer than the time that the V_{IN}supply transitions between 6 V and 7 V.

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times t_{START} \quad \text{(Farads)} \tag{5}$$

APPLICATION INFORMATION (continued)

PROGRAMMING CURRENT LIMIT

This device uses a two-tier approach for overcurrent protection. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when the gate is driven low. The MOSFET voltage is compared to the voltage dropped across a resistor connected from VIN pin to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

The second tier consists of a fault counter. The fault counter is incremented on an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7) a restart is issued and seven soft-start cycles are initiated. Both the upper and lower MOSFETs are turned off during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled. If the fault has been removed the output starts up normally. If the output is still present the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. See Figure 6 for typical overcurrent protection waveforms.

The minimum current limit setpoint (I_{LIM}) depends on t_{START}, C_O, V_O, and the load current at turn-on (I_L).

$$I_{LIM} = \left[\frac{\left(C_O \times V_O\right)}{t_{SS}}\right] + I_L \quad (A) \tag{6}$$

The current limit programming resistor (R_{ILIM}) is calculated using Equation 7. Care must be taken in choosing the values used fro V_{OS} and I_{SINK} in the equation. In order to ensure the output current at the overcurrent level, the minimum value of I_{SINK} and the maximum value of V_{OS} must be used.

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)[max]}}{I_{SINK}} + \frac{V_{OS}}{I_{SINK}} \quad (\Omega) \tag{7}$$

where:

- I_{SINK} is the current into the ILIM pin and is nominally 8.3 μA, minimum
- I_{OC} is the overcurrent setpoint which is the DC output current plus one-half of the peak inductor current
- V_{OS} is the overcurrent comparator offset and is 50 mV maximum

BP5, BPN10 AND BPN10 INTERNAL VOLTAGE REGULATOR

Start-up characteristics of the BP5, BP10 and BPN10 regulators are shown in Figure 6. Slight variations in the BP5 occurs dependent upon the switching frequency. Variation in the BPN10 and BP10 regulation characteristics is also based on the load presented by switching the external MOSFETs.

APPLICATION INFORMATION (continued)

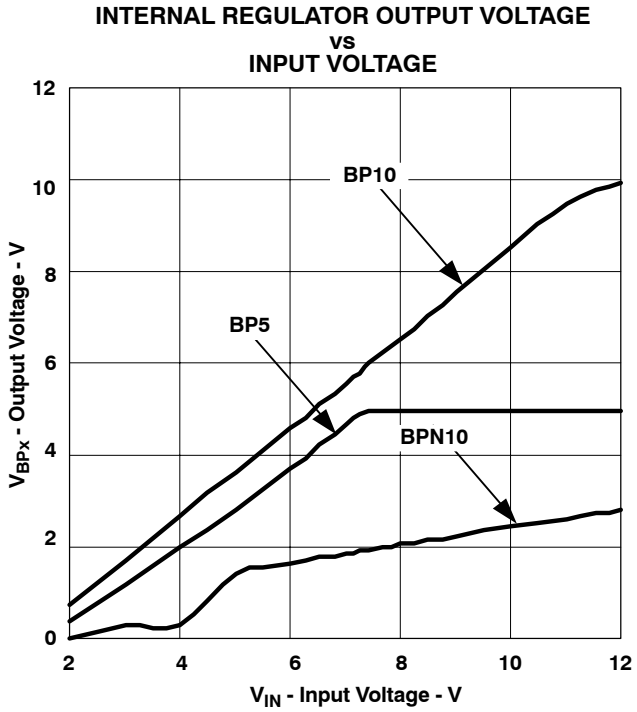


Figure 6.

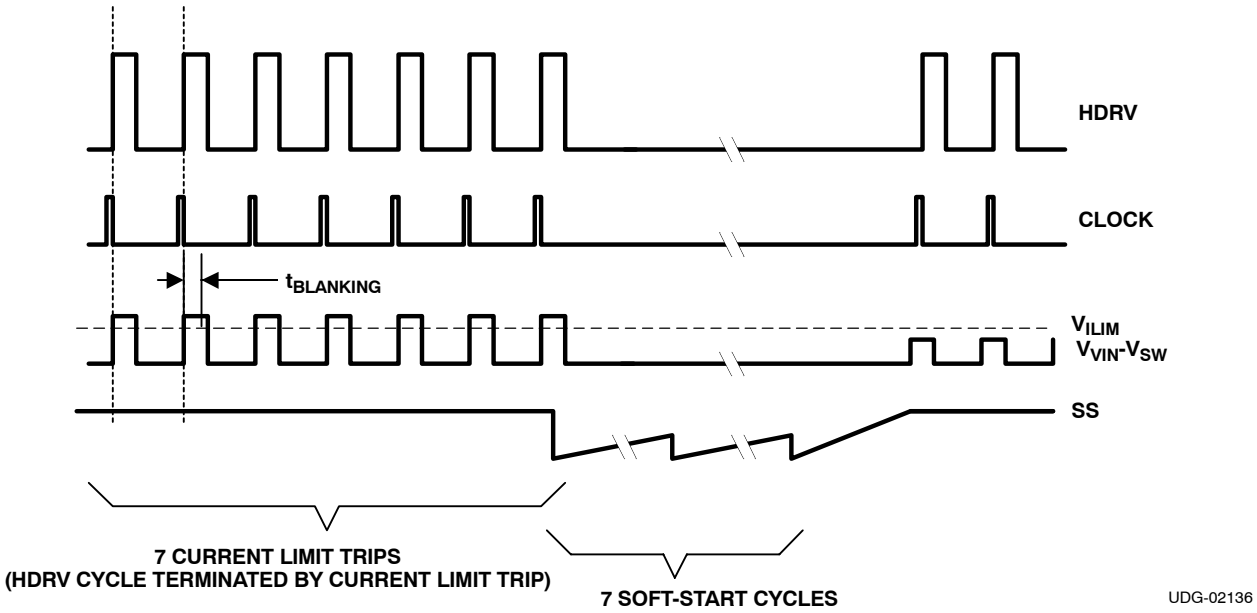


Figure 7. Typical Current Limit Protection Waveforms

CALCULATING THE BPN10 AN BP10V BYPASS CAPACITOR

The BPN10 capacitance provides a local, low impedance source for the high-side driver. The BPN10 capacitor should be a good quality, high-frequency capacitor. The size of the bypass capacitor depends on the total gate charge of the MOSFET and the amount of droop allowed on the bypass capacitor. The BPN10 capacitance is described in Equation 8.

APPLICATION INFORMATION (continued)

$$C_{BPN10} = \frac{Q_g}{\Delta V} \quad (F) \tag{8}$$

The 10-V reference pin, BP10V needs to provide energy for the synchronous MOSFET gate drive via the BP10V capacitor. Neglecting any efficiency penalty, the BP10V capacitance is described in Equation 9.

$$C_{BP10V} = \frac{Q_{gSR}}{\Delta V} \quad (F) \tag{9}$$

SYNCHRONIZING TO AN EXTERNAL SUPPLY

The TPS4006x can be synchronized to an external clock through the SYNC pin. The SW node rises on the falling edge of the SYNC signal. The synchronization frequency should be in the range of 20% to 30% higher than its programmed free-run frequency. The clock frequency at the SYNC pin replaces the master clock generated by the oscillator circuit. Pulling the SYNC pin low programs the TPS4006x to freely run at the frequency programmed by R_T.

Internally, the SYNC pin has a pull-down current between 5 μA and 10 μA. In order to synchronize the device to an external clock signal, the SYNC pin has to be overdriven from the external clock circuit. Normal logic gates or an external MOSFET with a pull-up resistor of 10 kΩ is adequate.

Internally there is a delay of between approximately 50 ns and 100 ns from the time the SYNC pin is pulled low and the HDRV signal goes high to turn on the upper MOSFET. Additionally, there is some delay as the MOSFET gate charges to turn on the upper MOSFET, typically between 20 ns and 50 ns.

The higher synchronization must be factored in when programming the PWM ramp generator circuit. If the PWM ramp is interrupted by the SYNC pulse, a UVLO condition is declared and the PWM becomes disabled. Typically this is of concern under low-line conditions only. In any case, R_{KFF} needs to be adjusted for the higher switching frequency. In order to specify the correct value for R_{KFF} at the synchronizing frequency, calculate a 'dummy' value for RT that would cause the oscillator to run at the synchronizing frequency. Do not use this value of RT in the design.

$$R_{T(dummy)} = \left(\frac{1}{f_{SYNC} \times 17.82 \times 10^{-6}} - 23\right) k\Omega \tag{10}$$

Use the value of $R_{T(dummy)}$ to calculate the value for R_{KFF}.

$$R_{KFF} = \left(V_{IN(min)} - 3.5\ V\right) \times \left(65.27 \times R_{T(dummy)} + 1502\right) k\Omega \tag{11}$$

where:

- R_T is in kΩ

This value of R_{KFF} ensures that UVLO is not engaged when operating at the synchronization frequency.

SELECTING THE INDUCTOR VALUE

The inductor value determines the magnitude of ripple current in the output capacitors as well as the load current at which the converter enters discontinuous mode. Too large an inductance results in lower ripple current but is physically larger for the same load current. Too small an inductance results in larger ripple currents and a greater number of (or more expensive output capacitors for) the same output ripple voltage requirement. A good compromise is to select the inductance value such that the converter doesn't enter discontinuous mode until the load approximated somewhere between 10% and 30% of the rated output. The inductance value is described in Equation 12.

$$L = \frac{\left(V_{IN} - V_O\right) \times V_O}{V_{IN} \times \Delta I \times f_{SW}} \quad (H) \tag{12}$$

where:

- V_O is the output voltage
- ΔI is the peak-to-peak inductor current

APPLICATION INFORMATION (continued)

CALCULATING THE OUTPUT CAPACITANCE

The output capacitance depends on the output ripple voltage requirement, output ripple current, as well as any output voltage deviation requirement during a load transient.

The output ripple voltage is a function of both the output capacitance and capacitor ESR. The worst case output ripple is described in Equation 13.

$$\Delta V = \Delta I \left[ESR + \left(\frac{1}{8 \times C_O \times f_{SW}} \right) \right] \quad \left(V_{P-P}\right) \tag{13}$$

The output ripple voltage is typically between 90% and 95% due to the ESR component.

The output capacitance requirement typically increases in the presence of a load transient requirement. During a step load, the output capacitance must provide energy to the load (light to heavy load step) or absorb excess inductor energy (heavy-to-light load step) while maintaining the output voltage within acceptable limits. The amount of capacitance depends on the magnitude of the load step, the speed of the loop and the size of the inductor.

Stepping the load from a heavy load to a light load results in an output overshoot. Excess energy stored in the inductor must be absorbed by the output capacitance. The energy stored in the inductor is described in Equation 14 and Equation 15.

$$E_L = \frac{1}{2} \times L \times I^2 \quad (J) \tag{14}$$

where:

$$I^2 = \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right] \quad \left((Amperes)^2\right) \tag{15}$$

where:

- I_{OH} is the output current under heavy load conditions
- I_{OL} is the output current under light load conditions

Energy in the capacitor is given by the following equation:

$$E_C = \frac{1}{2} \times C \times V^2 \quad (J) \tag{16}$$

where:

$$V^2 = \left(V_f\right)^2 - \left(V_i\right)^2 \quad \left(Volts^2\right) \tag{17}$$

where:

- V_f is the final peak capacitor voltage
- V_i is the initial capacitor voltage

By substituting Equation 14 into Equation 13, substituting Equation 16 into Equation 15, setting Equation 13 equal to Equation 15 and solving for C_O yields the following equation.

$$C_O = \frac{L \times \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right]}{\left[\left(V_f\right)^2 - \left(V_i\right)^2 \right]} \quad (F) \tag{18}$$

Loop Compensation

Voltage-mode buck-type converters are typically compensated using Type III networks. Since the TPS40060 and TPS40061 use voltage feedforward control, the gain of the PWM modulator with voltage feedforward circuit must be included. The modulator gain is described in Figure 7, with V_{IN} being the minimum input voltage required to cause the ramp excursion to cover the entire switching period.

APPLICATION INFORMATION (continued)

$$A_{MOD} = \frac{V_{IN}}{V_S} \quad \text{or} \quad A_{MOD(db)} = 20 \times \log\left(\frac{V_{IN}}{V_S}\right) \tag{19}$$

Duty dycle, D, varies from 0 to 1 as the control voltage, V_C, varies from the minimum ramp voltage to the maximum ramp voltage, V_S. Also, for a synchronous buck converter, $D = V_O / V_{IN}$. To get the control voltage to output voltage modulator gain in terms of the input voltage and ramp voltage,

$$D = \frac{V_O}{V_{IN}} = \frac{V_C}{V_S} \quad \text{or} \quad \frac{V_O}{V_C} = \frac{V_{IN}}{V_S} \tag{20}$$

Calculate the Poles and Zeros

For a buck converter using voltage mode control there is a double pole due to the output L-C_O. The double pole is located at the frequency calculated in Equation 21.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_O}} \quad \text{(Hz)} \tag{21}$$

There is also a zero created by the output capacitance, C_O, and its associated ESR. The ESR zero is located at the frequency calculated in Equation 22.

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(Hz)} \tag{22}$$

Calculate the value of $R_{BIAS}$to set the output voltage, V_{OUT}.

$$R_{BIAS} = \frac{0.7 \times R1}{V_{OUT} - 0.7}\ \Omega \tag{23}$$

The maximum crossover frequency (0 dB loop gain) is calculated in Equation 24.

$$f_C = \frac{f_{SW}}{4} \quad \text{(Hertz)} \tag{24}$$

Typically, f_C is selected to be close to the midpoint between the L-C_O double pole and the ESR zero. At this frequency, the control to output gain has a –2 slope (-40 dB/decade), while the Type III topology has a +1 slope (20 dB/decade), resulting in an overall closed loop –1 slope (–20 dB/decade). Figure 9 shows the modulator gain, L-C filter, output capacitor ESR zero, and the resulting response to be compensated.

A Type III topology, shown in Figure 10, has two zero-pole pairs in addition to a pole at the origin. The gain and phase boost of a Type III topology is shown in Figure 11. The two zeros are used to compensate the L-C_O double pole and provide phase boost. The double pole is used to compensate for the ESR zero and provide controlled gain roll-off. In many cases the second pole can be eliminated and the amplifier's gain roll-off used to roll-off the overall gain at higher frequencies.

APPLICATION INFORMATION (continued)

PWM MODULATOR RELATIONSHIPS

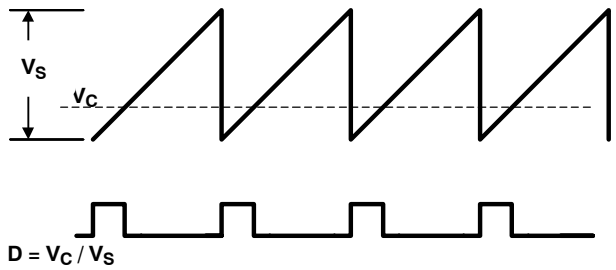


Figure 8.

MODULATOR GAIN vs SWITCHING FREQUENCY

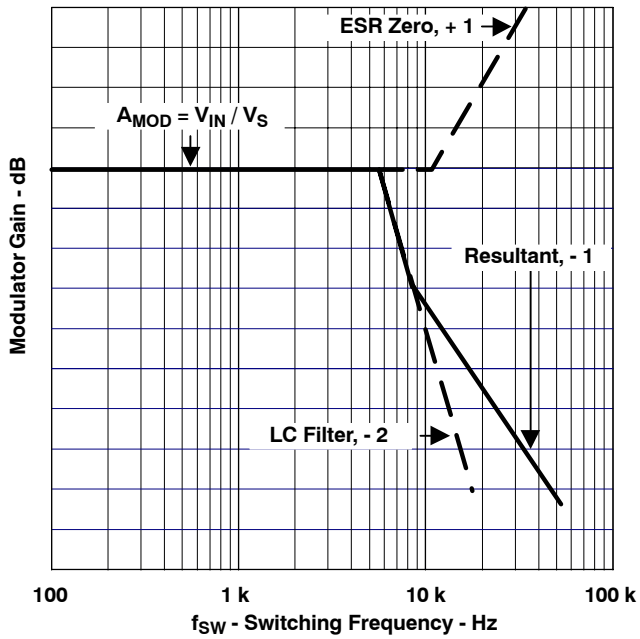


Figure 9.

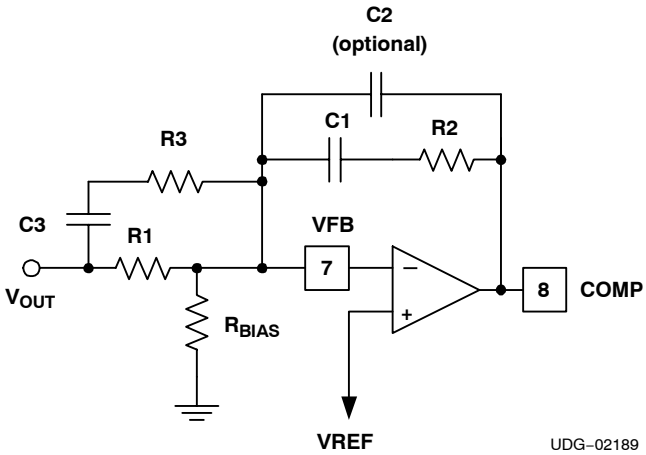


Figure 10. Type III Compensation of Configuration

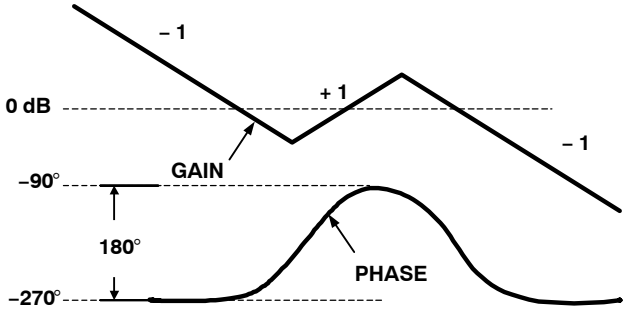


Figure 11. Type III Compensation Gain and Phase

The poles and zeros for a type III network are described in Equation 25.

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \text{ (Hz)} \qquad f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \text{ (Hz)}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \text{ (Hz)} \qquad f_{P2} = \frac{1}{2\pi \times R3 \times C3} \text{ (Hz)} \tag{25}$$

The value of R1 is somewhat arbitraty, but influences other component values. A value between 50kΩ and 100kΩ usually yields reasonable values.

The unity gain frequency is described in Equation 26.

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \text{ (Hertz)} \tag{26}$$

where G is the reciprocal of the modulator gain at f_C.

APPLICATION INFORMATION (continued)

The modulator gain as a function of frequency at f_C, is described in Equation 27.

$$AMOD(f) = AMOD \times \left(\frac{f_{LC}}{f_C}\right)^2 \quad \text{and} \quad G = \frac{1}{AMOD(f)} \tag{27}$$

Care must be taken not to load down the output of the error amplifier with the feedback resistor, R2, that is too small. The error amplifier has a finite output source and sink current which must be considered when sizing R2. Too small a value does not allow the output to swing over its full range.

$$R2_{(MIN)} = \frac{V_{C\,(max)}}{I_{SOURCE\,(min)}}\ (\Omega) = \frac{3.45\ V}{2.0\ mA} = 1.725\ k\Omega \tag{28}$$

dv/dt INDUCED TURN-ON

MOSFETs are susceptible to dv/dt turn-on particularly in high-voltage (V_{DS}) applications. The turn-on is caused by the capacitor divider that is formed by C_{GD} and C_{GS}. High dv/dt conditions and drain-to-source voltage, on the MOSFET causes current flow through C_{GD} and causes the gate-to-source voltage to rise. If the gate-to-source voltage rises above the MOSFET threshold voltage, the MOSFET turns on, resulting in large shoot-through currents. Therefore the SR MOSFET should be chosen so that the C_{GD} capacitance is smaller than the C_{GS} capacitance. A 2-Ω to 5-Ω resistor in the upper MOSFET gate lead shapes the turn-on and dv/dt of the SW node and helps reduce the induced turn-on.

HIGH-SIDE MOSFET POWER DISSIPATION

The power dissipated in the external high-side MOSFET is comprised of conduction and switching losses. The conduction losses are a function of the I_{RMS} current through the MOSFET and the $R_{DS(on)}$ of the MOSFET. The high-side MOSFET conduction losses are defined by Equation 29.

$$P_{COND} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \times \left(1 + TC_R \times \left[T_J - 25^\circ C\right]\right) \quad (W) \tag{29}$$

where:

- TC_R is the temperature coefficient of the MOSFET $R_{DS(on)}$

The TC_R varies depending on MOSFET technology and manufacturer but is typically ranges between 0.0035 ppm/°C and 0.010 ppm/°C.

The I_{RMS} current for the high side MOSFET is described in Equation 30.

$$I_{RMS} = I_O \times \sqrt{d} \quad \left(Amperes_{RMS}\right) \tag{30}$$

The switching losses for the high-side MOSFET are descibed in Equation 31.

$$P_{SW(fsw)} = \left(V_{IN} \times I_{OUT} \times t_{SW}\right) \times f_{SW} \quad (Watts) \tag{31}$$

where:

- I_O is the DC output current
- t_{SW} is the switching rise time, typically < 20 ns
- f_{SW} is the switching frequency

Typical switching waveforms are shown in Figure 12.

APPLICATION INFORMATION (continued)

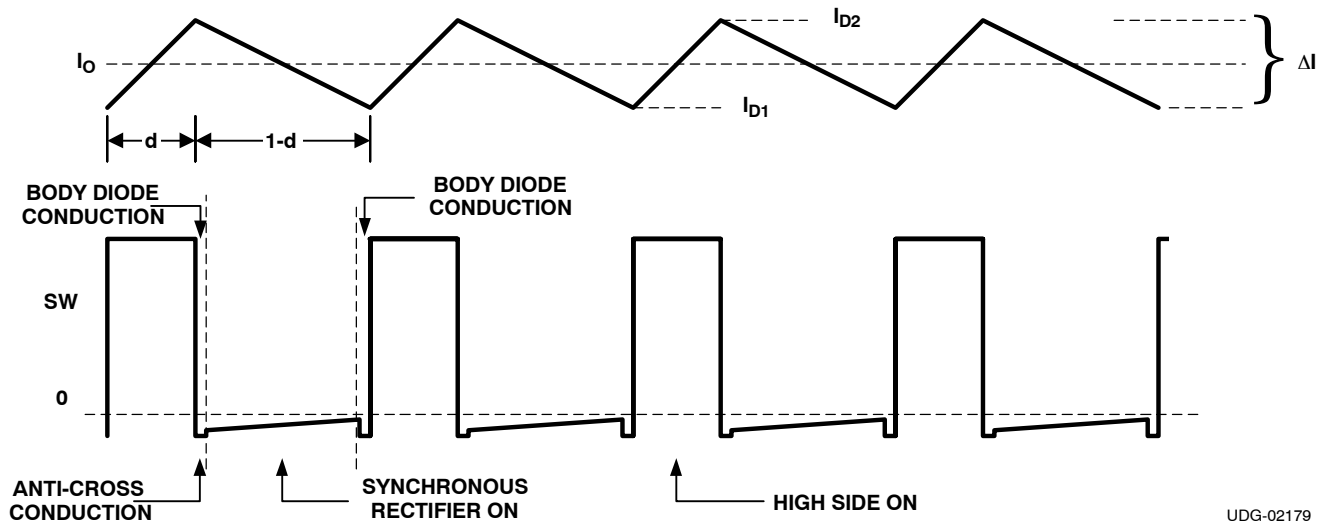


Figure 12. Inductor Current and SW Node Waveforms

The maximum allowable power dissipation in the MOSFET is determined by the following equation.

$$P_T = \frac{(T_J - T_A)}{\theta_{JA}} \quad (W) \tag{32}$$

where:

$$P_T = P_{COND} + P_{SW(fsw)} \quad (W) \tag{33}$$

and Θ_{JA} is the package thermal impedance.

SYNCHRONOUS RECTIFIER MOSFET POWER DISSIPATION

The power dissipated in the synchronous rectifier MOSFET is comprised of three components: $R_{DS(on)}$ conduction losses, body diode conduction losses, and reverse recovery losses. $R_{DS(on)}$) conduction losses can be found using Equation 29 and the RMS current through the synchronous rectifier MOSFET is described in Equation 34.

$$I_{RMS} = I_O \times \sqrt{1 - d} \quad (A_{RMS}) \tag{34}$$

The body-diode conduction losses are due to forward conduction of the body diode during the anti-cross conduction delay time. The body diode conduction losses are described by Equation 35.

$$P_{DC} = 2 \times I_O \times V_F \times t_{DELAY} \times f_{SW} \quad (W) \tag{35}$$

where:

- V_F is the body diode forward voltage
- t_{DELAY} is the delay time just before the SW node rises

The 2-multiplier is used because the body-diode conducts twice during each cycle (once on the rising edge and once on the falling edge)

The reverse recovery losses are due to the time it takes for the body diode to recovery from a forward bias to a reverse blocking state. The reverse recovery losses are described in Equation 36.

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} \quad (W) \tag{36}$$

where:

- Q_{RR} is the reverse recovery charge of the body diode

The total synchronous rectifier MOSFET power dissipation is described in Equation 37.

APPLICATION INFORMATION (continued)

$$P_{SR} = P_{DC} + P_{RR} + P_{COND} \quad (W) \tag{37}$$

TPS40060/TPS40061 POWER DISSIPATION

The power dissipation in the TPS40060 and TPS40061 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance, refer to [2] can be calculated from Equation 38.

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad (W) \tag{38}$$

And the total power dissipation in the device, assuming MOSFETs with similar gate charges for both the high-side and synchronous rectifier is described in Equation 39.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad (W) \tag{39}$$

or

$$P_T = \left[\left(2 \times Q_g \times f_{SW}\right) + I_Q\right] \times V_{IN} \quad (W) \tag{40}$$

where:

- I_Q is the quiescent operating current (neglecting drivers)

The maximum power capability of the device's PowerPad package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2 oz. copper trace and thermal pad with solder and no air flow.

Θ_{JA} = 36.51°C/W

The maximum allowable package power dissipation is related to ambient temperature by Equation 36. Substituting Equation 32 into Equation 40 and solving for f_{SW} yields the maximum operating frequency for the TPS40060 and TPS40061. The result is:

$$f_{SW} = \frac{\left(\left[\frac{(T_J - T_A)}{(\theta_{JA} \times V_{DD})}\right] - I_Q\right)}{(2 \times Q_g)} \quad (Hz) \tag{41}$$

LAYOUT CONSIDERATIONS

THE PowerPAD™ PACKAGE

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. For maximum thermal performance, the circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depends on the size of the PowerPAD package. For a 16-pin TSSOP (PWP) package the dimensions of the circuit board pad are 5 mm x 3.4 mm. The dimensions of the package pad are shown in Figure 13.

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to *PowerPAD Thermally Enhanced Package*[2] for more information on the PowerPAD package.

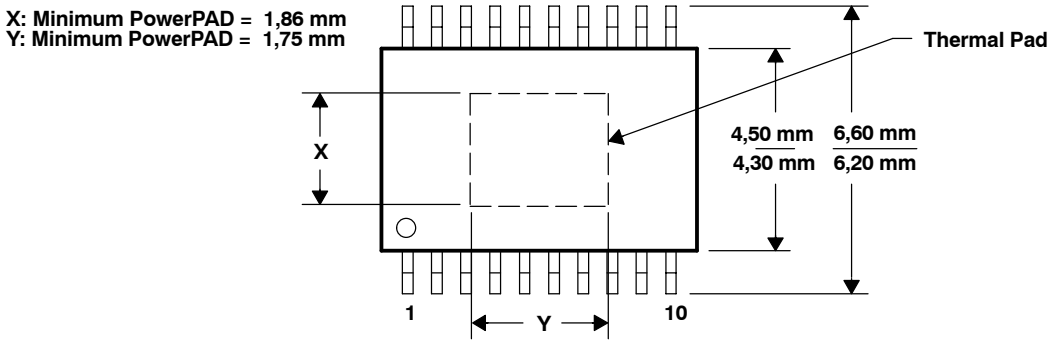


Figure 13. PowerPAD Dimensions

MOSFET PACKAGING

MOSFET package selection depends on MOSFET power dissipation and the projected operating conditions. In general, for a surface-mount applications, the DPAK style package provides the lowest thermal impedance (θ_{JA}) and, therefore, the highest power dissipation capability. However, the effectiveness of the DPAK depends on proper layout and thermal management. The θ_{JA}specified in the MOSFET data sheet refers to a given copper area and thickness. In most cases, a thermal impedance of 40°C/W requires one square inch of 2-ounce copper on a G-10/FR-4 board. Lower thermal impedances can be achieved at the expense of board area. Please refer to the selected MOSFET's data sheet for more information regarding proper mounting.

GROUNDING AND CIRCUIT LAYOUT CONSIDERATIONS

The device provides separate signal ground (SGND) and power ground (PGND) pins. It is important that circuit grounds are properly separated. Each ground should consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (BP10), and the input capacitor should be connected to PGND plane at the input capacitor.

Sensitive nodes such as the FB resistor divider, R_T, and ILIM should be connected to the SGND plane. The SGND plane should only make a single point connection to the PGND plane.

Component placement should ensure that bypass capacitors (BP10, BP5, and BPN10) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BPN10, and the switch node (SW).

DESIGN EXAMPLE

- Input voltage: 18 V_{DC} to 55 V_{DC}
- Output voltage: 3.3 V ±2%
- Output current: 5 A (maximum, steady-state), 7 A (surge, 10-ms duration, 10% duty cycle maximum)
- Output ripple: 33 mV_{P-P} at 5 A
- Output load response: 0.3 V => 10% to 90% step load change
- Operating temperature: –40°C to 85°C
- f_{SW} = 130 kHz

1. Calculate maximum and minimum duty cycles

$$d_{MIN} = \frac{V_{O(min)}}{V_{IN(max)}} = 0.0588 \qquad d_{MAX} = \frac{V_{O(max)}}{V_{IN(min)}} = = 0.187 \tag{42}$$

2. Select switching frequency

The switching frequency is based on the minimum duty cycle ratio and the propagation delay of the current limit comparator. In order to maintain current limit capability, the on time of the upper MOSFET, t_{ON}, must be greater than 330 ns (see Electrical Characteristics table). Therefore

$$\frac{V_{O(min)}}{V_{IN(max)}} = \frac{t_{ON}}{T_{SW}} \quad \text{or} \tag{43}$$

$$\frac{1}{T_{SW}} = f_{SW} = \left[\frac{\left(\frac{V_{O(min)}}{V_{IN(max)}}\right)}{T_{ON}}\right] \tag{44}$$

Using 400 ns to provide margin,

$$f_{SW} = \frac{0.0588}{400\ \text{ns}} = 147\ \text{kHz} \tag{45}$$

Since the oscillator can vary by 10%, decrease f_{SW}, by 10%

$$f_{SW} = 0.9 \times 147\ \text{kHz} = 130\ \text{kHz}$$

and therefore choose a frequency of 130 kHz.

3. SelectΔ I

In this case ΔI is chosen so that the converter enters discontinuous mode at 20% of nominal load.

$$\Delta I = I_O \times 2 \times 0.2 = 5 \times 2 \times 0.2 = 2.0\ \text{A} \tag{46}$$

4. Calculate the power losses

Power losses in the high-side MOSFET (Si9407AGY) at 55-V_{IN} where switching losses dominate can be calculated from Equation 46 through Equation 49.

$$I_{RMS} = I_O \times \sqrt{d} = 5 \times \sqrt{0.0588} = 1.2\ \text{A} \tag{47}$$

substituting Equation 30 into Equation 29 yields

$$P_{COND} = 1.2^2 \times 0.12 \times (1 + 0.007 \times (150 - 25)) = 0.324\ \text{W} \tag{48}$$

and from Equation 31, the switching losses can be determined.

DESIGN EXAMPLE (continued)

$$P_{SW(fsw)} = \left(V_{IN} \times I_O \times t_{SW}\right) \times f_{SW} = 55\ V \times 5\ A \times 20\ ns \times 130\ kHz = 0.715\ W \quad (49)$$

The MOSFET junction temperature can be found by substituting Equation 33 into Equation 32

$$T_J = \left(P_{COND} + P_{SW}\right) \times \theta_{JA} + T_A = (0.324 + 0.715) \times 40 + 85 = 127^{\circ}C \quad (50)$$

5. Calculate synchronous rectifier losses

The synchronous rectifier MOSFET has two (2) loss components, conduction, and diode reverse recovery losses. The conduction losses are due to I_{RMS} losses as well as body diode conduction losses during the dead time associated with the anti-cross conduction delay.

The I_{RMS} current through the synchronous rectifier from Equation 51

$$I_{RMS} = I_O \times \sqrt{1 - d} = 5 \times \sqrt{1 - 0.0588} = 4.85\ A_{RMS} \quad (51)$$

The synchronous MOSFET conduction loss from Equation 29 is:

$$P_{COND} = I_{RMS}^2 \times R_{DS(on)} = 4.85^2 \times 0.011 \times (1 + 0.007(150 - 25)) = 0.10\ W \quad (52)$$

The body diode conduction loss from Equation 35 is:

$$P_{DC} = 2 \times I_O \times V_{FD} \times t_{DELAY} \times f_{SW} = 2 \times 5.0\ A \times 0.8\ V \times 100\ ns \times 130\ kHz = 0.104\ W \quad (53)$$

The body diode reverse recovery loss from Equation 36 is:

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} = 0.5 \times 30\ nC \times 55\ V \times 130\ kHz = 0.107\ W \quad (54)$$

The total power dissipated in the synchronous rectifier MOSFET from Equation 37 is:

$$P_{SR} = P_{RR} + P_{COND} + P_{DC} = 0.107 + 0.1 + 0.104 = 0.311\ W \quad (55)$$

The junction temperature of the synchronous rectifier at 85°C is:

$$T_J = P_{SR} \times \theta_{JA} + T_A = (0.311) \times 40 + 85 = 97^{o}C \quad (56)$$

In typical applications, paralleling the synchronous rectifier MOSFET with a Schottky rectifier increases the overall converter efficiency by approximately 2% due to the lower power dissipation during the body diode conduction and reverse recovery periods.

6. Calculate the Inductor Value

The inductor value is calculated from Equation 11

$$L = \frac{(48 - 3.3) \times 3.3}{48 \times 2.0 \times 130\ kHz} = 11.8\ \mu H \quad (57)$$

A standard inductor value of 10-μH is chosen. A Coev DXM1306-10RO or Panasonic ETQPF102HFA could be used.

7. Setting the switching frequency

The clock frequency is set with a resistor (R_T) from the RT pin to ground. The value of R_T can be derived from following Equation 58, with f_{SW} in kHz.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82\ E - 06} - 23\right) k\Omega = 408\ k\Omega, \quad \text{use } 412\ k\Omega \quad (58)$$

8. Programming the Ramp Generator Circuit

The PWM ramp is programmed through a resistor (R_{KFF}) from the KFF pin to V_{IN}. The ramp generator also controls the input UVLO voltage. For an undervoltage level of 14.4V (20% below the 18 $V_{IN(min)}$, R_{KFF} is calculated in Equation 59.

DESIGN EXAMPLE (continued)

$$R_{KFF} = \left(V_{IN(min)} - 3.5\right)\left(65.27 \times R_T + 1502\right)\ \Omega = 133.7\ k\Omega,\ \text{use } 133\ k\Omega \tag{59}$$

9. Calculating the Output Capacitance (C_O)

In this example. the output capacitance is determined by the load response requirement of $\Delta V = 0.3$ V for a 1 A to 5 A step load. C_O can be calculated using Equation 18.

$$C_O = \frac{10\ \mu H \times \left(5^2 - 1^2\right)}{\left(3.3^2 - 3.0^2\right)} = 127\ \mu F \tag{60}$$

Using Equation 13 calculate the ESR required to meet the output ripple requirements.

$$33\ mV = 2.0\left(ESR + \frac{1}{8 \times 127\ \mu F \times 130\ kHz}\right) \tag{61}$$

ESR = 12.7 mΩ

In order to get the required ESR, the capacitance needs to be greater than the 127-μF calculated. For example, a single Panasonic SP capacitor, 180-μF with ESR of 12 mΩ can be used. Re-calculating the ESR required with the new value of 180-μF is shown in Equation 62.

$$33\ mV = 2.0\left(ESR + \frac{1}{8 \times 180\ \mu F \times 130\ kHz}\right) \tag{62}$$

ESR = 13.8 mΩ

10. Calculate the Soft-Start Capacitor (C_{SS})

This design requires a soft-start time (t_{START}) of 1 ms. C_{SS} is calculated in Equation 63.

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times 1\ ms = 3.28\ nF = 3300\ pF \tag{63}$$

11. Calculate the Current Limit Resistor (R_{ILIM})

The current limit set point depends on t_{START}, V_O, C_O and I_{LOAD} at start up as shown in Equation 7.

$$I_{LIM} > \frac{180\ \mu F \times 3.3}{1\ m} + 7.0 = 7.6\ A \tag{64}$$

Set I_{LIM} for 10.0 A minimum, then from Equation 7

$$R_{ILIM} = \frac{10 \times 0.14}{I_{SINK}} + \frac{V_{OS}}{I_{SINK}}\ \Omega = \frac{10 \times 0.14}{8.3\ \mu A} + \frac{(50\ mV)}{8.3\ \mu A}\ \Omega = 175\ k\Omega = 174\ k\Omega \tag{65}$$

12. Calculate Loop Compensation Values

Calculate the DC modulator gain (A_{MOD}) from Equation 19.

$$A_{MOD} = \frac{10}{2} = 5 \tag{66}$$

$$A_{MOD(dB)} = 20 \times \log(5.0) = 14\ dB \tag{67}$$

Calculate the output poles and zeros from Equation 21 and Equation 22 of the L-C filter.

$$f_{LC} = \frac{1}{2\pi\sqrt{10\ \mu H \times 180\ \mu F}} = 3.7\ kHz \tag{68}$$

and

$$f_Z = \frac{1}{2\pi \times 0.012 \times 180\ \mu F} = 74\ kHz \tag{69}$$

Select the close-loop 0 dB crossover frequency, f_C. For this example f_C = 10 kHz.

DESIGN EXAMPLE (continued)

Select the double zero location for the Type III compensation network at the output filter double pole at 3.7 kHz.

Select the double pole location for the Type III compensation network at the output capacitor ESR zero at 73.7 kHz.

The amplifier gain at the crossover frequency of 10 kHz is determined by the reciprocal of the modulator gain AMOD at the crossover frequency from Equation 27.

$$A_{MOD(f)} = A_{MOD} \times \left(\frac{f_{LC}}{f_C}\right)^2 = 5 \times \left(\frac{3.7\ \text{kHz}}{10\ \text{kHz}}\right)^2 = 0.68 \tag{70}$$

And also from Equation 27.

$$G = \frac{1}{A_{MOD(f)}} = \frac{1}{0.68} = 1.46 \tag{71}$$

Choose R1 = 100 kΩ

The poles and zeros for a Type III network are described in Equation 25 and Equation 26.

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \therefore C3 = \frac{1}{2\pi \times 100\ \text{k}\Omega \times 3.7\ \text{kHz}} = 430\ \text{pF, choose 470 pF} \tag{72}$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \therefore R3 = \frac{1}{2\pi \times 470\ \text{pF} \times 73.3\ \text{kHz}} = 4.62\ \text{k}\Omega\text{, choose 4.64 k}\Omega \tag{73}$$

$$f_C = \frac{1}{2\pi \times R1 \times C2 \times G} \therefore C2 = \frac{1}{2\pi \times 100\ \text{k}\Omega \times 3.29 \times 1.46\ \text{kHz}} = 109\ \text{pF, choose 100 pF} \tag{74}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \therefore R2 = \frac{1}{2\pi \times 100\ \text{pF} \times 73.3\ \text{kHz}} = 21.7\ \text{k}\Omega\text{, choose 21.5 k}\Omega \tag{75}$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \therefore C1 = \frac{1}{2\pi \times 21.5\ \text{k}\Omega \times 3.7\ \text{kHz}} = 2000\ \text{pF, choose 1800 pF} \tag{76}$$

Calculate the value of R_{BIAS} from Equation 23 with R1 = 100 kΩ.

$$R_{BIAS} = \frac{0.7\ \text{V} \times R1}{V_O - 0.7\ \text{V}} = \frac{0.7\ \text{V} \times 100\text{k}\Omega}{3.3\ \text{V} - 0.7\ \text{V}} = 26.9\ \text{k}\Omega\text{, choose 26.7 k}\Omega \tag{77}$$

CALCULATING THE BPN10 AND BP10V BYPASS CAPACITANCE

The size of the bypass capacitor depends on the total gate charge of the MOSFET being used and the amount of droop allowed on the bypass capacitor. The BPN10 capacitance, allowing for a 0.5-V droop on the BPN10 pin from Equation 8 is shown in Equation 78.

$$C_{BPN10} = \frac{Q_g}{\Delta V} = \frac{30\ \text{nC}}{0.5} = 60\ \text{nF} \tag{78}$$

and the BP10V capacitance from Equation 9 is shown in Equation 79.

$$C_{BP10V} = \frac{Q_{gSR}}{\Delta V} = \frac{57\ \text{nC}}{0.5} = 114\ \text{nF} \tag{79}$$

For this application, a 0.1-μF capacitor was used for the BPN10V and a 1.0-μF was used for the BP10V bypass ccapacitor. Figure 14 shows component selection for the 18-V through 55-V to 3.3-V at 5-A dc-to-dc converter specified in the design example.

GATE DRIVE CONFIGURATION

Due to the possibility of dv/dt induced turn-on from the fast MOSFET switching times, high V_{DS} voltage and low gate threshold voltage of the Si4470, the design includes a 2-Ω in the gate lead of the upper MOSFET. The resistor can be used to shape the low-to-high transition of the SWitch node and reduce the tendancy of dv/dt-induced turn on.

DESIGN EXAMPLE (continued)

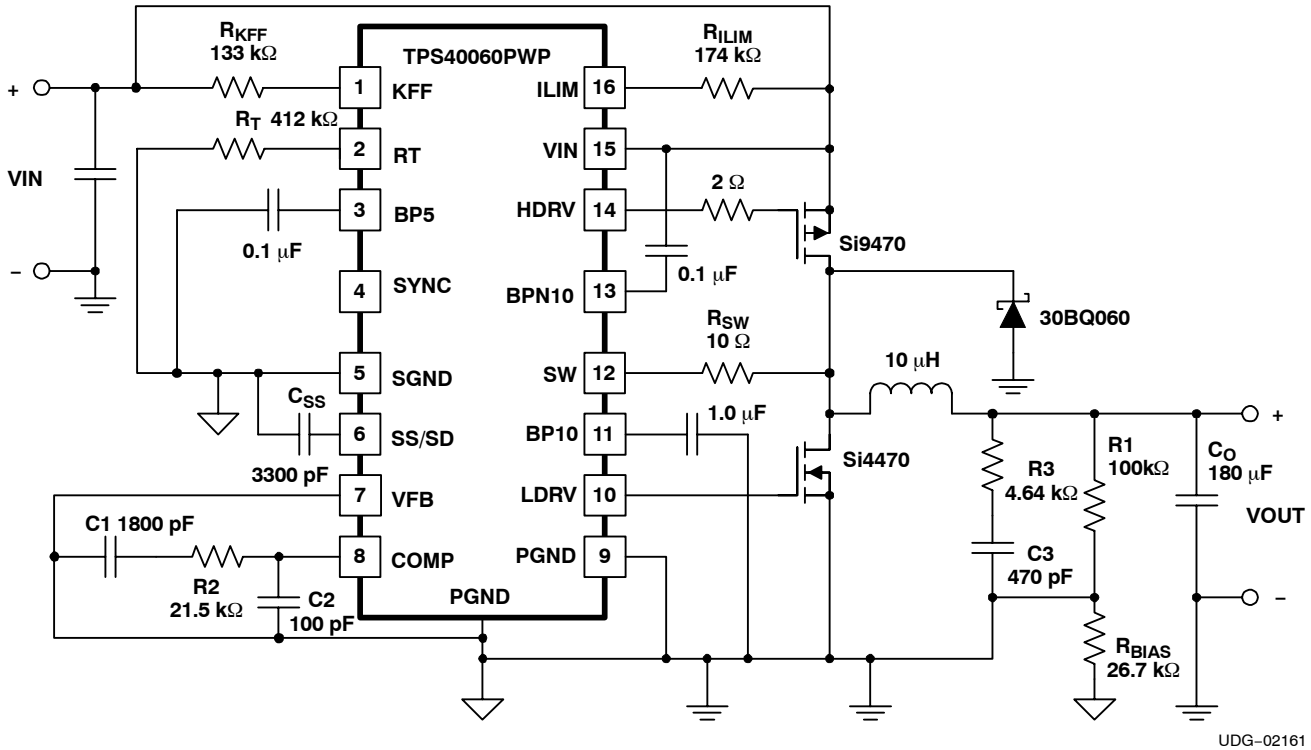


Figure 14. Design Example, 48 V to 3.3 V at 5 A dc-to-dc Converter

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2. *PowerPAD Thermally Enhanced Package* Texas Instruments, Semiconductor Group, Technical Brief: TI Literature No. SLMA002

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