19-1413; Rev 0; 12/98

EVALUATION KIT AVAILABLE

MAXIM

# +5V Single-Supply, 1Msps, 16-Bit Self-Calibrating ADC

MAX1200

## General Description

The MAX1200 16-bit, monolithic, analog-to-digital converter (ADC) is capable of conversion rates up to 1Msps. This CMOS integrated circuit uses a fully differential, pipelined architecture with digital error correction and a short self-calibration to ensure 16-bit linearity at full sample rates. An on-chip track/hold (T/H) maintains superb dynamic performance up to the Nyquist frequency. The MAX1200 operates from a single +5V supply.

The fully differential inputs allow an input swing of $\pm V_{REF}$. The reference is also differential with the positive reference (RFPF) typically connected to +4.096V and the negative reference (RFNF) connected to analog ground. Additional sensing pins (RFPS, RFNS) are provided to compensate for any resistive divider action that may occur. A single-ended input is also possible using two operational amplifiers.

Power dissipation is typically only 273mW at +5V, at a sampling rate of 1Msps. The device employs a CMOS-compatible, 16-bit parallel, two's complement output data format. For a higher sampling speed (up to 2.2Msps) but lower resolution (14-bit), select the MAX1201, a pin-compatible version of the MAX1200.

The MAX1200 is available in an MQFP package and operates over the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges.

## Applications

- High-Resolution Imaging
- Communications
- Scanners
- Data Acquisition
- Instrumentation

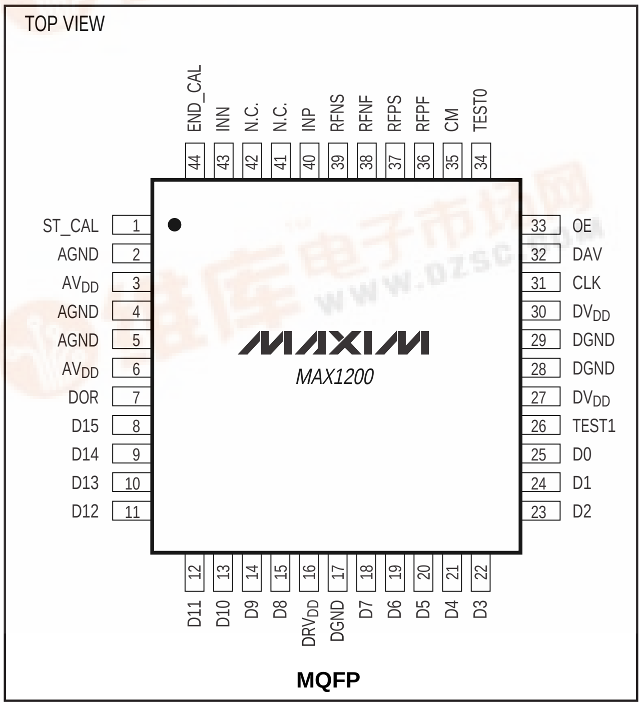
## Features

- ♦ **Monolithic 16-Bit, 1Msps A/D Converter**
- ♦ **Single +5V Supply**
- ♦ **$\pm V_{REF}$ Differential Input Voltage Range**
- ♦ **87dB SNR for $f_{IN}$ = 100kHz**
- ♦ **91dB SFDR for $f_{IN}$ = 100kHz**
- ♦ **273mW Low-Power Dissipation**
- ♦ **±0.5LSB Differential Nonlinearity Error**
- ♦ **Three-State, Two's Complement Output Data**
- ♦ **On-Demand Self-Calibration**
- ♦ **Pin-Compatible 14-Bit Versions Available (1Msps MAX1205, 2.2Msps MAX1201)**

## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | DNL (LSB) |
|---|---|---|---|
| MAX1200ACMH | 0°C to +70°C | 44 MQFP | ±0.5 |
| MAX1200BCMH | 0°C to +70°C | 44 MQFP | — |
| MAX1200AEMH | -40°C to +85°C | 44 MQFP | ±0.5 |
| MAX1200BEMH | -40°C to +85°C | 44 MQFP | — |

## Pin Configuration



# +5V Single-Supply, 1Msps, 16-Bit Self-Calibrating ADC

## ABSOLUTE MAXIMUM RATINGS

$AV_{DD}$ to AGND, DGND ....+7V
$DV_{DD}$ to DGND, AGND ....+7V
$DRV_{DD}$ to DGND, AGND ....+7V
INP, INN, RFPF, RFPS,
RFNF, RFNS, CLK, CM ....(AGND - 0.3V) to ($AV_{DD}$ + 0.3V)
Digital Inputs to DGND ....-0.3V to ($DV_{DD}$ + 0.3V)
Digital Output (DAV) to DGND ....-0.3V to ($DRV_{DD}$ + 0.3V)
Other Digital Outputs to DGND ....-0.3V to ($DRV_{DD}$ + 0.3V)

Continuous Power Dissipation ($T_A$ = +70°C)
44-Pin MQFP (derate 11.11mW/°C above +70°C) ....889mW
Operating Temperature Ranges ($T_A$)
MAX1200_CMH ....0°C to +70°C
MAX1200_EMH ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($AV_{DD}$ = +5V ±5%, $DV_{DD}$ = $DRV_{DD}$ = +3.3V, $V_{RFPS}$ = +4.096V, $V_{RFNS}$ = AGND, $V_{CM}$ = +2.048V, $V_{IN}$ = -0.5dBFS, $f_{CLK}$ = 2.048MHz; digital output load ≤ 20pF; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | |
| Input Voltage Range (Note 2) | $V_{IN}$ | Single-ended | | 4.096 | | V |
| | | Differential | | ±4.096 | | |
| Input Resistance (Note 3) | $R_I$ | | | 55 | | kΩ |
| Input Capacitance | $C_I$ | Per side in track mode | | 21 | | pF |
| **EXTERNAL REFERENCE** | | | | | | |
| Reference Voltage (Note 4) | $V_{REF}$ | | | 4.096 | 4.5 | V |
| Reference Input Resistance | $R_{REF}$ | | 700 | 1000 | | Ω |
| **TRANSFER CHARACTERISTICS** | | | | | | |
| Resolution (No missing codes; Note 5) | RES | After calibration, guaranteed for MAX1200A only | 16 | | | Bits |
| Integral Nonlinearity | INL | | | ±3.5 | | LSB |
| Differential Nonlinearity | DNL | MAX1200A | -1 | ±0.5 | +1 | LSB |
| | | MAX1200B | | ±0.6 | | |
| Offset Error | | | -0.2 | ±0.003 | +0.2 | %FSR |
| Gain Error | | | -5 | -3 | 5 | %FSR |
| Input-Referred Noise | | | | 75 | | $\mu V_{RMS}$ |
| **DYNAMIC SPECIFICATIONS** (Note 6) | | | | | | |
| Maximum Sampling Rate | $f_{SAMPLE}$ | $f_{SAMPLE} = f_{CLK} / 2$ | 1.024 | | | Msps |
| Conversion Time (Pipeline Delay/Latency) | | | | 4 | | $f_{SAMPLE}$ Cycles |
| Acquisition Time | $t_{ACQ}$ | To full-scale step (0.006%) | | 125 | | ns |
| Overvoltage Recovery Time | $t_{OVR}$ | | | 450 | | ns |
| Aperture Delay | $t_{AD}$ | | | 3 | | ns |
| Aperture Jitter | $t_{AJ}$ | | | 5 | | $ps_{RMS}$ |
| Full-Power Bandwidth | | | | 3.3 | | MHz |
| Small-Signal Bandwidth | | | | 78 | | MHz |

## ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD}$ = +5V ±5%, $DV_{DD}$ = $DRV_{DD}$ = +3.3V, $V_{RFPS}$ = +4.096V, $V_{RFNS}$ = AGND, $V_{CM}$ = +2.048V, $V_{IN}$ = -0.5dBFS, $f_{CLK}$ = 2.048MHz; digital output load ≤ 20pF; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Signal-to-Noise Ratio (Note 5) | SNR | $V_{RFPS}$ = 4.096V, $V_{RFNS}$ = AGND | $f_{IN}$ = 99.5kHz | 83 | 87 | | dB |
| | | | $f_{IN}$ = 300.5kHz | | 84 | | |
| | | | $f_{IN}$ = 504.5kHz | | 83 | | |
| | | $V_{RFPS}$ = 3.5V, $V_{RFNS}$ = 1.5V | $f_{IN}$ = 99.5kHz | 78 | 83 | | |
| | | | $f_{IN}$ = 300.5kHz | | 81 | | |
| | | | $f_{IN}$ = 504.5kHz | | 80 | | |
| Spurious-Free Dynamic Range (Note 5) | SFDR | $V_{RFPS}$ = 4.096V, $V_{RFNS}$ = AGND | $f_{IN}$ = 99.5kHz | 84 | 91 | | dB |
| | | | $f_{IN}$ = 300.5kHz | | 89 | | |
| | | | $f_{IN}$ = 504.5kHz | | 88 | | |
| | | $V_{RFPS}$ = 3.5V, $V_{RFNS}$ = 1.5V | $f_{IN}$ = 99.5kHz | 85 | 92 | | |
| | | | $f_{IN}$ = 300.5kHz | | 91 | | |
| | | | $f_{IN}$ = 504.5kHz | | 90 | | |
| Total Harmonic Distortion (Note 5) | THD | $V_{RFPS}$ = 4.096V, $V_{RFNS}$ = AGND | $f_{IN}$ = 99.5kHz | | -87 | -82 | dB |
| | | | $f_{IN}$ = 300.5kHz | | -86 | | |
| | | | $f_{IN}$ = 504.5kHz | | -85 | | |
| | | $V_{RFPS}$ = 3.5V, $V_{RFNS}$ = 1.5V | $f_{IN}$ = 99.5kHz | | -90 | -84 | |
| | | | $f_{IN}$ = 300.5kHz | | -89 | | |
| | | | $f_{IN}$ = 504.5kHz | | -88 | | |
| Signal-to-Noise Ratio plus Distortion (Note 5) | SINAD | $V_{RFPS}$ = 4.096V, $V_{RFNS}$ = AGND | $f_{IN}$ = 99.5kHz | 80 | 84 | | dB |
| | | | $f_{IN}$ = 300.5kHz | | 82 | | |
| | | | $f_{IN}$ = 504.5kHz | | 81 | | |
| | | $V_{RFPS}$ = 3.5V, $V_{RFNS}$ = 1.5V | $f_{IN}$ = 99.5kHz | 77 | 82 | | |
| | | | $f_{IN}$ = 300.5kHz | | 80.5 | | |
| | | | $f_{IN}$ = 504.5kHz | | 79.5 | | |
| **POWER REQUIREMENTS** | | | | | | | |
| Analog Supply Voltage | $AV_{DD}$ | | | 4.75 | 5 | 5.25 | V |
| Analog Supply Current | $I(AV_{DD})$ | | | | 51 | 70 | mA |
| Digital Supply Voltage | $DV_{DD}$ | | | 3 | | 5.25 | V |
| Digital Supply Current | $I(DV_{DD})$ | | | | 0.4 | 1.2 | mA |
| Output Drive Supply Voltage | $DRV_{DD}$ | | | 3 | | $DV_{DD}$ | V |
| Output Drive Supply Current | $I(DRV_{DD})$ | 10pF loads on D0–D15 and DAV | | | 0.1 | 0.6 | mA |
| Power Dissipation | PDSS | | | | 273 | 377 | mW |
| Warm-Up Time | | | | | 0.1 | | sec |
| Power-Supply Rejection Ratio | PSRR | Offset | | 55 | | | dB |
| | | Gain | | 55 | | | |

# +5V Single-Supply, 1Msps, 16-Bit Self-Calibrating ADC

## TIMING CHARACTERISTICS (Figures 7, 8, 9)

($AV_{DD}$ = +5V ±5%, $DV_{DD}$ = $DRV_{DD}$ = +3.3V, $f_{CLK}$ = 2.048MHz, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Conversion Time | $t_{CONV}$ | | | 4 / $f_{SAMPLE}$ | | ns |
| Clock Period | $t_{CLK}$ | | | 488 | | ns |
| Clock HIGH Time | $t_{CH}$ | | 187 | 244 | 301 | ns |
| Clock LOW Time | $t_{CL}$ | | 187 | 244 | 301 | ns |
| Acquisition Time | $t_{ACQ}$ | | | $t_{CLK}$ / 2 | | ns |
| Output Delay | $t_{OD}$ | | | 70 | 150 | ns |
| DAV Pulse Width | $t_{DAV}$ | | | 1 / $f_{CLK}$ | | ns |
| CLK-to-DAV Rising Edge | $t_S$ | | | 65 | 145 | ns |
| Data Access Time | $t_{AC}$ | $C_L$ = 20pF | | 16 | 75 | ns |
| Bus Relinquish Time | $t_{REL}$ | | | 16 | 75 | ns |
| Calibration Time | $t_{CAL}$ | ST_CAL = $DV_{DD}$ | | 17,400 | | $f_{CLK}$ Cycles |

## DIGITAL INPUT AND OUTPUT CHARACTERISTICS

($AV_{DD}$ = +5V ±5%, $DV_{DD}$ = $DRV_{DD}$ = +3.3V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

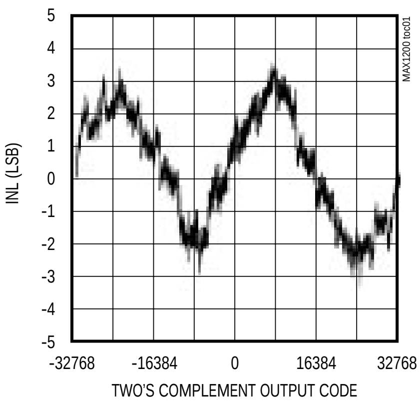
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input LOW Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input HIGH Voltage | $V_{IH}$ | | $DV_{DD}$ - 0.8 | | | V |
| Input Capacitance | | | | 4 | | pF |
| CLK Input LOW Voltage | $V_{CLK}$ | | | | 0.8 | V |
| CLK Input HIGH Voltage | $V_{CLK}$ | | $AV_{DD}$ - 0.8 | | | V |
| CLK Input Current | $I_{CLK}$ | $V_{IN}$ = 0 or $V_{DD}$ | | ±1 | ±10 | µA |
| CLK Input Capacitance | $C_{CLK}$ | | | 9 | | pF |
| Digital Input Current | $I_{IN}$ | $V_{IN}$ = 0 or $DV_{DD}$ | | ±0.1 | ±10 | µA |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 1.6mA | | 70 | 400 | mV |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 200µA | $DV_{DD}$ - 0.4 | $DV_{DD}$ - 0.03 | | V |
| Three-State Leakage Current | $I_{LEAKAGE}$ | | | ±0.1 | ±10 | µA |
| Three-State Output Capacitance | $C_{OUT}$ | | | 3.5 | | pF |

**Note 1:** Reference inputs driven by operational amplifiers for Kelvin-sensed operation.
**Note 2:** For unipolar mode, the analog input voltage, $V_{INP}$, must be within 0 and $V_{REF}$, $V_{INN}$ = $V_{CM}$ / 2; where $V_{REF}$ = $V_{RFPS}$ - $V_{RFNS}$. For differential mode, the analog input voltages $V_{INP}$ and $V_{INN}$ must be within 0 and $V_{REF}$; where $V_{REF}$ = $V_{RFPS}$ - $V_{RFNS}$. The common-mode voltage of the inputs INP and INN is $V_{CM}$ = ($V_{RFPS}$ + $V_{RFNS}$) / 2.
**Note 3:** $R_I$ varies inversely with sample rate.
**Note 4:** Minimum and maximum parameters are not tested. Guaranteed by design.
**Note 5:** Calibration remains valid for temperature changes within ±20°C and power-supply variations ±5%. Guaranteed by design.
**Note 6:** All AC specifications are shown for the differential mode.

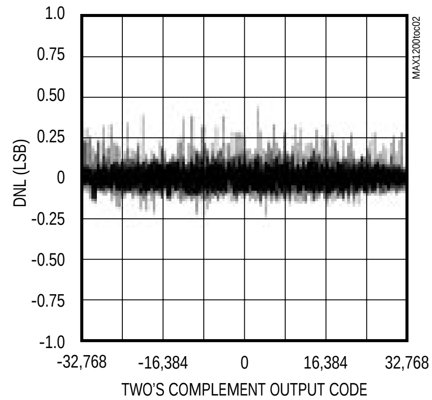
## *Typical Operating Characteristics*

($AV_{DD}$ = +5V ±5%, $DV_{DD}$ = $DRV_{DD}$ = +3.3V, **$V_{RFPS}$ = +4.096V, $V_{RFNS}$ = AGND**; $V_{CM}$ = +2.048V, differential input, $f_{CLK}$ = 2.048MHz, calibrated, $T_A$ = +25°C, unless otherwise noted.)

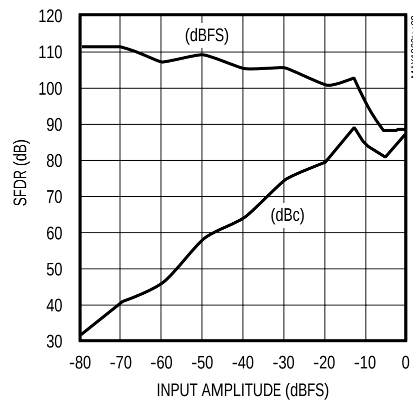
**INTEGRAL NONLINEARITY vs. TWO'S COMPLEMENT OUTPUT CODE**



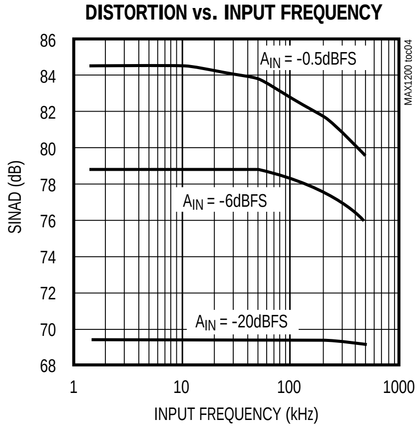

**DIFFERENTIAL NONLINEARITY vs. TWO'S COMPLEMENT OUTPUT CODE**



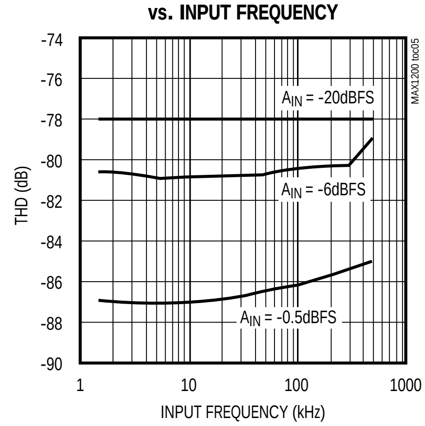

**SINGLE-TONE SPURIOUS-FREE DYNAMIC RANGE vs. INPUT AMPLITUDE ($f_{IN}$ = 99.5kHz)**



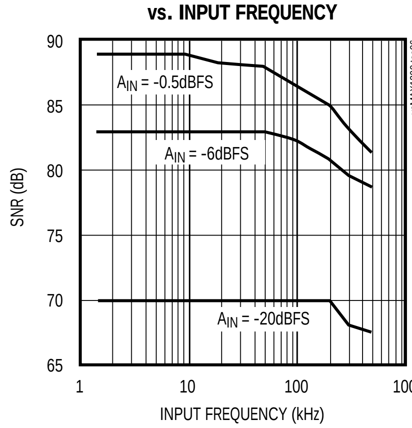

**SIGNAL-TO-NOISE RATIO PLUS DISTORTION vs. INPUT FREQUENCY**



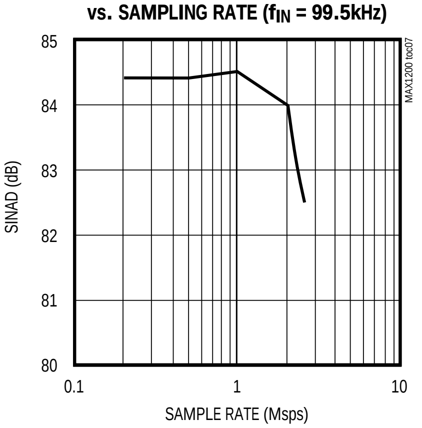

**TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY**



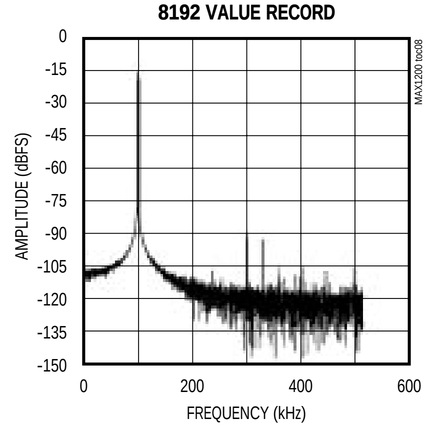

**SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY**



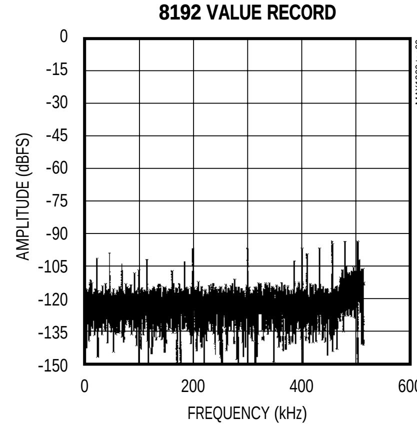

**SIGNAL-TO-NOISE RATIO PLUS DISTORTION vs. SAMPLING RATE ($f_{IN}$ = 99.5kHz)**




**TYPICAL FFT, $f_{IN}$ = 99.5kHz, 8192 VALUE RECORD**




**TYPICAL FFT, $f_{IN}$ = 504.5MHz, 8192 VALUE RECORD**

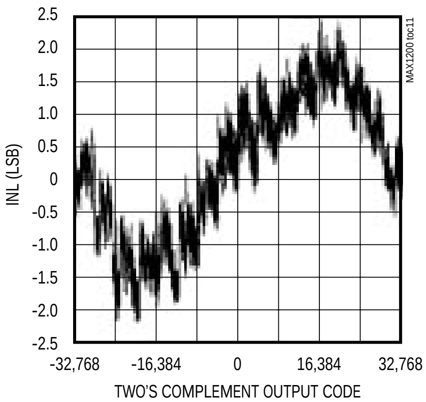


# +5V Single-Supply, 1Msps, 16-Bit Self-Calibrating ADC

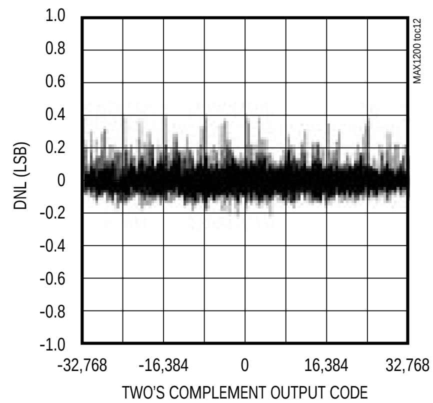
## Typical Operating Characteristics

($AV_{DD}$ = +5V ±5%, $DV_{DD}$ = $DRV_{DD}$ = +3.3V, **$V_{RFPS}$ = +3.5V, $V_{RFNS}$ = +1.5V;** $V_{CM}$ = +2.5V, differential input, $f_{CLK}$ = 2.048MHz, calibrated, $T_A$ = +25°C, unless otherwise noted.)

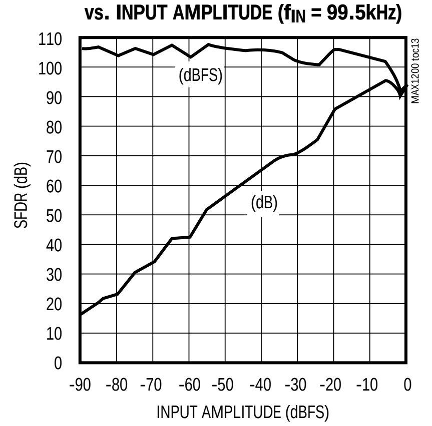
**INTEGRAL NONLINEARITY vs. TWO'S COMPLEMENT OUTPUT CODE**



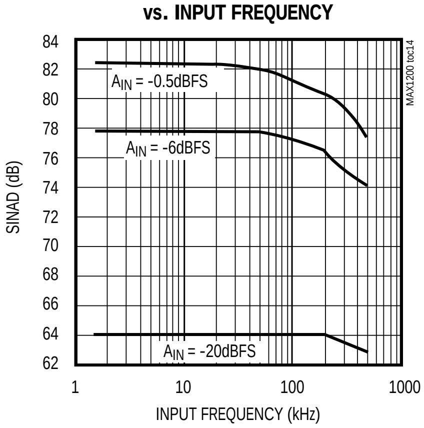

**DIFFERENTIAL NONLINEARITY vs. TWO'S COMPLEMENT OUTPUT CODE**



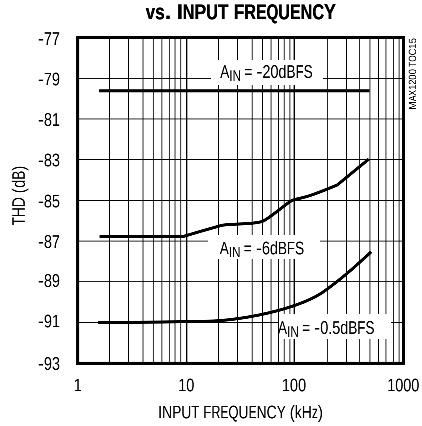

**SINGLE-TONE SPURIOUS-FREE DYNAMIC RANGE vs. INPUT AMPLITUDE ($f_{IN}$ = 99.5kHz)**



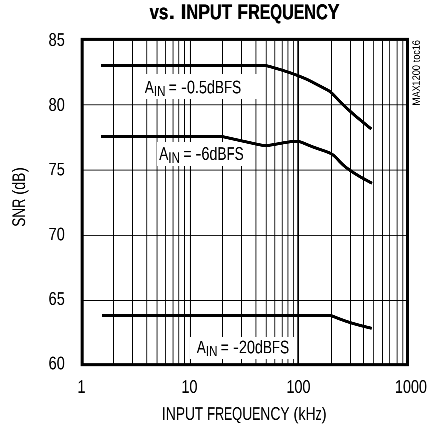

**SIGNAL-TO-NOISE RATIO PLUS DISTORTION vs. INPUT FREQUENCY**



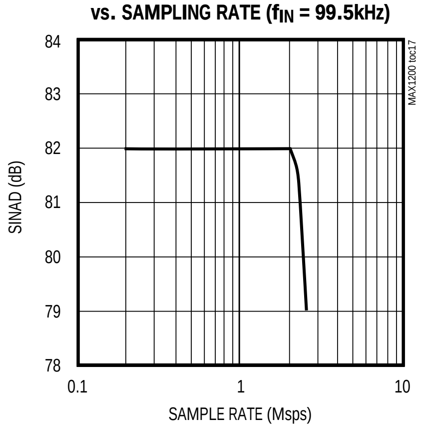

**TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY**



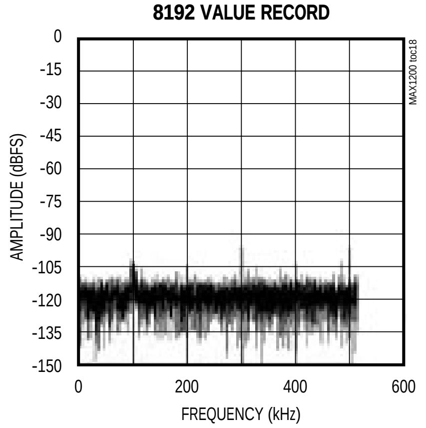

**SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY**



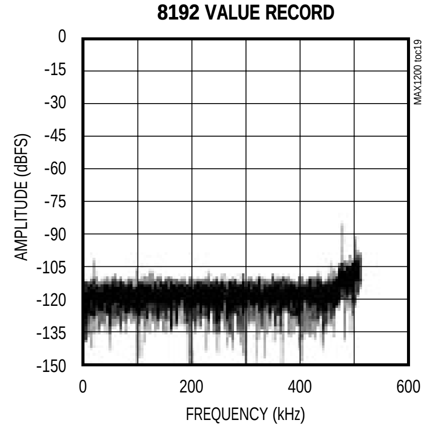

**SIGNAL-TO-NOISE RATIO PLUS DISTORTION vs. SAMPLING RATE ($f_{IN}$ = 99.5kHz)**




**TYPICAL FFT, $f_{IN}$ = 99.5kHz, 8192 VALUE RECORD**




**TYPICAL FFT, $f_{IN}$ = 504.5MHz, 8192 VALUE RECORD**



## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | ST_CAL | Digital Input to Start Calibration.<br>ST_CAL = 0: Normal conversion mode.<br>ST_CAL = 1: Start self-calibration. |
| 2, 4, 5 | AGND | Analog Ground |
| 3, 6 | $AV_{DD}$ | Analog Power Supply, +5V ±5% |
| 7 | DOR | Data Out-of-Range Bit |
| 8 | D15 | Bit 15 (MSB) |
| 9 | D14 | Bit 14 |
| 10 | D13 | Bit 13 |
| 11 | D12 | Bit 12 |
| 12 | D11 | Bit 11 |
| 13 | D10 | Bit 10 |
| 14 | D9 | Bit 9 |
| 15 | D8 | Bit 8 |
| 16 | $DRV_{DD}$ | Digital Power Supply for the Output Drivers. +3V to +5.25V, $DRV_{DD} \leq DV_{DD}$ |
| 17, 28, 29 | DGND | Digital Ground |
| 18 | D7 | Bit 7 |
| 19 | D6 | Bit 6 |
| 20 | D5 | Bit 5 |
| 21 | D4 | Bit 4 |
| 22 | D3 | Bit 3 |
| 23 | D2 | Bit 2 |
| 24 | D1 | Bit 1 |
| 25 | D0 | Bit 0 (LSB) |
| 26 | TEST1 | Test Pin 1. **Do not connect.** |
| 27, 30 | $DV_{DD}$ | Digital Power Supply, +3V to +5.25V |
| 31 | CLK | Input Clock. Receives power from $AV_{DD}$ to reduce jitter. |
| 32 | DAV | Data Valid Clock. This clock can be used to transfer the data to a memory or any other data acquisition system. |
| 33 | OE | Output Enable. OE = 0: D0–D15 and DOR are high impedance. OE = 1: All bits are active. |
| 34 | TEST0 | Test Pin 0. **Do not connect.** |
| 35 | CM | Common-Mode Voltage. Analog Input. Drive midway between positive and negative reference voltages. |
| 36 | RFPF | Positive Reference Voltage, Force Input |
| 37 | RFPS | Positive Reference Voltage, Sense Input |
| 38 | RFNF | Negative Reference Voltage, Force Input |
| 39 | RFNS | Negative Reference Voltage, Sense Input |
| 40 | INP | Positive Input Voltage |
| 41, 42 | N.C. | Not Connected. No internal connection. |
| 43 | INN | Negative Input Voltage |
| 44 | END_CAL | Digital Output for End of Calibration.<br>END_CAL = 0: Calibration in progress.<br>END_CAL = 1: Normal conversion mode. |

## Detailed Description

### Converter Operation

The MAX1200 is a 16-bit, monolithic analog-to-digital converter (ADC) capable of conversion rates up to 1Msps. It uses a multistage, fully differential, pipelined architecture with digital error correction and self-calibration to provide typically 91dB spurious-free dynamic range at a 1Msps sampling rate. It also provides excellent SNR and THD performance up to the Nyquist frequency. This makes the device suitable for applications such as data acquisition, high-resolution imaging, scanners, digital communication, and instrumentation.

Figure 1 shows the simplified, internal structure of the ADC. A switched-capacitor, pipelined architecture is used to digitize the signal at a high throughput rate. The first four stages of the pipeline use a low-resolution quantizer to approximate the input signal. The multiplying digital-to-analog converter (MDAC) stage is used to subtract the quantized analog signal from the input. The residue is then amplified with a fixed gain and passed on to the next stage. The accuracy of the converter is improved by a digital calibration algorithm which corrects for mismatches between the capacitors in the switched-capacitor MDAC. Note that the pipeline introduces latency of four sampling periods between the input being sampled and the output appearing at D15–D0.

While the device can handle both single-ended or differential inputs (see the *Requirements for Reference and Analog Signal Inputs* section), the latter mode of operation will guarantee best THD and SFDR performance. The differential input provides the following advantages compared to a single-ended operation:

- Twice as much signal input span
- Common-mode noise immunity
- Virtual elimination of the even-order harmonics
- Less stringent requirements on the input signal processing amplifiers

### Requirements for Reference and Analog Signal Inputs

Fully differential switched-capacitor circuits (SC) are used for both the reference and analog inputs (Figure 2). This allows either single-ended or differential signals to be used in the reference and/or analog signal paths. The signal voltage on these pins (INP, INN, RFP_, RFN_) should never exceed the analog supply rail, $AV_{DD}$, nor fall below ground.

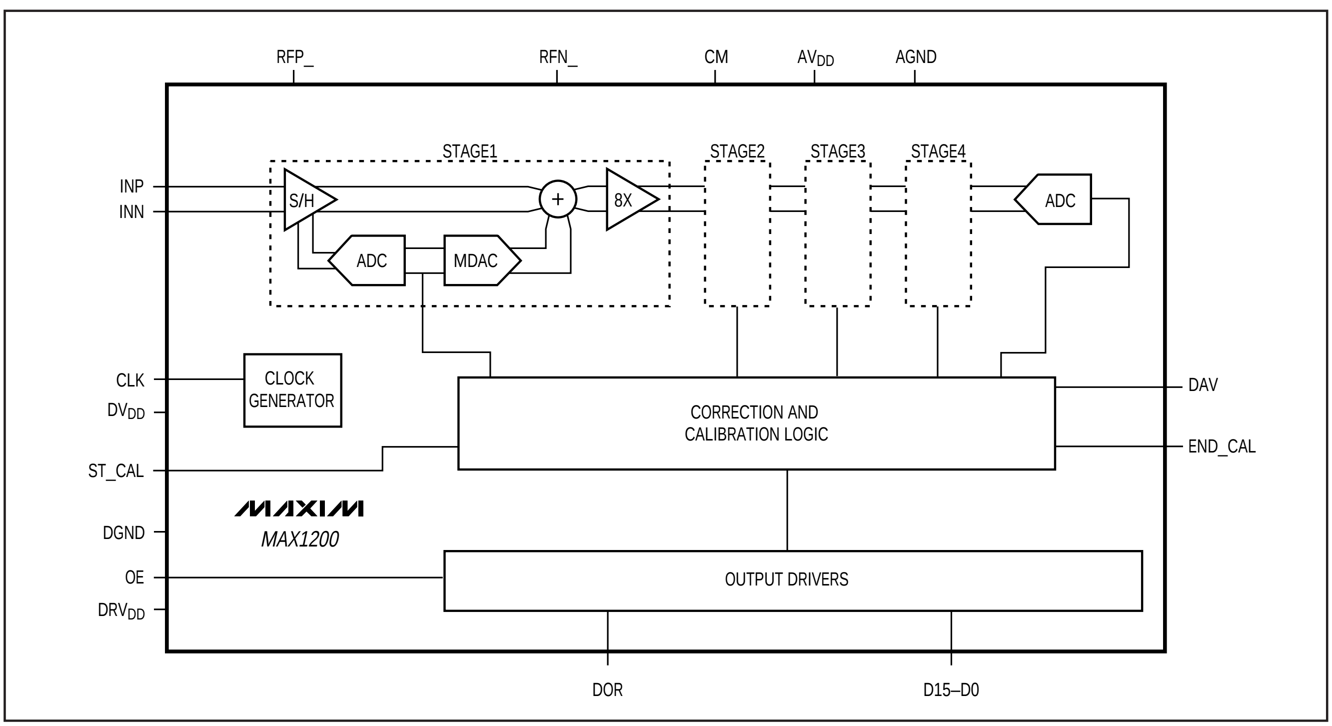



*Figure 1. Internal Functional Diagram*

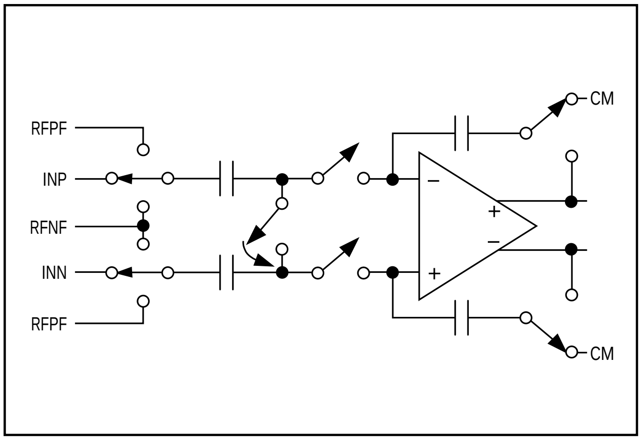



*Figure 2. Simplified MDAC Architecture*

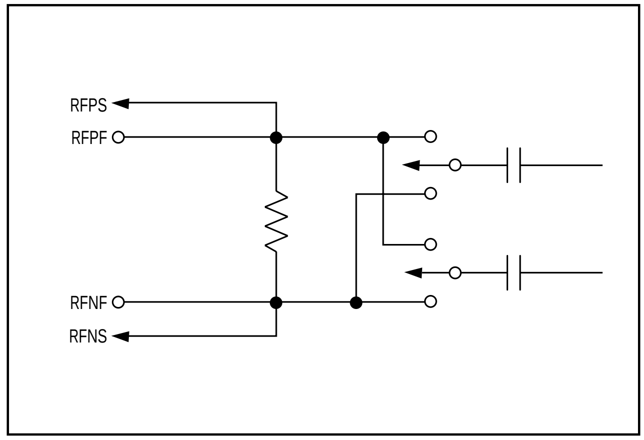



*Figure 3. Equivalent Input at the Reference Pins. The sense pins should not draw any DC current.*

### *Choice of Reference*

It is important to choose a low-noise reference such as the MAX6341, which can provide both excellent load regulation and low temperature drift. The equivalent input circuit for the reference pins is shown in Figure 3. Note that the reference pins drive approximately 1kΩ of resistance on-chip. They also drive a switched capacitor of 21pF. To meet the dynamic performance, the reference voltage is required to settle to 0.0015% within one clock cycle. Carefully choose an appropriate driving circuit (Figure 4). The capacitors at the reference pins (RFPF, RFNF) provide the dynamic charge required during each clock cycle, while the op amps ensure accuracy of the reference signals. These capacitors must have low dielectric-absorption characteristics, such as polystyrene or teflon capacitors.

The reference pins can be connected to either single-ended or differential voltages within the specified maximum levels. Typically the positive reference pin (RFPF) would be driven to +4.096V, and the negative reference pin (RFNF) connected to analog ground for best SNR performance. If THD performance is more important to the application than signal-to-noise ratio, choose a lower level, differential voltage such as $V_{RFPS}$ = +3.5V and $V_{RFNS}$ = +1.5V.

There are sense pins, RFPS and RFNS, which can be used with external amplifiers to compensate for any resistive drop on these lines, internal or external to the chip. Ensure a correct reference voltage by using proper Kelvin connections at the sense pins.

### *Common-Mode Voltage*

The switched-capacitor input circuit at the analog input allows signals between AGND and the analog power supply. Since the common-mode voltage has a strong influence on the performance of the ADC, the best results are obtained by choosing $V_{CM} = (V_{RFPS} + V_{RFNS}) / 2$. This can be achieved by using a resistive divider between the two reference potentials. Figure 4 shows a typical driving circuit for good dynamic performance.

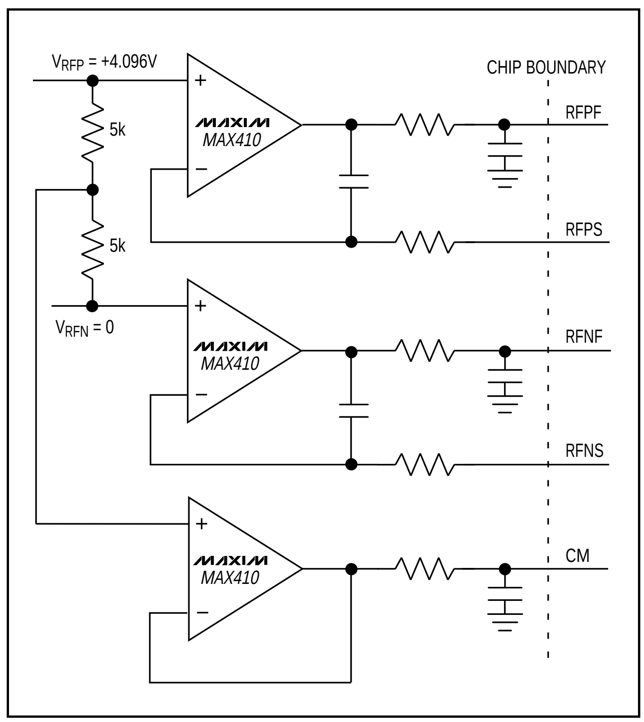



*Figure 4. Drive Circuit for Reference Pins and Common-Mode Pin*

### Analog Signal Conditioning

For single-ended inputs, the negative analog input pin (INN) is connected to the common-mode voltage pin (CM) and the positive analog input pin (INP) is connected to the input.

To take full advantage of the ADC's superior AC performance up to the Nyquist frequency, drive the chip with differential signals. In communication systems the signals may inherently be available in differential mode; however medical and/or other applications may only provide single-ended inputs. In this case, convert the single-ended signals into differential ones by using the circuit recommended in Figure 5. Use low-noise, wideband amplifiers, such as the MAX4108, to maintain the signal purity over the full-power bandwidth of the MAX1200 input.

Lowpass or bandpass signals may be required to improve the signal-to-noise and distortion of the incoming signal. For low-frequency signals (<100kHz), active filters may be used. For higher frequencies, passive filters are more convenient.

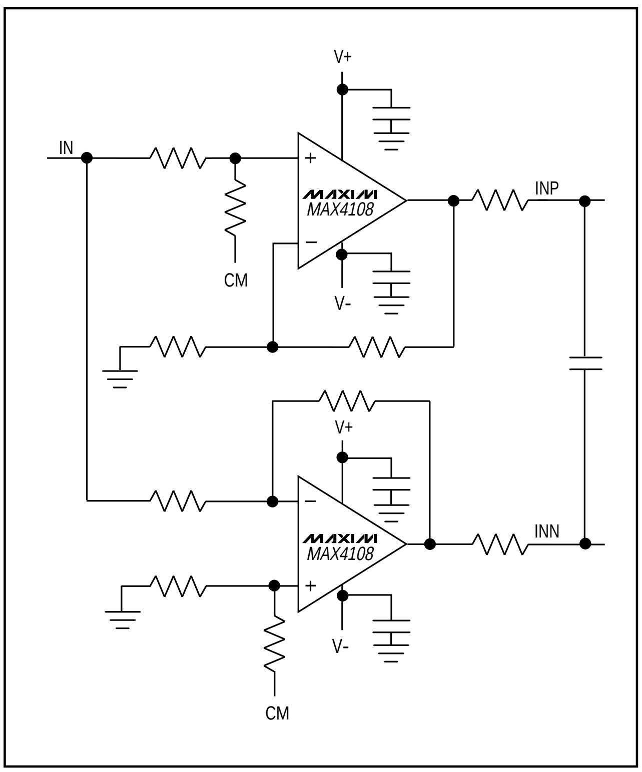



*Figure 5. A simple circuit generates differential signals from a single-ended input referred to analog ground. The common-mode voltage at INP and INN is the same as CM.*

### Single-Ended to Differential Conversion Using Transformers

An alternative single-ended to differential-ended conversion method is a balun transformer such as the CTX03-13675 from Coiltronics. An important benefit of these transformers is their ability to level-shift single-ended signals referred to ground on the primary side to optimum common-mode voltages on the secondary side. At frequencies below 20kHz the transformer core begins to saturate, causing odd-order harmonics.

### Clock Source Requirements

Pipelined ADCs typically need a 50% duty cycle clock. To avoid this constraint, the MAX1200 provides a divide-by-two circuit to relax this requirement. The clock generator should be chosen commensurate with the frequency range, amplitude, and slew rate of the signal source. If the slew rate of the input signal is small, the jitter requirement on the clock is relaxed. However, if the slew rate is high, the clock jitter needs to be kept at a minimum. For a full-scale amplitude input sine wave, the maximum possible signal-to-noise ratio (SNR) due completely to clock jitter is given by:

$$SNR_{MAX} = \frac{1}{2 \cdot \pi \cdot f_{IN} \cdot \sigma_{JITTER}}$$

For example, if $f_{IN}$ is 500kHz and $\sigma_{JITTER}$ is 10ps RMS, then the SNR limit due to jitter is about 90dB. Generating such a clock source requires a low-noise comparator and a low-phase-noise signal generator. The clock circuit shown in Figure 6 is a possible solution.

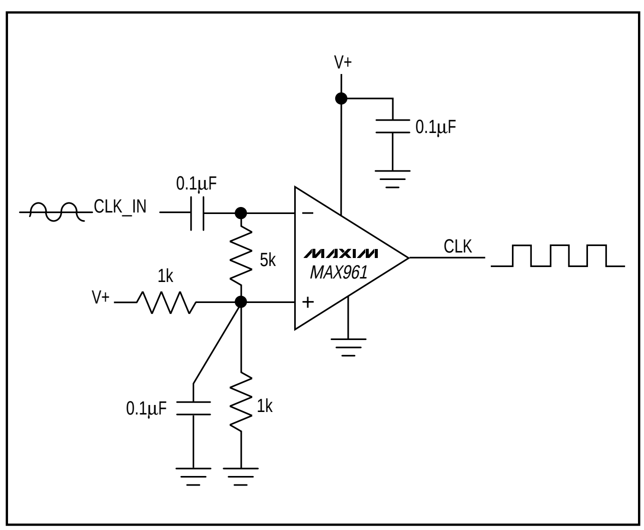



*Figure 6. Clock Generation Circuit Using Low-Noise Comparator*

### Calibration Procedure

Since the MAX1200 is based on a pipelined architecture, low-resolution quantizers ("coarse ADCs") are used to approximate the input signal. MDACs of the same resolution are then used to reconstruct the input signal, which is subtracted from the input and the residue amplified by the SC gain stage. This residue is then passed on to the next stage.

The accuracy of the MAX1200 is limited by the precision of the MDAC, which is strongly dependent on the matching of the capacitors used. The mismatch between the capacitors is determined and stored in an on-chip memory, which is later used during the conversion of the input signal.

During the calibration procedure, the clock must be running continuously. ST_CAL (start of calibration) is initiated by a positive pulse with a minimum width of four clock cycles, but not longer than about 17,400 clock cycles (Figure 8).

The ST_CAL input may be asynchronous with the clock, since it is retimed internally. With ST_CAL activated, END_CAL goes low one or two clock cycles later and remains low until the calibration is complete. During this period, the reference voltages must be stable to less than 0.01%; otherwise the calibration will be invalid. During calibration, the analog inputs INP and INN are not used; however, better performance is achieved if these inputs are static. Once END_CAL goes high (indicating that the calibration procedure is complete), the ADC is ready for conversion.

Once calibrated, the MAX1200 is insensitive to small changes (±5%) in power-supply voltage or temperature. Following calibration, if the temperature changes more than ±20°C, the device should be recalibrated to maintain optimum performance.

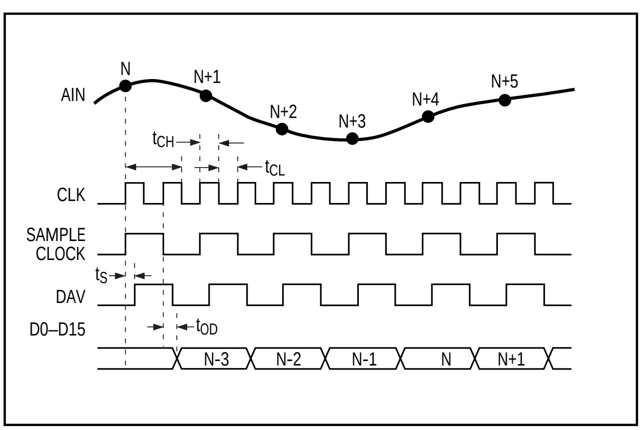



*Figure 7. Main Timing Diagram*

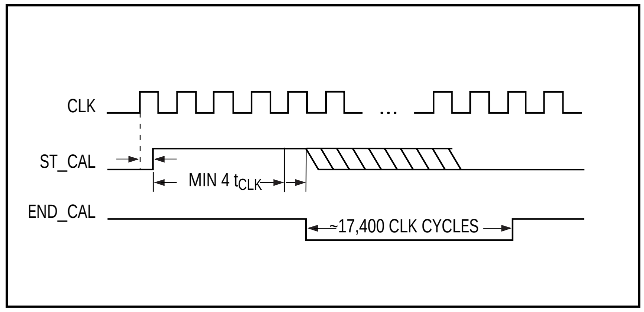



*Figure 8. Timing for Start and End of Calibration*

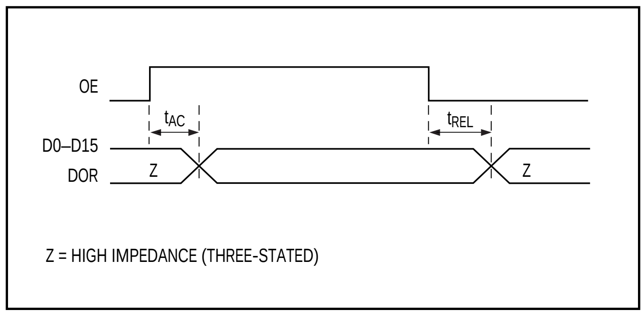



*Figure 9. Timing for Bus Access and Bus Relinquish—Controlled by Output Enable (OE)*

### Two's Complement Output

The MAX1200 outputs data in two's complement format. Table 1 shows how to convert the various full-scale inputs into their two's complement output codes.

## Applications Information

### Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{(MAX)} = (6.02 \cdot N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise which includes all spectral components minus the fundamental, the first nine harmonics, and the DC offset.

## Table 1. Two's Complement Output Codes

| SCALE | OFFSET BINARY | ONE'S COMPLEMENT | TWO'S COMPLEMENT |
|---|---|---|---|
| +FSR - 1LSB | 1111 .... 1111 | 0111 .... 1111 | 0111 .... 1111 |
| +3/4FSR | 1110 .... 0000 | 0110 .... 0000 | 0110 .... 0000 |
| +1/2FSR | 1100 .... 0000 | 0100 .... 0000 | 0100 .... 0000 |
| +1/4FSR | 1010 .... 0000 | 0010 .... 0000 | 0010 .... 0000 |
| +0 | 1000 .... 0000 | 0000 .... 0000 | 0000 .... 0000 |
| -0 | —— .... —— | —— .... —— | 1111 .... 1111 |
| -1/4FSR | 0110 .... 0000 | 1110 .... 0000 | 1101 .... 1111 |
| -1/2FSR | 0100 .... 0000 | 1100 .... 0000 | 1011 .... 1111 |
| -3/4FSR | 0010 .... 0000 | 1010 .... 0000 | 1001 .... 1111 |
| -FSR +1LSB | 0000 .... 0001 | 1000 .... 0001 | 1000 .... 0000 |
| -FSR | 0000 .... 0000 | 1000 .... 0000 | —— .... —— |

### *Signal-to-Noise Plus Distortion (SINAD)*

SINAD is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals:

$$\text{SINAD (dB)} = 20\log\left[\text{Signal}_{RMS} / (\text{Noise} + \text{Distortion})_{RMS}\right]$$

### *Effective Number of Bits (ENOB)*

ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, the effective number of bits can be calculated as follows:

$$\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$$

### *Total Harmonic Distortion (THD)*

THD is the ratio of the RMS sum of the first nine harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20\log\left[\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + \cdots + V_9^2\right)}}{V_1}\right]$$

where $V_1$ is the fundamental amplitude, and $V_2$ through $V_9$ are the amplitudes of the 2nd through 9th-order harmonics.

### *Spurious-Free Dynamic Range (SFDR)*

SFDR is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

### *Grounding and Power-Supply Decoupling*

Grounding and power-supply decoupling strongly influence the performance of the MAX1200. At 16-bit resolution, unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections; this adversely affects the SNR or SFDR. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX1200. Therefore, grounding and power-supply decoupling guidelines should be closely followed.

First, a multilayer printed circuit board (PCB) with separate ground and power-supply planes is recommended. Run high-speed signal traces directly above the ground plane. Since the MAX1200 has separate analog and digital ground buses (AGND and DGND respectively), the PCB should also have separate analog and digital ground sections connected at only one point (star ground). Digital signals should run above the digital ground plane and analog signals should run above the analog ground plane. Digital signals should be kept far away from the sensitive analog inputs, reference input senses, common-mode input, and clock input.

The MAX1200 has three power-supply inputs: analog $V_{DD}$ ($AV_{DD}$), digital $V_{DD}$ ($DV_{DD}$), and drive $V_{DD}$ ($DRV_{DD}$). Each AVDD input should be decoupled with parallel ceramic chip capacitors of values 0.1µF and 0.001µF, with these capacitors as close to the pin as possible and with the shortest possible connection to the ground plane. The $DV_{DD}$ pins should also have separate 0.1µF capacitors again adjacent to their respective pins, as should the $DRV_{DD}$ pin. Minimize the digital load capacitance. However, if the total load capacitance on each digital output exceeds 20pF, the $DRV_{DD}$ decoupling capacitor should be increased or, preferably, digital buffers should be added.

The power-supply voltages should also be decoupled with large tantalum or electrolytic capacitors at the point they enter the PCB. Ferrite beads with additional decoupling capacitors forming a pi network may improve performance.

The analog power-supply input ($AV_{DD}$) for the MAX1200 is typically +5V while the digital supplies can vary from +3V to +5V. Usually, $DV_{DD}$ and $DRV_{DD}$ pins are connected to the same power supply. Note that the $DV_{DD}$ supply voltage must be greater than or equal to the $DRV_{DD}$ voltage. For example, a digital +3.3V supply could be connected to $DRV_{DD}$ while a cleaner +5V supply is connected to $DV_{DD}$, resulting in slightly improved performance. Alternatively, the +3.3V supply could be connected to both $DRV_{DD}$ and $DV_{DD}$. However, the +3.3V supply must **not** be connected to $DV_{DD}$ while the +5V supply is connected to $DRV_{DD}$ (Table 2).

### Table 2. Power-Supply Voltage Combinations

| $AV_{DD}$ (V) | $DV_{DD}$ (V) | $DRV_{DD}$ (V) | ALLOWED/ NOT ALLOWED |
|---|---|---|---|
| +5 | +5 | +5 | Allowed |
| +5 | +5 | +3.3 | Allowed |
| +5 | +3.3 | +3.3 | Allowed |
| +5 | +3.3 | +5 | Not Allowed |

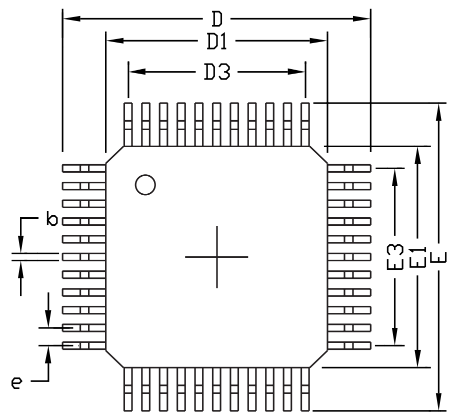
## *Chip Information*

TRANSISTOR COUNT: 56,577

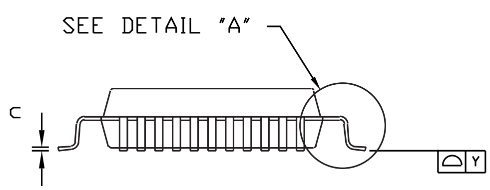
SUBSTRATE CONNECTED TO AGND

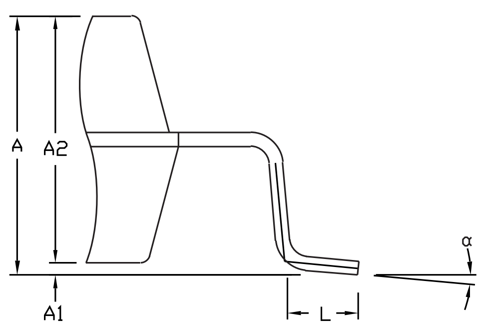
## Package Information

MQFP44.EPS




| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 2.032 | 2.388 | 0.080 | 0.094 |
| A1 | 0.102 | 0.254 | 0.004 | 0.010 |
| A2 | 1.930 | 2.134 | 0.076 | 0.084 |
| b | 0.305 | 0.457 | 0.012 | 0.018 |
| c | 0.102 | 0.254 | 0.004 | 0.010 |
| D | 12.954 | 13.462 | 0.510 | 0.530 |
| D1 | 9.906 | 10.109 | 0.390 | 0.398 |
| D3 | 8.000 REF | | 0.315 REF | |
| E | 12.954 | 13.462 | 0.510 | 0.530 |
| E1 | 9.906 | 10.109 | 0.390 | 0.398 |
| E3 | 8.000 REF | | 0.315 REF | |
| e | 0.800 REF | | 0.0315 REF | |
| L | 0.635 | 0.940 | 0.025 | 0.037 |
| α | °0 | °10 | °0 | °10 |




DETAIL "A"

NOTES:

1. D1&E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-AA-2.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, MQFP, 44L

| APPROVAL | DOCUMENT CONTROL NO. | REV | |
|---|---|---|---|
| | 21-0826 | C | 1/1 |

**NOTES**

## NOTES