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HIGH-EFFICIANCY MIDRANGE INPUT SYNCHRONOUS BUCK CONTROLLER WITH VOLTAGE FEED-FORWARD

FEATURES

- Operation Over 4.5-V to 28-V Input Range
- Programmable Fixed-Frequency up to 1-MHz Voltage-Mode Controller
- Predictive Gate Drive™ With Anti-Cross Conduction Circuitry
- <1% Internal 700-mV Reference
- Internal Gate Drive Outputs for High-Side and Synchronous N-Channel MOSFETs
- 16-Pin PowerPAD™ Package
- Thermal Shutdown Protection
- TPS40070: Source Only
- TPS40071: Source/Sink
- Programmable High-Side Sense Short Circuit Protection

APPLICATIONS

- Power Modules
- Networking/Telecom
- Industrial
- Servers

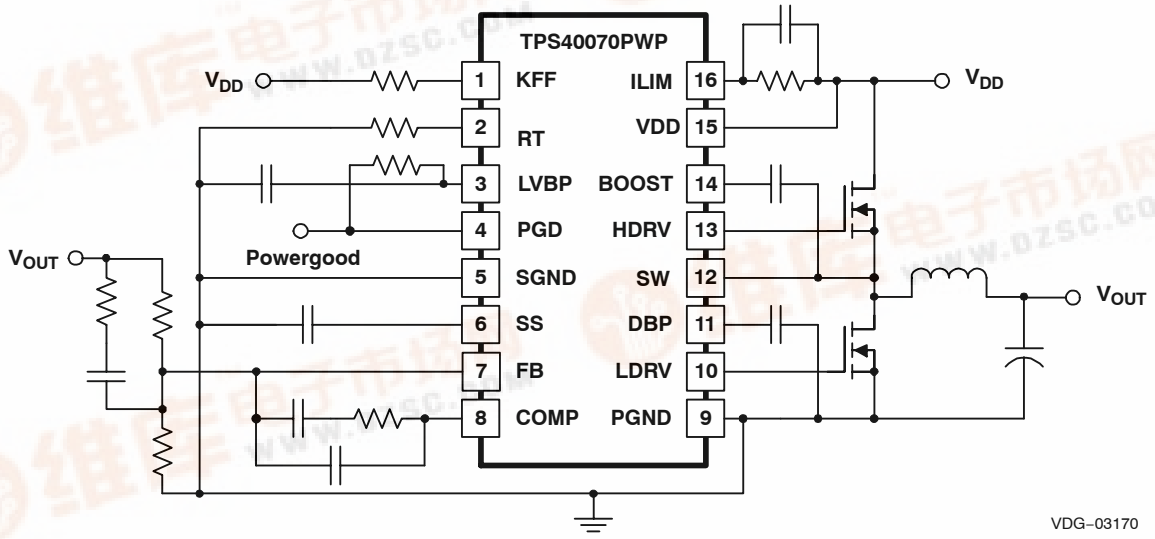
DESCRIPTION

The TPS4007x is a mid voltage, wide input (4.5 V to 28 V), synchronous, step-down converter.

The TPS4007x offers design flexibility with a variety of user programmable functions, including; soft-start, UVLO, operating frequency, voltage feed-forward and high-side FET sensed short circuit protection.

The TPS4007x incorporates MOSFET gate drivers for external N-channel high-side and synchronous rectifier (SR) MOSFETs. Gate drive logic incorporates predictive anti-cross conduction circuitry to prevent simultaneous high-side and synchronous rectifier conduction, while minimizing to eliminating current flow in the body diode of the SR FET. The TPS40071 allows the supply output to sink current at all times. The TPS40070 implements a source-only power supply.

SIMPLIFIED APPLICATION DIAGRAM



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DESCRIPTION (CONTINUED)

The TPS4007x uses voltage feed-forward control techniques to provide good line regulation over a wide-input voltage range, and fast response to input line transients with near constant gain with input variation to ease loop compensation. The externally programmable short circuit protection provides fault current limiting, as well as hiccup mode operation for thermal protection in the presence of a shorted output.The TPS4007x is packaged in a 16-pin PowerPAD package for better thermal performance at higher voltages and frequencies. See SLMA002 for information on board layout for the PowerPAD package. The pcb pad that the PowerPAD solders to should be connected to GND. Due to the die attach method, the PowerPAD itself cannot be used as the device ground connection. The two device grounds must be connected as well.

ORDERING INFORMATION

T_A	APPLICATION	PACKAGE	PART NUMBER
40°C to 85°C	SOURCE ONLY (1)	Plastic HTSSOP (PWP) (2)	TPS40070PWP
	SOURCE/SINK (1)	Plastic HTSSOP (PWP) (2)	TPS40071PWP

(1) See *Application Information* section and Table 1.
(2) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS40070PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

			TPS40070 TPS40071	UNIT
V_{DD}	Input voltage range	VDD, ILIM	30	V
		COMP, FB, KFF, PGD, LVBP	–0.3 to 6	
		SW	–0.3 to 40	
		SW, transient < 50 ns	–2.5	
V_{OUT}	Output voltage range	COMP, KFF, RT, SS	–0.3 to 6	
		VBOOST	50	
		DBP	10.5	
		LVBP	6	
I_{OUT}	Output current source	LDRV, HDRV	1.5	A
I_{OUT}	Output current sink	LDRV, HDRV	2.0	
		KFF	10	
	Output current	RT	1	mA
		LVBP	1.5	
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature		–55 to 150	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Input voltage	4.5		28	V
T_A	Operating free-air temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 μA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

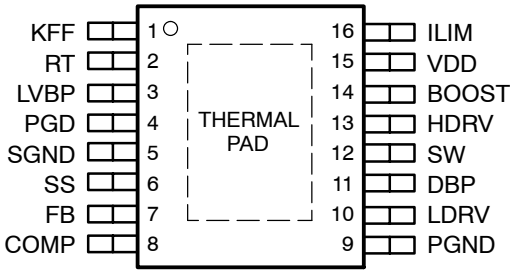
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{DD}	Input voltage range, VIN		4.5		28	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching		2.5	3.5	mA
LVBP						
V_{LVBP}	Output voltage	$T_A = T_J$ = 25°C	3.9	4.2	4.5	V
OSCILLATOR/RAMP GENERATOR (1)						
f_{OSC}	Accuracy		450	500	550	kHz
V_{RAMP}	PWM ramp voltage (2)	V_{PEAK}-V_{VAL}		2.0		V
V_{RT}	RT voltage		2.23	2.40	2.58	V
t_{ON}	Minimum output pulse time (2)	C_{HDRV} = 0 nF			250	ns
	Maximum duty cycle	V_{FB} = 0 V, 100 kHz ≤ f_{SW} ≤ 500 kHz	84%		93%	
		V_{FB} = 0 V, f_{SW} = 1 MHz	76%		93%	
V_{KFF}	Feed-forward voltage		0.35	0.40	0.45	V
I_{KFF}	Feed-forward current operating range (2)		20		1100	μA
SOFT START						
I_{SS}	Charge current		7	12	17	μA
t_{DSCH}	Discharge time	C_{SS} = 3.9 nF	25		75	μs
t_{SS}	Soft-start time	C_{SS} = 3.9 nF, V_{SS} rising from 0.7 V to 1.6 V	210	290	500	
	Command zero output voltage (1)		300			mV
DBP						
V_{DBP}	Output voltage	V_{DD} > 10 V	7	8	9	V
		V_{DD} = 4.5 V, I_{OUT} = 25 mA	4.0	4.3		
ERROR AMPLIFIER						
V_{FB}	Feedback regulation voltage total variation	$T_A = T_J$ = 25°C	0.698	0.700	0.704	V
		0°C ≤ T_A ≤ 85°C	0.690	0.700	0.707	
		40°C ≤ T_A ≤ 85°C	0.690	0.700	0.715	
V_{SS}	Soft-start offset from VSS	Offset from V_{SS} to error amplifier		1		
G_{BW}	Gain bandwidth (1)		5	10		MHz
A_{VOL}	Open loop gain		50			dB
I_{SRC}	Output source current		2.5	4.5		mA
I_{SINK}	Output sink current		2.5	6		
I_{BIAS}	Input bias current	V_{FB} = 0.7 V	–250		0	nA

(1) For zero output voltage only. Does not assure lack of activity on HDRV or LDRV.
(2) Ensured by design. Not production tested.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SHORT CIRCUIT CURRENT PROTECTION						
I_{ILIM}	Current sink into current limit		80	105	125	μA
$V_{ILIM(ofst)}$	Current limit offset voltage	V_{ILIM} = 11.5 V, (V_{SW} - V_{ILIM}) V_{DD} = 12 V	–75	–50	–30	mV
t_{HSC}	Minimum HDRV pulse width	During short circuit		135	225	ns
	Propagation delay to output (3)			50		ns
t_{BLANK}	Blanking time (3)			50		ns
t_{OFF}	Off time during a fault (SS cycle times)			7		cycles
V_{SW}	Switching level to end precondition (3)	(V_{DD} - V_{SW})		2		V
t_{PC}	Precondition time (3)				100	ns
V_{ILIM}	Current limit precondition voltage threshold (3)			6.8		V
OUTPUT DRIVERS						
t_{HFALL}	High-side driver fall time (3)	C_{HDRV} = 2200 pF, (HDRV - SW)		36		ns
t_{HRISE}	High-side driver rise time (3)			48		
t_{HFALL}	High-side driver fall time (3)	C_{HDRV} = 2200 pF, (HDRV - SW) V_{DD} = 4.5 V, 0.2 V ≤ V_{SS}≤ 4 V		72		ns
t_{HRISE}	High-side driver rise time (3)			96		
t_{LFALL}	Low-side driver fall time (3)	C_{LDRV} = 2200 pF		24		ns
t_{LRISE}	Low-side driver rise time (3)			48		
t_{LFALL}	Low-side driver fall time (3)	C_{LDRV} = 2200 pF, V_{DD}= 4.5 V, 0.2 V ≤ V_{SS}≤ 4 V		48		ns
t_{LRISE}	Low-side driver rise time (3)			96		
V_{OH}	High-level output voltage, HDRV	I_{HDRV} = -0.01 A, (V_{BOOST}- V_{HDRV})		0.7	1.0	V
		I_{HDRV} = -0.1 A, (V_{BOOST} - V_{HDRV})		0.95	1.30	
V_{OL}	Low-level output voltage, HDRV	(V_{HDRV} - V_{SW}), I_{HDRV} = 0.01A		0.06	0.10	V
		(V_{HDRV} - V_{SW}), I_{HDRV} = 0.1 A		0.65	1.0	
V_{OH}	High-level output voltage, LDRV	(V_{DBP} - V_{LDRV}), I_{LDRV}= -0.01A		0.65	1.00	V
		(V_{DBP} - V_{LDRV}), I_{LDRV} = -0.1 A		0.875	1.200	
V_{OL}	Low-level output voltage, LDRV	I_{LDRV} = 0.01 A		0.03	0.05	V
		I_{LDRV} = 0.1 A		0.3	0.5	
ZERO CURRENT DETECTION						
I_{ZERO}	Zero current threshold, TPS40070		–5	0	5	mV
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{DD} = 12 V	15.2	17.0		V
UVLO						
V_{UVLO}	Programmable UVLO threshold voltage	R_{KFF} = 90.9 kΩ, turn-on, V_{DD} rising	6.2	7.2	8.2	V
	Programmable UVLO hysteresis	R_{KFF} = 90.9 kΩ	1.10	1.55	2.00	
	Fixed UVLO threshold voltage	Turn-on, V_{DD} rising	4.15	4.30	4.45	
	Fixed UVLO hysteresis		275	365		mV
POWER GOOD						
V_{PG}	Powergood voltage	I_{PG} = 1 mA		370	500	mV
V_{OH}	High-level output voltage, FB			770		
V_{OL}	Low-level output voltage, FB			630		
THERMAL SHUTDOWN						
	Shutdown temperature threshold (3)			165		°C
	Hysteresis (3)			15		

(3) Ensured by design. Not production tested.

PWP PACKAGE(1)(2)
(TOP VIEW)



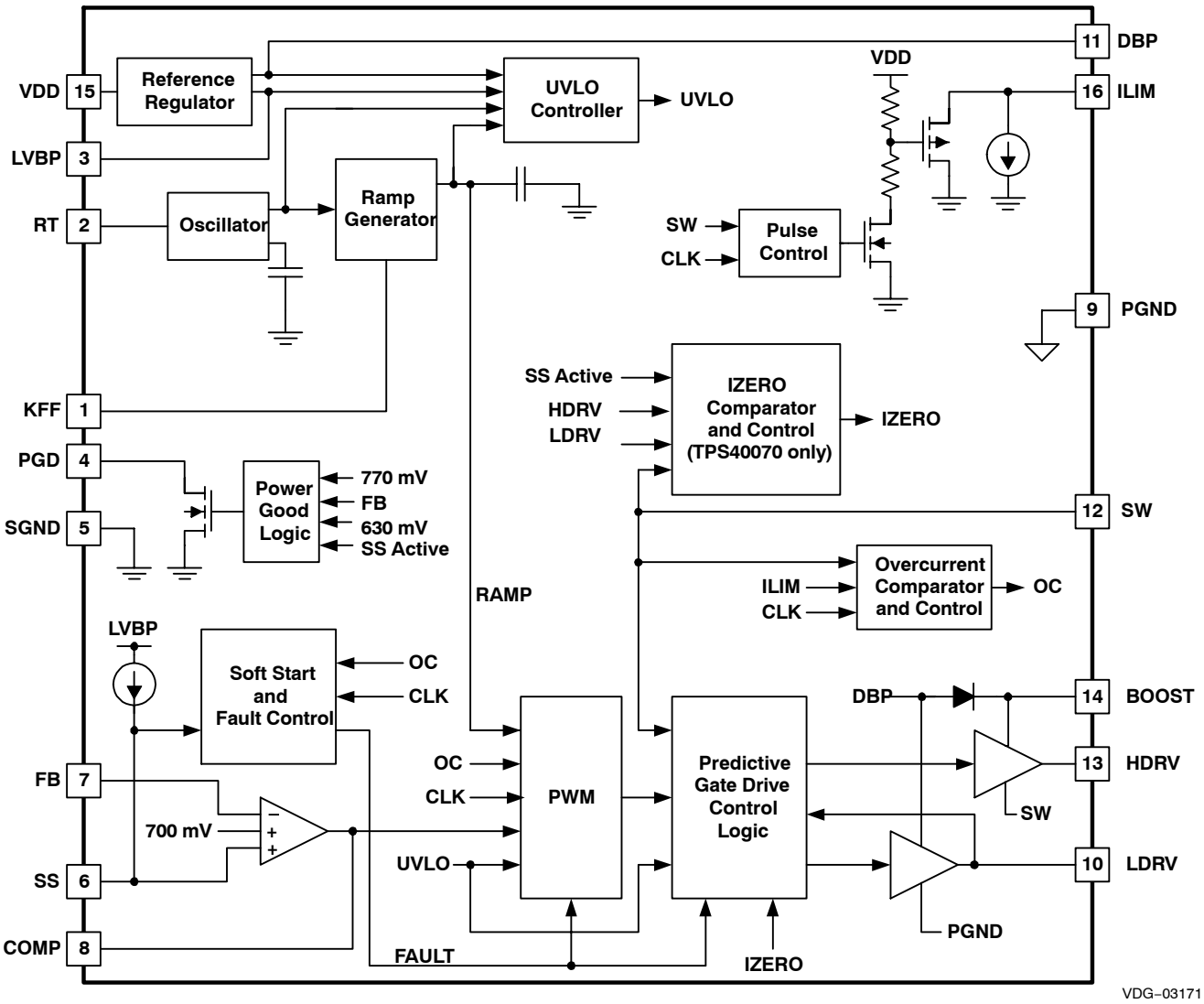
(1) For more information on the PWP package, refer to TI Technical Brief (SLMA002).

(2) PowerPAD™ heat slug must be connected to SGND (pin 5) or electrically isolated from all other pins.

Table 1. Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOST	14	I	Gate drive voltage for the high-side N-channel MOSFET. The BOOST voltage is 8 V greater than the input voltage. A capacitor should be connected from this pin to the SW pin.
COMP	8	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the FB pin to compensate the overall loop. The comp pin is internally clamped to 3.4 V.
DBP	11	O	8-V reference used for the gate drive of the N-channel synchronous rectifier. This pin should be bypassed to ground with a 1.0-μF ceramic capacitor.
FB	7	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage, 0.7 V.
HDRV	13	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	16	I	Short circuit protection programming pin. This pin is used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VDD. The voltage on this pin is compared to the voltage drop (V_{VDD} -V_{SW}) across the high side N-channel MOSFET during conduction. Just prior to the beginning of a switching cycle this pin is pulled to approximately VDD/2 and released when SW is within 2 V of V_{DD} or after a timeout (the precondition time) - whichever occurs first. Placing a capacitor across the resistor from ILIM to VDD allows the ILIM threshold to decrease during the switch on time, effectively programming the ILIM blanking time. See applications information.
KFF	1	I	A resistor is connected from this pin to VIN programs the amount of feed-forward voltage. The current fed into this pin is internally divided by 25 and used to control the slope of the PWM ramp and program undervoltage lockout. Nominal voltage at this pin is maintained at 400 mV.
LDRV	10	O	Gate drive for the N-channel synchronous rectifier. This pin switches from DBP (MOSFET on) to ground (MOSFET off).
LVBP	3	O	4.2-V reference used for internal device logic only. This pin should be bypassed by a 0.1-μF ceramic capacitor. External loads less than 1 mA and electrically quiet may be applied.
PGD	4	O	This is an open drain output that pulls to ground when soft start is active, or when the FB pin is outside a ±10% band around VREF.
PGND	9		Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
SGND	5		Signal ground reference for the device.
SS	6	I	Soft-start programming pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 10 μA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. The voltage at this error amplifier input is approximately 1 V less that that on the SS pin. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin reaches the internal reference voltage of 1 V plus the internal reference voltage of 0.7 V. If SS is below the 1-V offset voltage to the error amplifier. The resulting output voltage is zero. Also provides timing for fault recovery attempts.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing and for zero current sensing as well.
VDD	15	I	Supply voltage for the device.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The TPS40070 family of parts allows the user to construct synchronous voltage-mode buck converters with inputs ranging from 4.5 V to 28 V and outputs as low as 700 mV. Predictive gate drive circuitry optimizes switching delays for increased efficiency and improved converter output power capability. Voltage feed-forward is employed to ease loop compensation and provide better line transient response.

A converter based on the TPS40070 operates as a single quadrant (source only) converter at all times. When the rectifier FET is on and the controller senses that current is near zero in the inductor, the rectifier FET is turned off, preventing the buildup of negative or reverse current in the inductor. This feature prevents the converter from pulling energy from its output and forcing that energy onto its input.

Converters based on the TPS40071 operates as a two quadrant converter all the time (source and sink current). This is the controller of choice for most applications.

MINIMUM PULSE WIDTH

The TPS4007x devices have limitations on the minimum pulse width that can be used to design a converter. Reliable operation is guaranteed for nominal pulse widths of 250 ns and above. This places some restrictions on the conversion ratio that can be achieved at a given switching frequency. Figure 1 shows minimum output voltage for a given input voltage and frequency.

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS4007x has independent clock oscillator and PWM ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. Connecting a single resistor from RT to ground sets the switching frequency of the clock oscillator. The clock frequency is related to R_T by:

$$R_T = \left(\frac{1}{f_{SW}(\text{kHz}) \times 17.82 \times 10^{-6}} - 23 \right) \text{k}\Omega \tag{1}$$

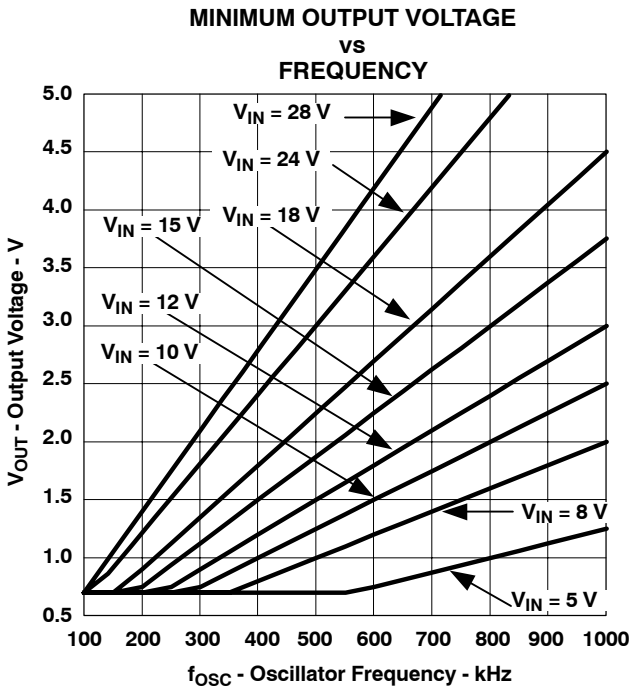


Figure 1.

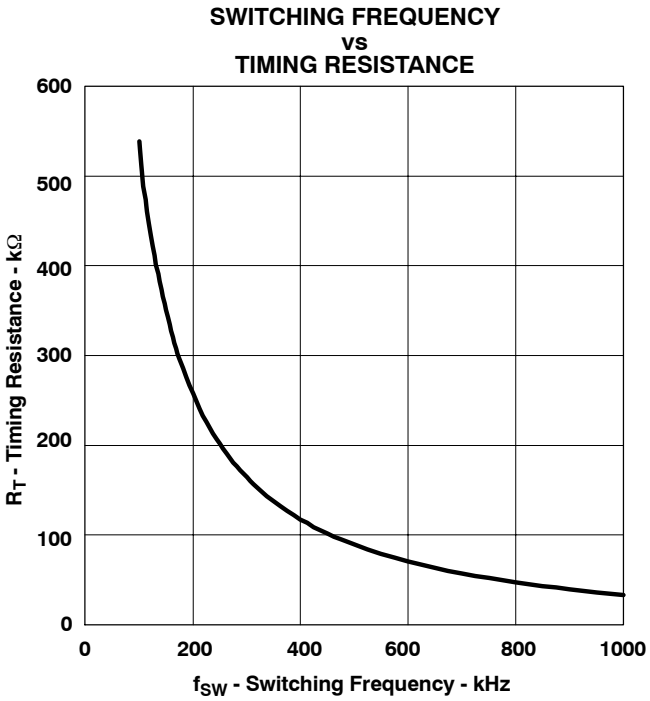


Figure 2.

APPLICATION INFORMATION (continued)

PROGRAMMING THE RAMP GENERATOR CIRCUIT AND UVLO

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations since the PWM does not have to wait for loop delays before changing the duty cycle. (See Figure 8).

The PWM ramp must reach approximately 1 V in amplitude during a clock cycle, or the PWM is not allowed to start. The PWM ramp time is programmed via a single resistor (R_{KFF}) connected from KFF VDD. R_{KFF} , V_{START} and R_T are related by (approximately):

$$V_{UVLO(on)} = 7.6 \times \frac{R_{KFF}}{R_T} + 0.4 \quad (2)$$

where

- $V_{UVLO(on)}$ is in volts
- resistors use the same units

This yields typical numbers for the programmed startup voltage. The minimum and maximum values may vary up ±15% from this number. Figure 4 through Figure 6 show the typical relationship of $V_{UVLO(on)}$, $V_{UVLO(off)}$ and R_{KFF} at three common frequencies.

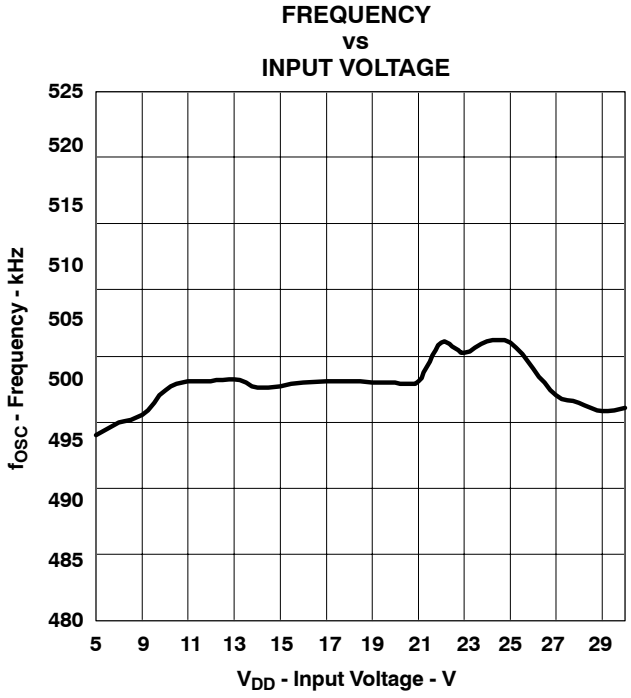


Figure 3.

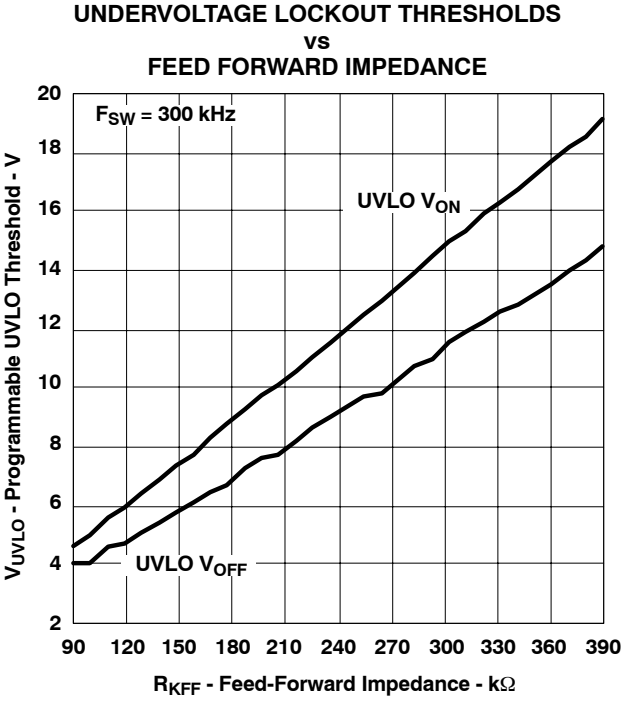


Figure 4.

APPLICATION INFORMATION (continued)

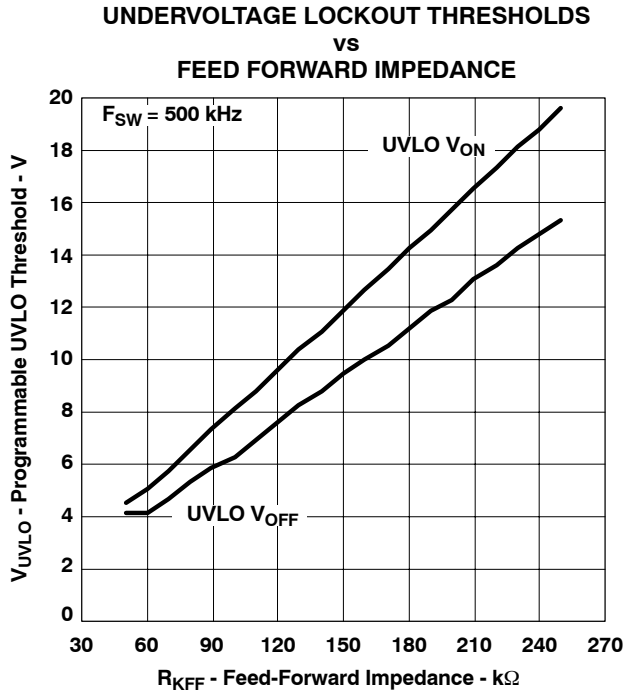


Figure 5.

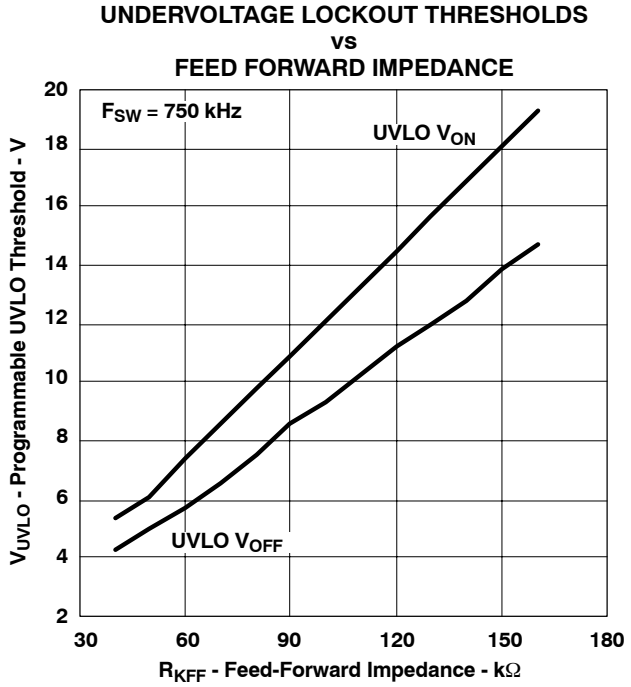


Figure 6.

The programmable UVLO circuit incorporates 20% hysteresis from the start voltage to the shutdown voltage. For example, if the startup voltage is programmed to be 10 V, the controller starts when V_{DD} reaches 10 V and shuts down when V_{DD} falls below 8 V. The maximum duty cycle begins to decrease as the input voltage rises to twice the startup voltage. Below this point, the maximum duty cycle is as specified in the electrical table. Note that with this scheme, the theoretical maximum output voltage that the converter can produce is approximately two times the programmed startup voltage. For design, set the programmed startup voltage equal to or greater than the desired output voltage divided by maximum duty cycle (85% for frequencies 500 kHz and below). For example, a 5-V output converter should not have a programmed startup voltage below 5.9 V. Figure 7 shows the theoretical maximum duty cycle (typical) for various programmed startup voltages

At startup, LDRV may pulse high when V_{DD} is in the range of 1 V to 1.25 V and V_{DD} is rising extremely slowly. To minimize these effects, the ramp rate of V_{DD} at startup should be greater than 1 V/ms.

APPLICATION INFORMATION (continued)

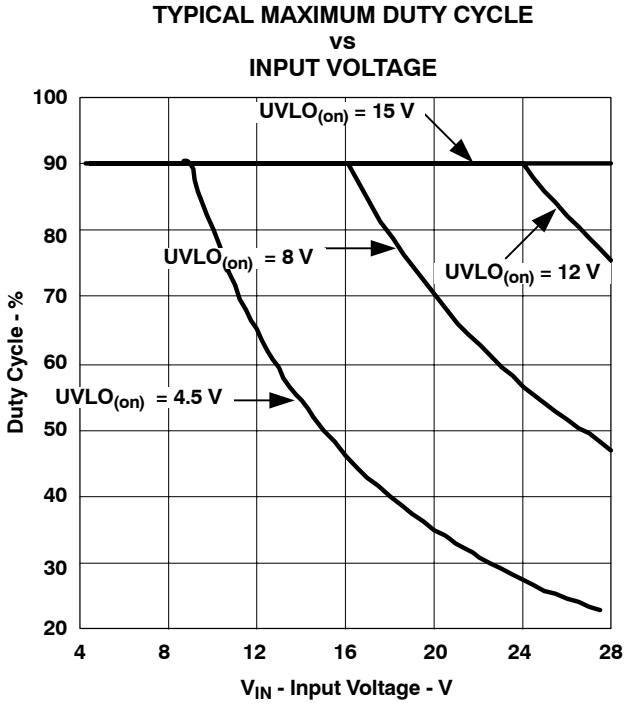


Figure 7.

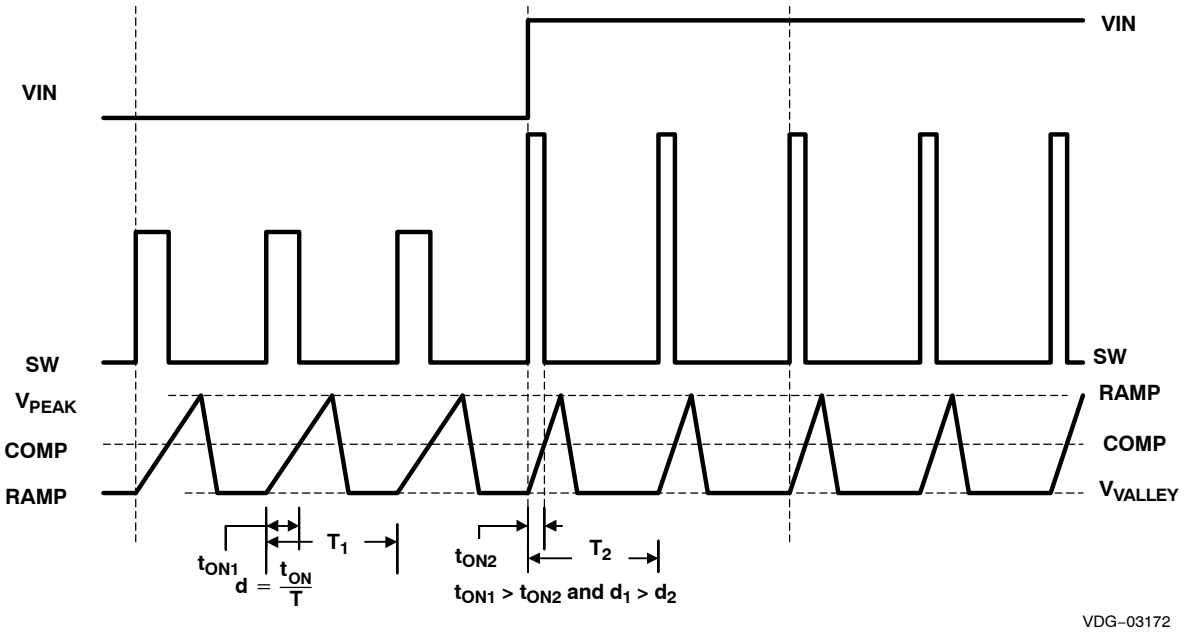


Figure 8. Voltage Feed-Forward and PWM Duty Cycle Waveforms

PROGRAMMING SOFT START

TPS4007x uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by connecting an external capacitor (C_{SS}) from the SS pin to GND. This capacitor is charged by a fixed current, generating a ramp signal. The voltage on SS is level shifted down approximately 1 V and fed into a separate non-inverting input to the error amplifier. The loop is closed on the lower of the level shifted SS voltage or the 700-mV internal reference voltage. Once the level shifted SS voltage rises above the internal reference voltage, output voltage regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage the soft-start time should be greater than the L-C_{OUT} time constant or:

$$t_{START} \geq 2\pi \times \sqrt{L \times C_{OUT}} \quad \text{(seconds)} \tag{3}$$

Please note: There is a direct correlation between t_{START} and the input current required during start-up. The lower t_{START} is, the higher the input current required during start-up since the output capacitance must be charged faster. For a desired soft-start time, the soft-start capacitance, C_{SS}, can be found from:

$$C_{SS} = \frac{12 \times 10^{-6}}{0.7\ \text{V}} \times t_{START} \quad \text{(Farads)} \tag{4}$$

PROGRAMMING SHORT CIRCUIT PROTECTION

The TPS4007x uses a two-tier approach for short circuit protection. The first tier is a pulse-by-pulse protection scheme. Short circuit protection is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when its gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor (R_{ILIM}) connected from V_{DD} to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated. This is illustrated in Figure 9.

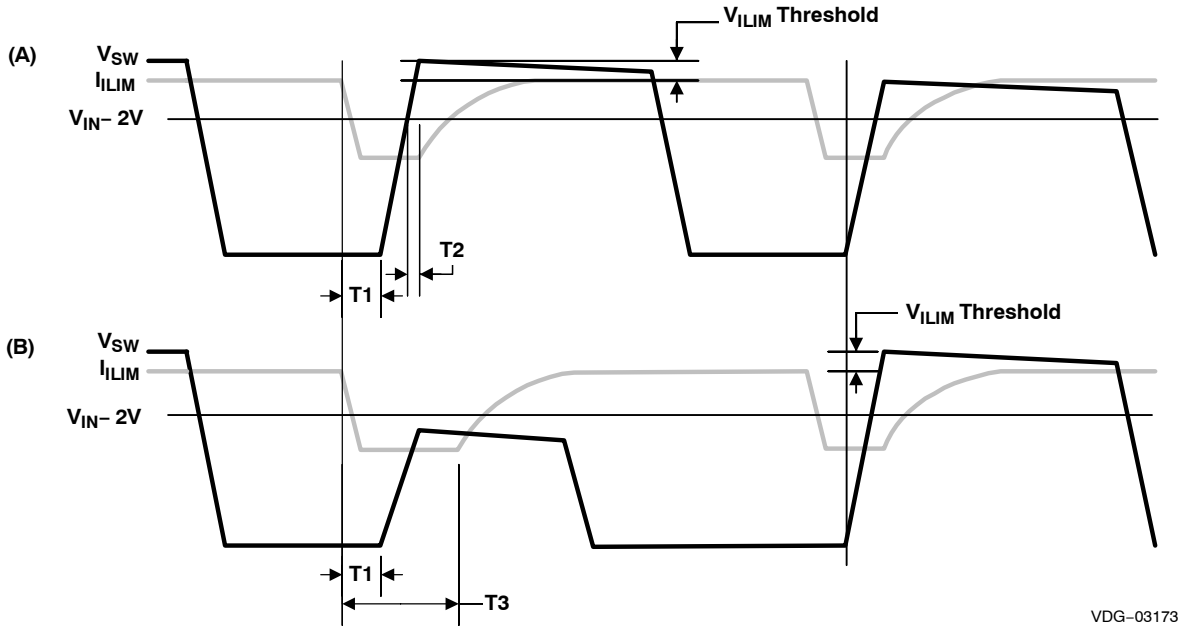


Figure 9. Voltage Feed-Forward and PWM Duty Cycle Waveforms

In addition, just prior to the high-side MOSFET turning on, the ILIM pin is pulled down to approximately half of VDD. The ILIM pin is allowed to return to its nominal value after one of two events occur. If the SW node rises to within approximately 2 V of V_{DD}, the device allows ILIM to go back to its nominal value. This is illustrated in Figure 9(A). T1 is the delay time from the internal PWM signal being asserted and the rise of SW. This includes a driver delay of 50 ns typical. T2 is the reaction time of the sensing circuit that allows ILIM to start to return to its nominal value, typically 20ns. The second event that can cause ILIM to return to its nominal value is for an internal timeout to expire. This is illustrated in Figure 9(B) as T3. Here SW never rises to V_{DD}-2 V, for whatever reason, and the internal timer times out, releasing the ILIM pin.

Prior to ILIM starting back to its nominal value, overcurrent sensing is not enabled. In normal operation, this ensures that the SW node is at a higher voltage than ILIM when overcurrent sensing starts, avoiding false trips while allowing for a quicker blanking delay than would ordinarily be possible. Placing a capacitor across R_{ILIM} sets an exponential approach to the normal voltage at the ILIM pin. This exponential decay of the overcurrent threshold can be used to compensate for ringing on the SW node after its rising edge and to help compensate for slower turn-on FETs. Choosing the proper capacitance requires care. If the capacitance is too large, the voltage at ILIM does not approach the desired overcurrent level quickly enough, resulting in an apparent shift in overcurrent threshold as pulse width changes.

Also, the comparator that uses ILIM and SW to determine if an overcurrent condition exists has a clamp on its SW input. This clamp makes the SW node never appear to fall more than 1.4 V (approximately, could be as much as 2 V at -40°C) below V_{DD}. When ILIM is more than 1.4 V below V_{DD}, the overcurrent circuit is effectively disabled. As a general rule, it is best to make the time constant of the R-C at the ILIM pin 0.2 times or less of the nominal pulse width of the converter as shown in see Equation 9.

The second tier protection incorporates a fault counter. The fault counter is incremented on each cycle with an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7) a fault condition is declared by the controller. When this happens, the outputs are placed in a state defined in Table 2. Seven soft-start cycles are initiated (without activity on the HDRV and LDRV outputs) and the PWM is disabled during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero the PWM is re-enabled and the controller attempts to restart. If the fault has been removed the output starts up normally. If the output is still present the counter counts seven overcurrent pulses and re-enter the second tier fault mode. Refer to Figure 10 for typical fault protection waveforms.

The minimum short circuit limit setpoint (ILIM) depends on t_{START}, C_{OUT}, V_{OUT}, and the load current at turn-on (I_{LOAD}).

$$I_{ILIM} > \frac{C_{OUT} \times V_{OUT}}{t_{START}} + I_{LOAD} \text{ (A)} \tag{5}$$

The short circuit limit programming resistor (R_{ILIM}) is calculated from:

$$R_{ILIM} = \frac{I_{SCP} \times R_{DS(onMAX)} + V_{ILIM\ (offset)}}{I_{ILIM}} \ \Omega \tag{6}$$

where

- I_{ILIM} is the current into the ILIM pin (110 μA typical)
- $V_{ILIM(offset)}$ is the offset voltage of the ILIM comparator (-50 mV typical)
- I_{SCP} is the short-circuit protection current

To find the range of the overcurrent values use the following equations.

$$I_{SCP(max)} = \frac{I_{ILIM(max)} \times R_{ILIM} + 75\text{ mV}}{R_{DS(onMIN)}} \ \Omega \tag{7}$$

$$I_{SCP(min)} = \frac{I_{ILIM(min)} \times R_{ILIM} + 30\text{ mV}}{R_{DS(onMAX)}} \ \Omega \tag{8}$$

The ILIM capacitor maximum value can be found from:

$$C_{ILIM(max)} = \frac{V_{OUT} \times 0.2}{V_{IN} \times R_{ILIM} \times f_{SW}} \text{ (Farads)} \tag{9}$$

Note that this is a recommended maximum value. If a smaller value can be used, it should be. For most applications, consider using half the maximum value above.

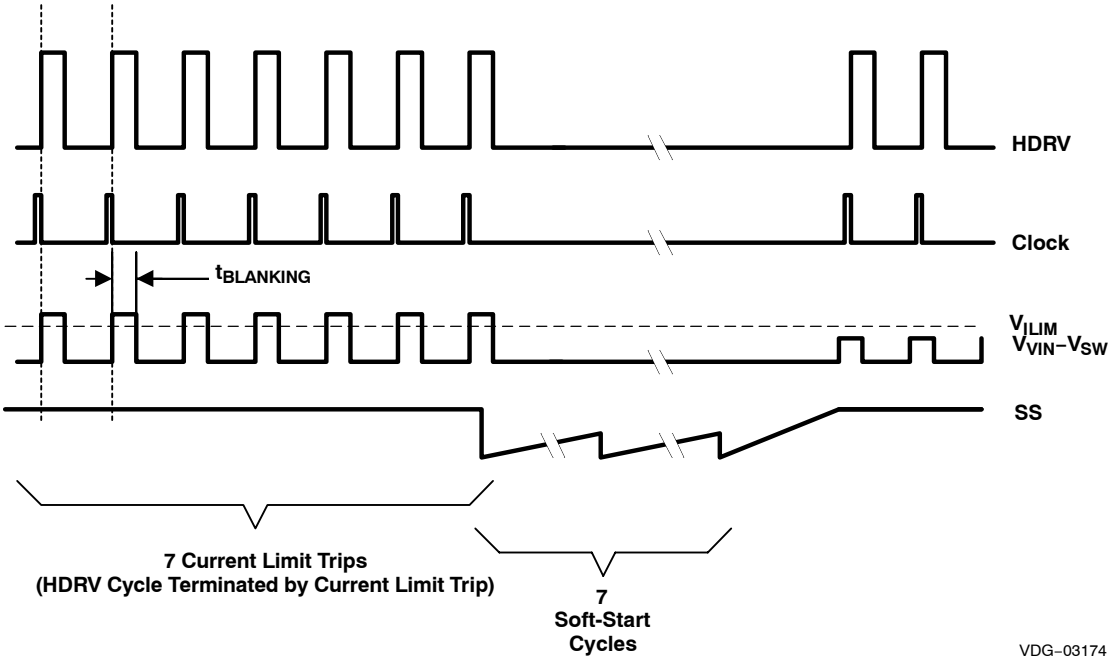


Figure 10. Typical Fault Protection Waveforms

LOOP COMPENSATION

Voltage mode buck type converters are typically compensated using Type III networks. Since the TPS4007x uses voltage feedforward control, the gain of the voltage feedforward circuit must be included in the PWM gain. The gain of the voltage feedforward circuit combined with the PWM circuit and power stage for the TPS4007x is:

$$K_{PWM} \cong V_{UVLO\ (on)} \tag{10}$$

The remainder of the loop compensation is performed as in a normal buck converter. Note that the voltage feedforward circuitry removes the input voltage term from the expression for PWM gain. PWM gain is strictly a function of the programmed startup voltage.

BOOST AND LVBP BYPASS CAPACITANCE

The BOOST capacitance provides a local, low-impedance flying source for the high-side driver. The BOOST capacitor should be a good quality, high-frequency capacitor. A capacitor with a minimum value of 100-nF is suggested.

The LVBP has to provide energy for both the synchronous MOSFET and the high-side MOSFET (via the BOOST capacitor). The suggested value for this capacitor is 1-μF ceramic, minimum.

INTERNAL REGULATORS

The internal regulators are linear regulators that provide controlled voltages for the drivers and the internal circuitry to operate from. The DBP pin is connected to a nominal 8-V regulator that provides power for the driver circuits to operate from. This regulator has two modes of operation. At V_{DD} voltages below 8.5 V ,the regulator is in a low dropout mode of operation and tries to provide as little impedance as possible from VDD to DBP. Above 10 V at V_{DD}, the regulator regulates DBP to 8 V. Between these two voltages, the regulator remains in the state it was in when V_{DD} entered this region (see Figure 11). Small amounts of current can be drawn from this pin for other circuit functions, as long as power dissipation in the controller device remains at acceptable levels and junction temperature does not exceed 125°C.

The LVBP pin is connected to another internal regulator that provides 4.2-V (nom) for the operation of low-voltage circuitry in the controller. This pin can be used for other circuit purposes, but extreme care must be taken to ensure that no extra noise is coupled onto this pin, since controller performance suffers. Current draw is not to exceed 1 mA. See Figure 12 for typical output voltage at this pin.

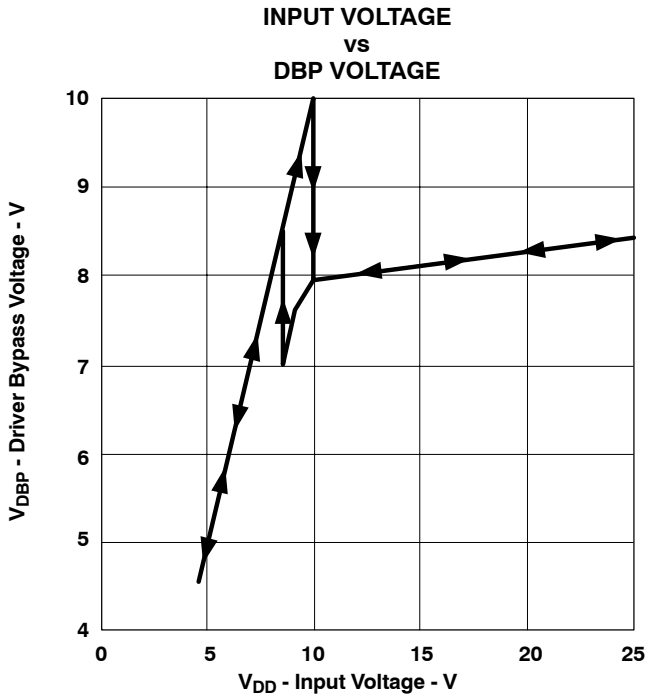


Figure 11.

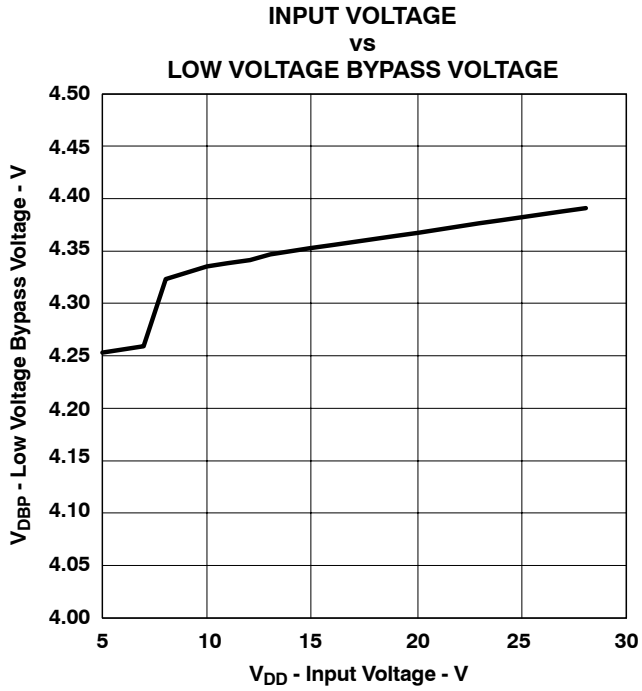


Figure 12.

TPS4007x POWER DISSIPATION

The power dissipation in the TPS4007x is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance) can be calculated from:

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad \text{(Watts/driver)} \tag{11}$$

where

- V_{DR} is the driver output voltage

And the total power dissipation in the TPS4007x, assuming the same MOSFET is selected for both the high-side and synchronous rectifier is described in Equation 12.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{12}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{13}$$

where:

- I_Q is the quiescent operating current (neglecting drivers)

The maximum power capability of the TPS4007x PowerPAD package is dependent on the layout as well as air flow. The thermal impedance from junction to air assuming 2-oz. copper trace and thermal pad with solder and no air flow is see teh application report titled*PowerPAD Thermally Enhanced Package* (SLMA002) for detailed information on PowerPAD package mounting and usage.

$$\theta_{JA} = 36.51^{\circ}C/W \tag{14}$$

The maximum allowable package power dissipation is related to ambient temperature by Equation 15.

$$P_T = \frac{T_J - T_A}{\theta_{JA}} \text{ (Watts)} \tag{15}$$

Substituting Equation 15 into Equation 14 and solving for f_{SW} yields the maximum operating frequency for the TPS4007x. The result is described in Equation 16.

$$f_{SW} = \frac{\left(\left[\frac{(T_J - T_A)}{(\theta_{JA} \times V_{DD})}\right] - I_Q\right)}{(2 \times Q_g)} \text{ (Hz)} \tag{16}$$

BOOST DIODE

The TPS4007x series has internal diodes to charge the boost capacitor connected from SW to BOOST. The drop across this diode is rather large at 1.4-V nominal at room temperature. If this drop is too large for a particular application, an external diode may be connected from DBP (anode) to BOOST (cathode). This provides significantly improved gate drive for the high side FET, especially at lower input voltages.

LOW VOLTAGE OPERATION

If the programmable UVLO is set to less than 6.5 V nominal, connect a 330-kΩ resistor across the soft-start capacitor. This eliminates a race condition inside the device that can lead to an output voltage overshoot on power down of the part. If operation is expected below -10°C ambient temperature and at less than 5-V input, it is recommended that a diode be connected from LVBP to DBP. (See Figure 15).

GROUNDING AND BOARD LAYOUT

The TPS4007x provides separate signal ground (SGND) and power ground (PGND) pins. Care should be given to proper separation of the circuit grounds. Each ground should consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (DBP), and the input capacitor should be connected to PGND plane.

Sensitive nodes such as the FB resistor divider and RT should be connected to the SGND plane. The SGND plane should only make a single point connection to the PGND plane. It is suggested that the SGND pin be tied to the copper area for the PowerPAD underneath the chip. Tie the PGND to the PowerPAD copper area as well and make the connection to the power circuit ground from the PGND pin. Reference the output voltage divider to the SGND pin.

Component placement should ensure that bypass capacitors (LVPB and DBP) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW). Failure to follow careful layout practices results in sub-optimal operation. More detailed information can be found in the TPS40071EVM User's Guide (SLUU180).

SYNCHRONOUS RECTIFIER CONTROL

Depending on which device is used the synchronous rectifier is controlled in slightly different ways. Table 2 describes the differences.

Table 2. Synchronous Rectifier MOSFET States

DEVICE	SYNCHRONOUS RECTIFIER OPERATION DURING			
	SOFT-START	NORMAL	FAULT	OVERVOLTAGE
TPS40070	Turns OFF when I_{ZERO} detected or start of next cycle	Turns Off when I_{ZERO} detected or start of next cycle	OFF	Turns OFF when I_{ZERO} detected or start of next cycle
TPS40071	Turns OFF only at start of next cycle	Turns OFF only at start of next cycle	ON	Turns OFF only at start of next cycle, if duty cycle is > 0

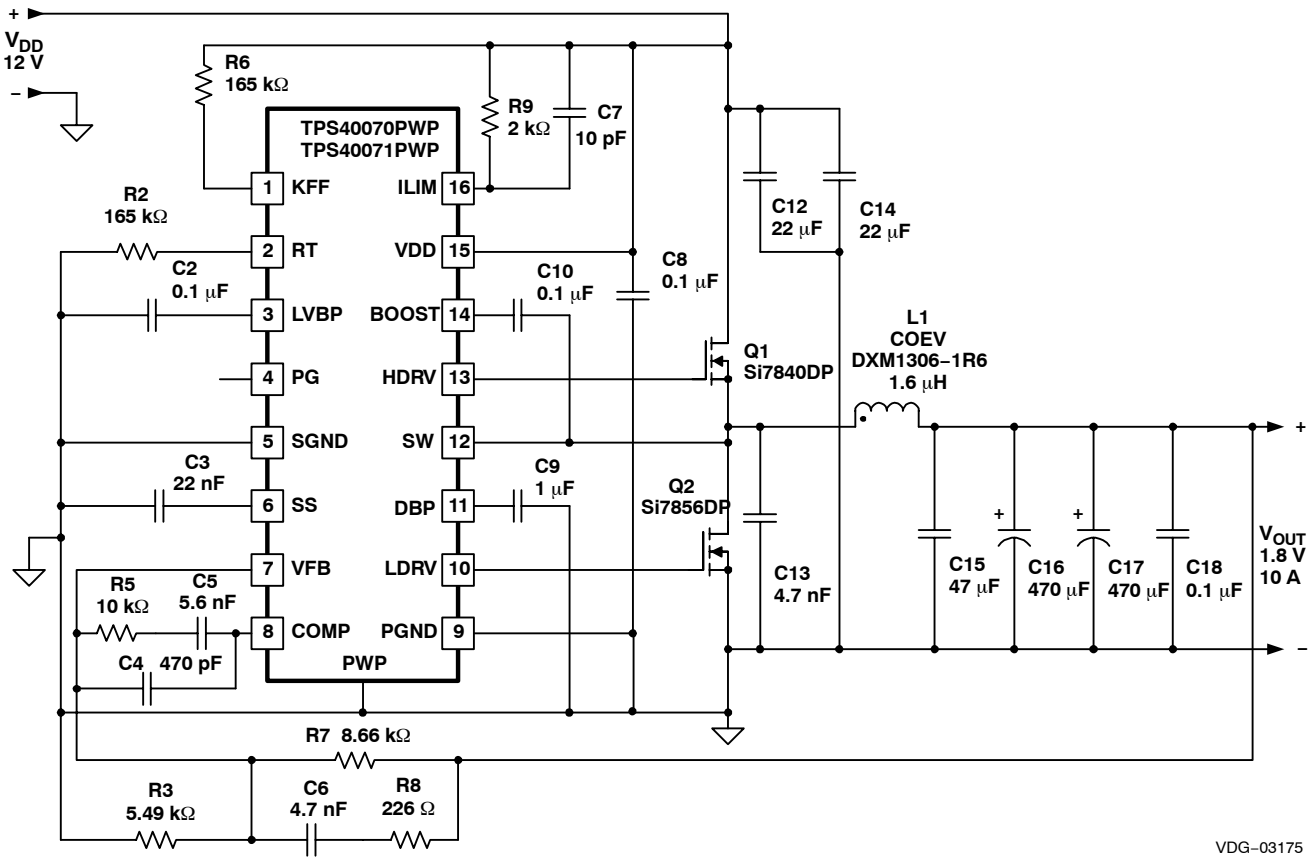


Figure 13. 300 kHz, 12 V to 1.8 V

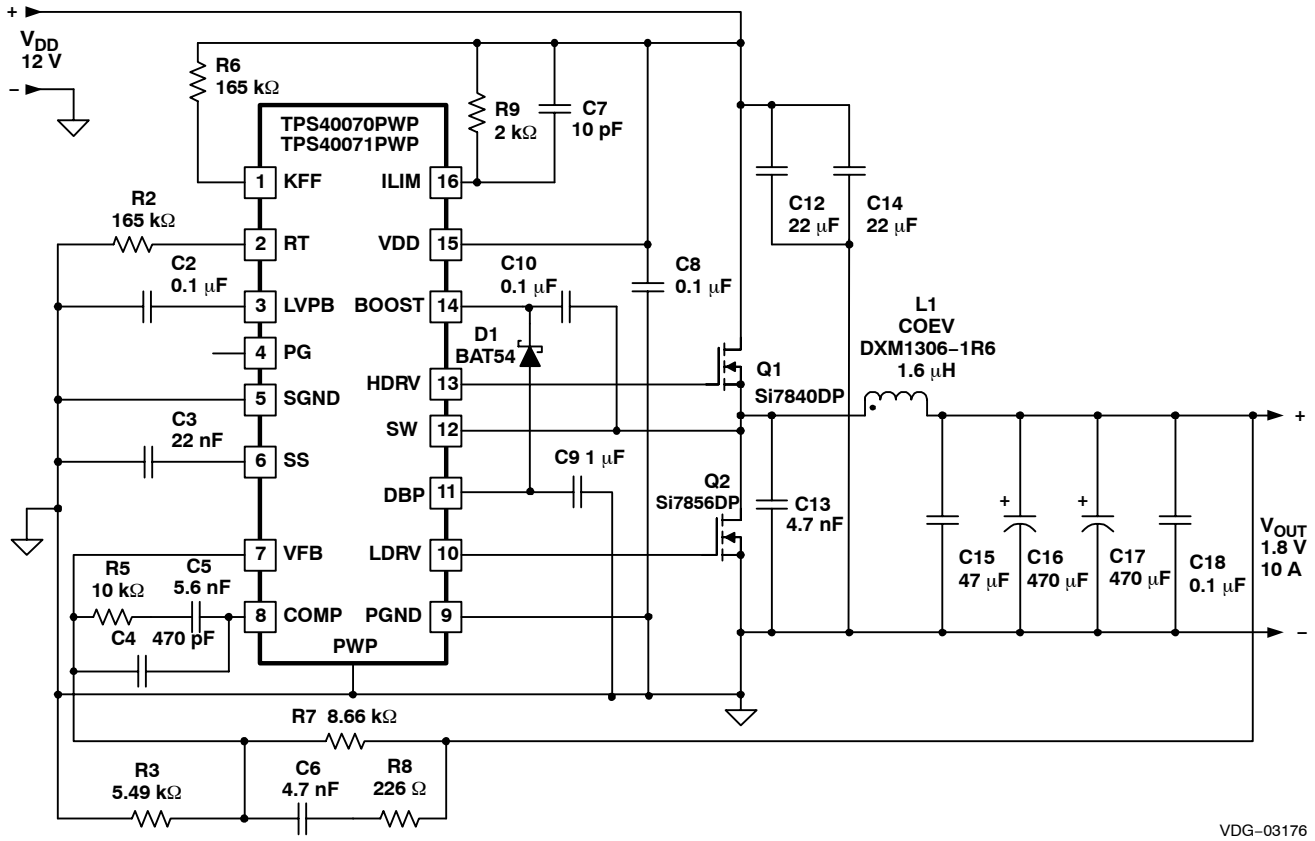


Figure 14. 300 kHz, 12 V to 1.8 V with Improved High-Side Gate Drive

See Application Information section *Boost Diodes*.

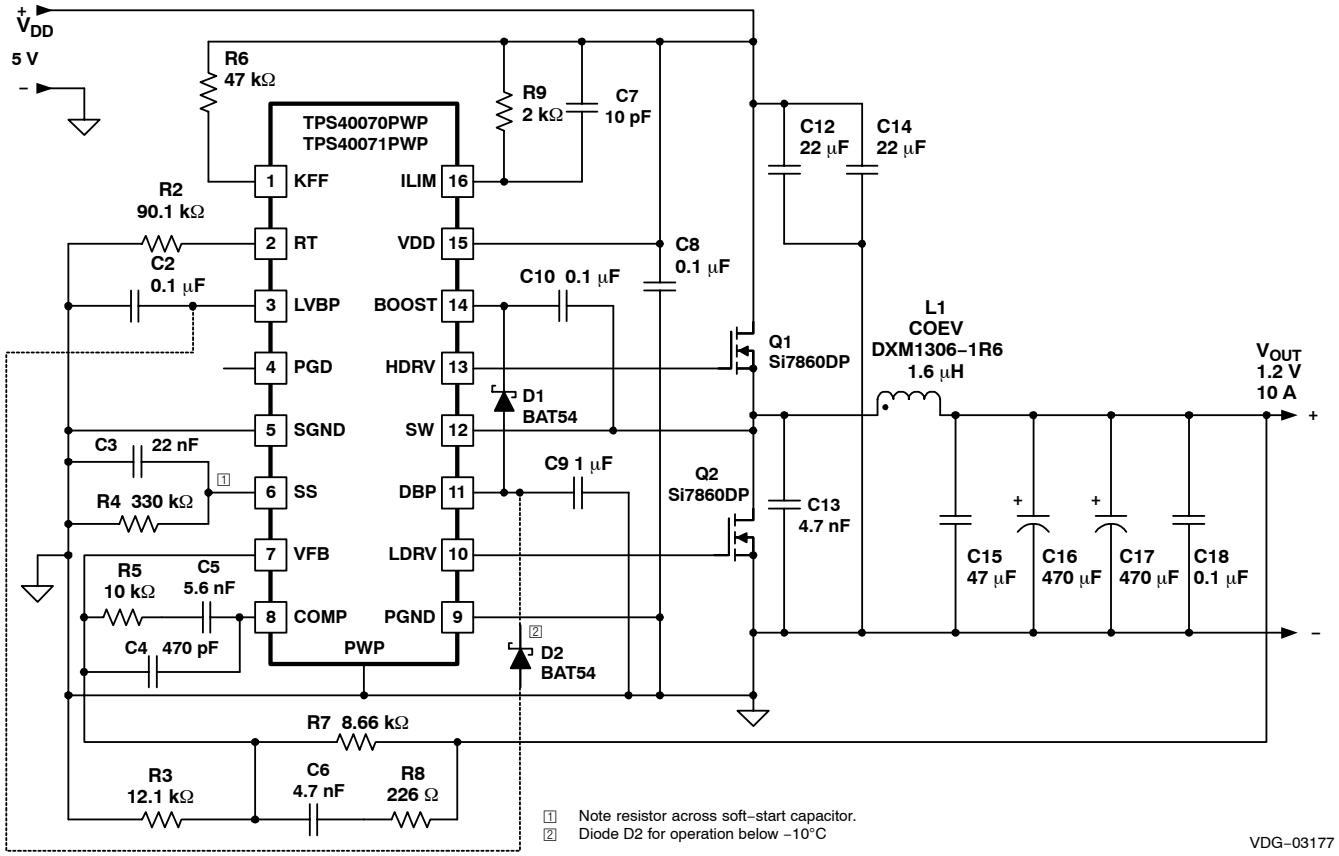
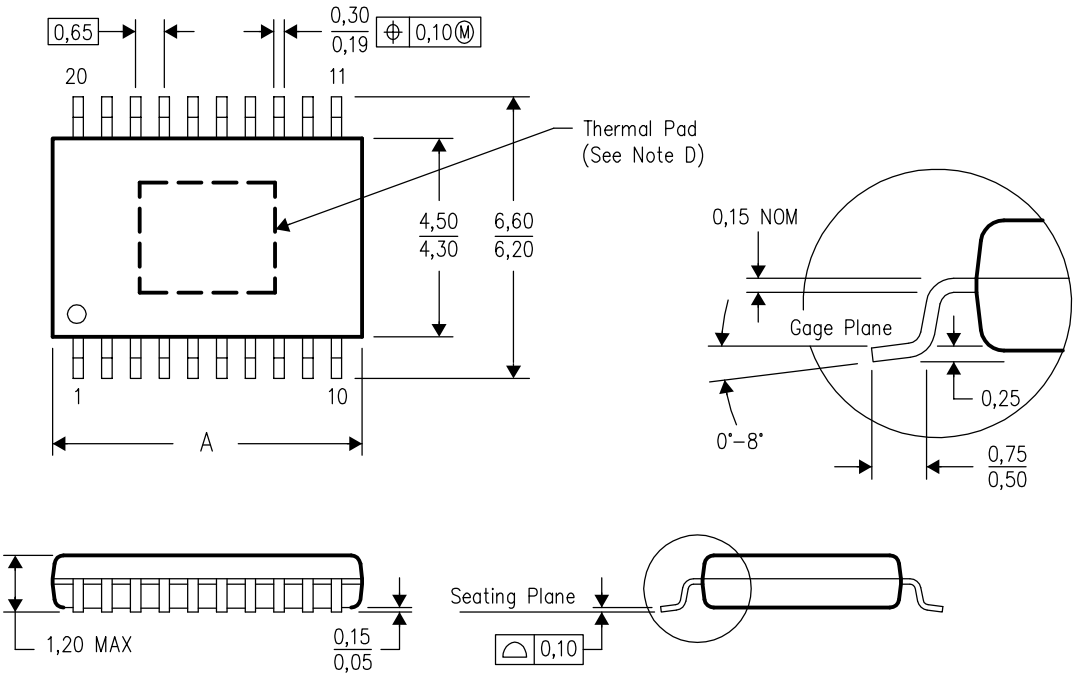


Figure 15. 500 kHz, 5 V to 1.2 V with Improved High-Side Gate Drive

See Application Information section *Boost Diodes*.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

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