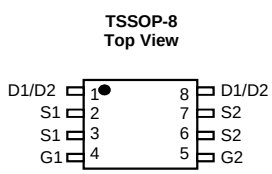
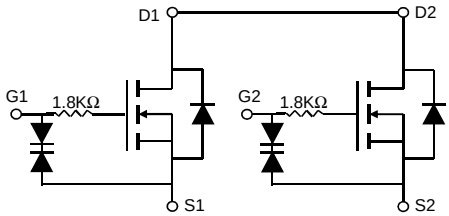
General Description

The AO8810 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi- directional load switch, facilitated by its common-drain configuration.

Features

V_{DS}	20V
I_D (at V_{GS}=4.5V)	7A
$R_{DS(ON)}$ (at V_{GS}= 4.5V)	< 20mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.0V)	< 20.5mΩ
$R_{DS(ON)}$ (at V_{GS} = 3.1V)	< 21.5mΩ
$R_{DS(ON)}$ (at V_{GS} = 2.5V)	< 23mΩ
$R_{DS(ON)}$ (at V_{GS} = 1.8V)	< 28mΩ





Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	7	A
	T_A=70℃		5.7	
Pulsed Drain Current [C]		I_{DM}	25	
Power Dissipation [B]	T_A=25℃	P_D	1.5	W
	T_A=70℃		1.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	64	83	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		89	120	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	53	70	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±8V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	0.4	0.7	1.1	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	25			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=7A		16	20	mΩ
		T_J=125℃		22	30	
		V_{GS}=4.0V, I_D=7A		16.2	20.5	mΩ
		V_{GS}=3.1V, I_D=6.5A		17	21.5	mΩ
		V_{GS}=2.5V, I_D=6.5A		18	23	mΩ
		V_{GS}=1.8V, I_D=5A		21	28	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=7A		50		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.62	1	V
I_S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz		1295		pF
C_{oss}	Output Capacitance			160		pF
C_{rss}	Reverse Transfer Capacitance			87		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.8		KΩ
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=7A		10	14	nC
Q_{gs}	Gate Source Charge			4.2		nC
Q_{gd}	Gate Drain Charge			2.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=4.5V, V_{DS}=10V, R_L=1.54Ω, R_{GEN}=3Ω		280		ns
t_r	Turn-On Rise Time			328		ns
$t_{D(off)}$	Turn-Off DelayTime			3.76		us
t_f	Turn-Off Fall Time			2.24		us
t_{rr}	Body Diode Reverse Recovery Time	I_F=7A, dI/dt=100A/μs, V_{GS}=-9V		31		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=7A, dI/dt=100A/μs, V_{GS}=-9V		6.8		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

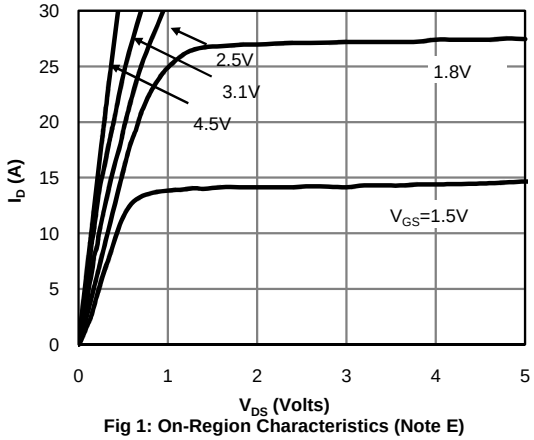


Fig 1: On-Region Characteristics (Note E)

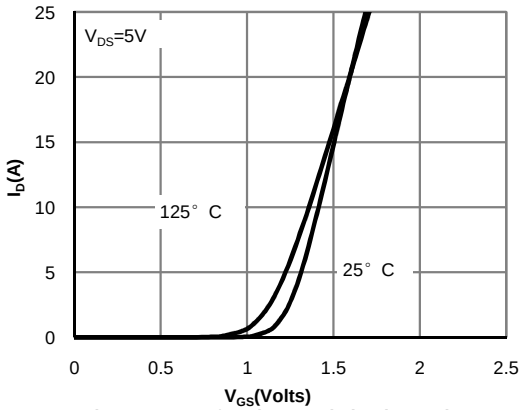


Figure 2: Transfer Characteristics (Note E)

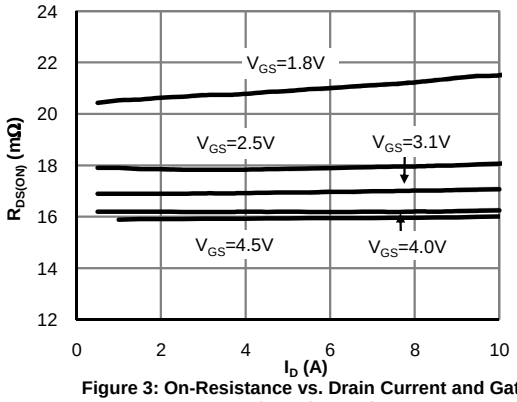


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

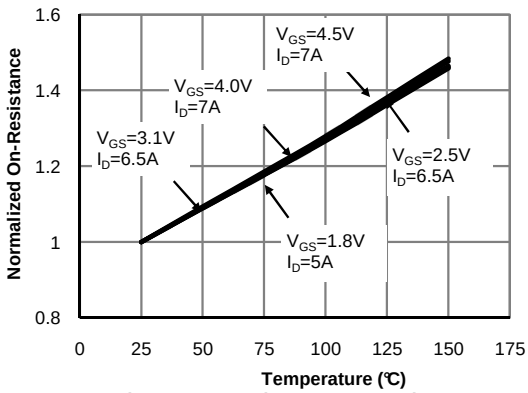


Figure 4: On-Resistance vs. Junction Temperature (Note E)

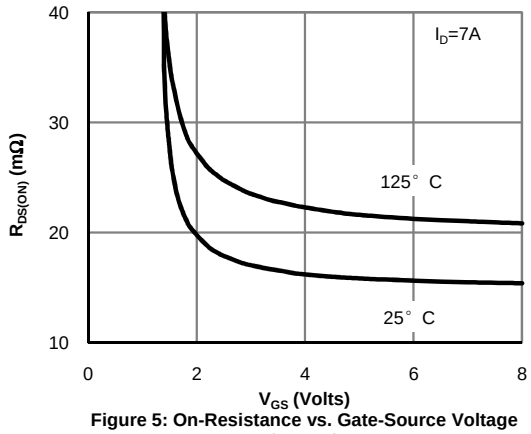


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

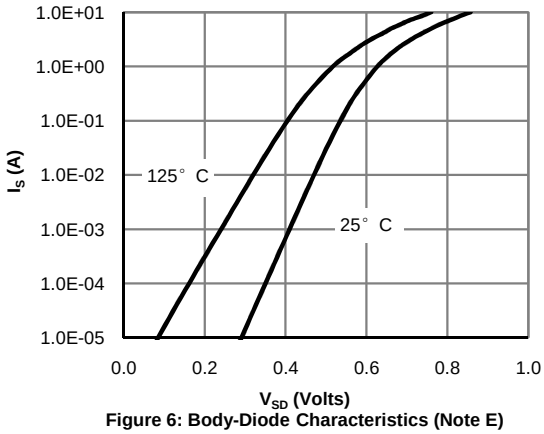


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

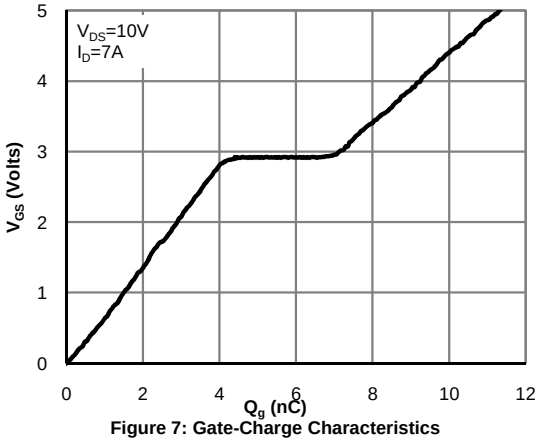


Figure 7: Gate-Charge Characteristics

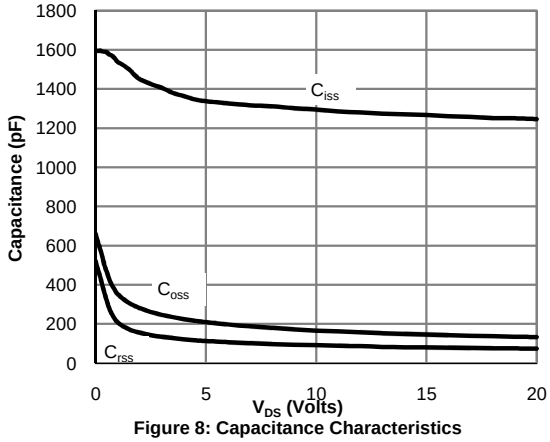


Figure 8: Capacitance Characteristics

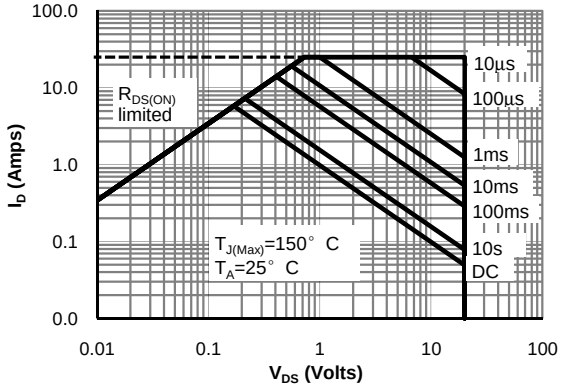


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

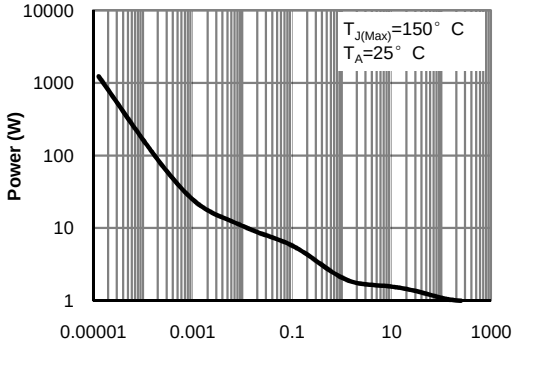


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

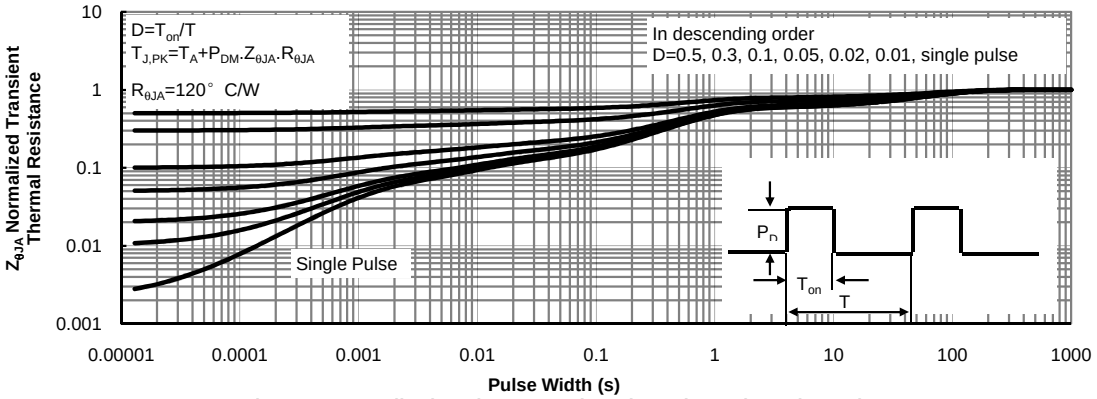
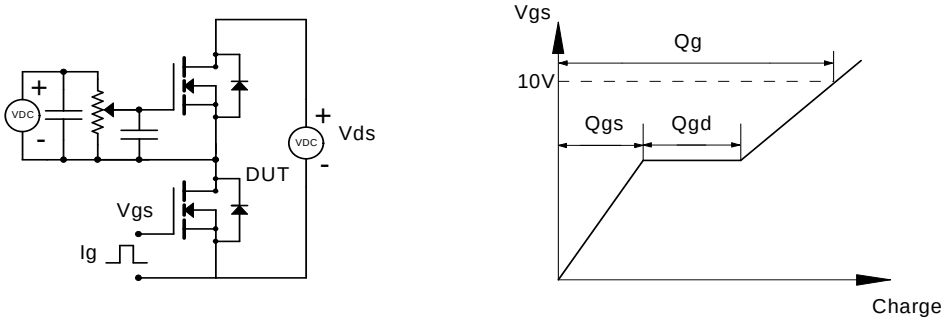
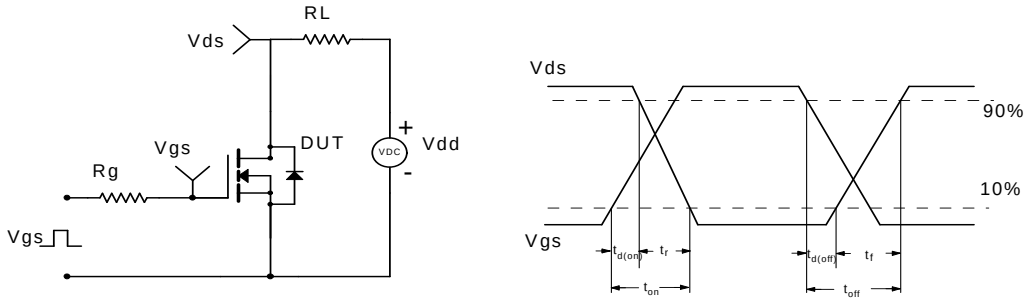


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms