freescale
飞思卡尔(深圳)功率半导体有限公司

AOL1401

P-Channel Enhancement Mode Field Effect Transistor

General Description

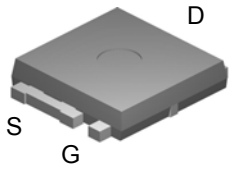
The AOL1401 uses advanced trench technology to provide excellent RDS(ON), and ultra-low low gate charge with a 25V gate rating. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

Features

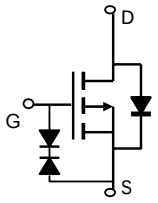
V_{DS} (V) = -38V
I_D = -85A
$R_{DS(ON)}$ < 8.5mΩ (V_{GS} = -20V)
$R_{DS(ON)}$ < 10mΩ (V_{GS} = -10V)

RoHS Compliant
Green Product

Ultra **SO-8™ Top View**



Bottom tab connected to drain



Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	-38	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current [G]	T_C=25°C	I_D	-85	A
	T_C=100°C		-62	
Pulsed Drain Current [C]		I_{DM}	-120	
Continuous Drain Current [G]	T_A=25°C	I_{DSM}	-12	
	T_A=70°C		-10	
Power Dissipation [B]	T_C=25°C	P_D	100	W
	T_C=100°C		50	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.08	W
	T_A=70°C		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	21	25	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		48	60	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	1	1.5	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-38			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-100	nA
		T_J=55°C			-500	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±1	µA
		V_{DS}=0V, V_{GS}=±25V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.5	-2.2	-3.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-20V, I_D=-20A		6.8	8.5	mΩ
		T_J=125°C		9.1	11	
		V_{GS}=-10V, I_D=-20A		7.9	10	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-20A		50		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		0.71	-1	V
I_S	Maximum Body-Diode Continuous Current				14.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-20V, f=1MHz		3800	4560	pF
C_{oss}	Output Capacitance			560		pF
C_{rss}	Reverse Transfer Capacitance			350		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		7.5	9	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge (10V)	V_{GS}=-10V, V_{DS}=-20V, I_D=-20A		61.2	74	nC
Q_{gs}	Gate Source Charge			11.88		nC
Q_{gd}	Gate Drain Charge			15.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-20V, R_L=1Ω, R_{GEN}=3Ω		13.5		ns
t_r	Turn-On Rise Time			17		ns
$t_{D(off)}$	Turn-Off DelayTime			97		ns
t_f	Turn-Off Fall Time			43		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=100A/µs		30	36	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=100A/µs		29		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.

* This device is guaranteed green after date code 8P11 (June 1ST 2008)

Rev 2: Dec 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

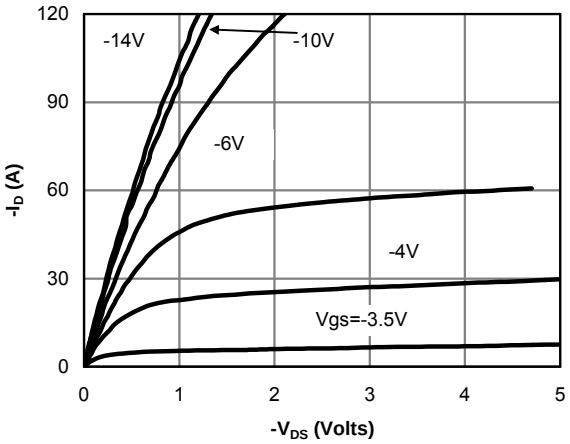


Fig 1: On-Region Characteristics

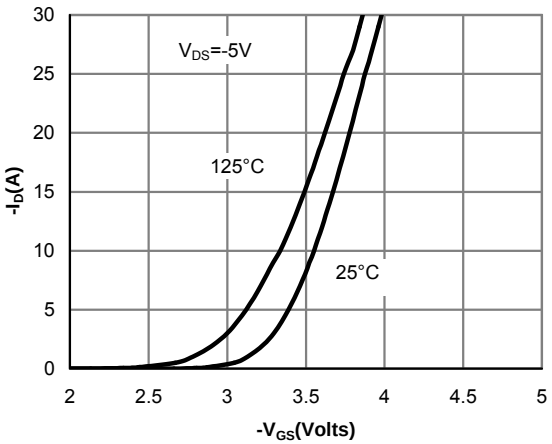


Figure 2: Transfer Characteristics

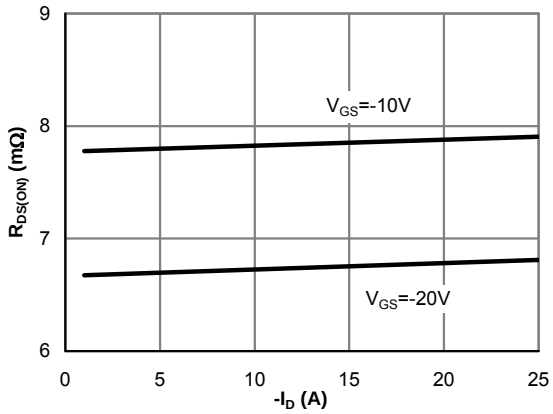


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

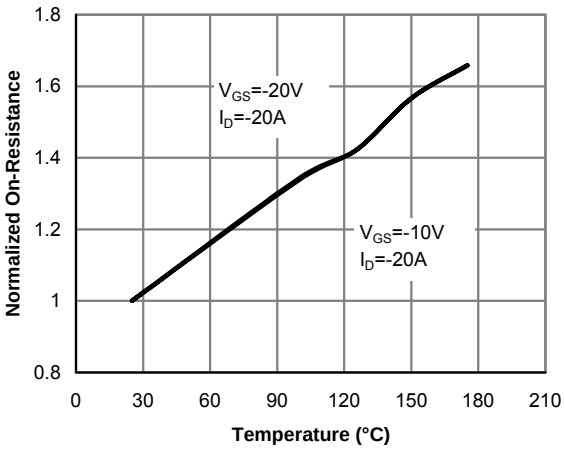


Figure 4: On-Resistance vs. Junction Temperature

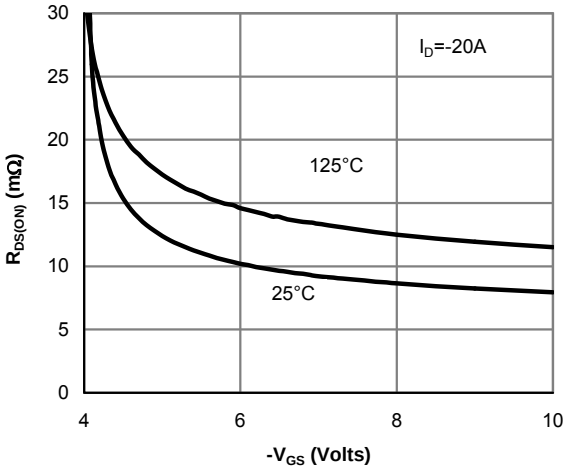


Figure 5: On-Resistance vs. Gate-Source Voltage

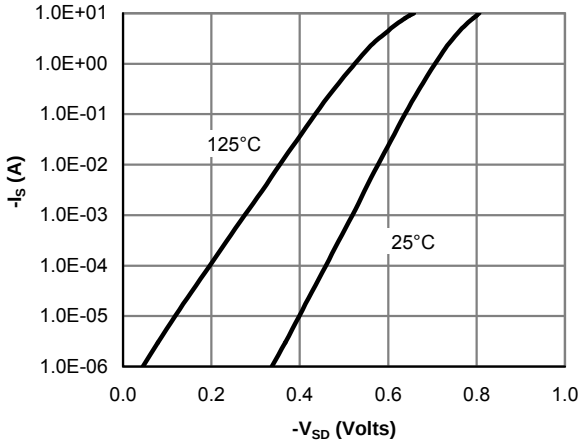


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

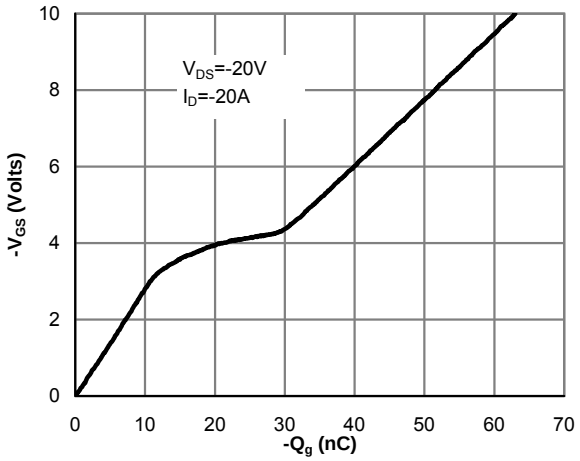


Figure 7: Gate-Charge Characteristics

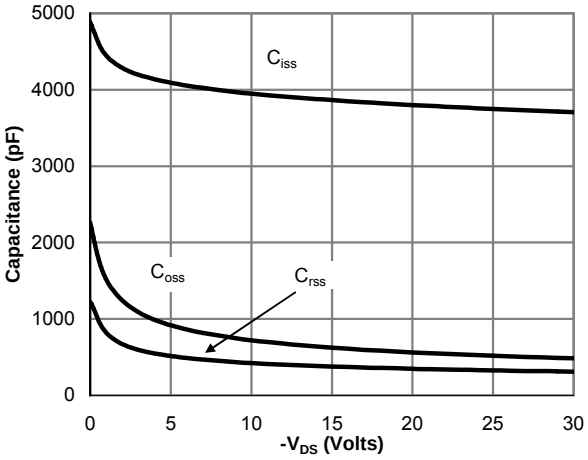


Figure 8: Capacitance Characteristics

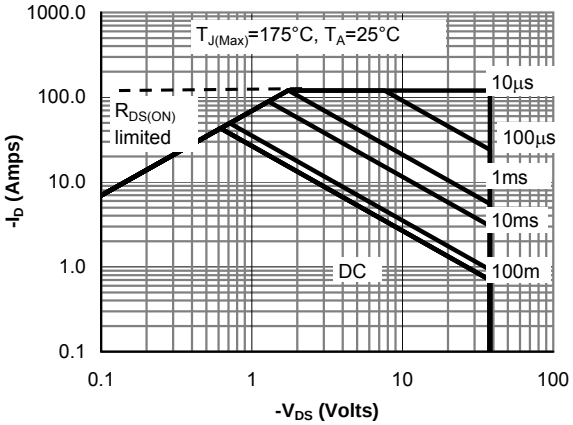


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

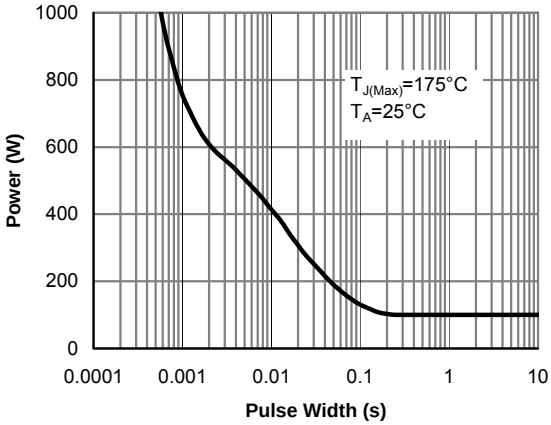


Figure 10: Single Pulse Power Rating Junction-to-Case (Note B)

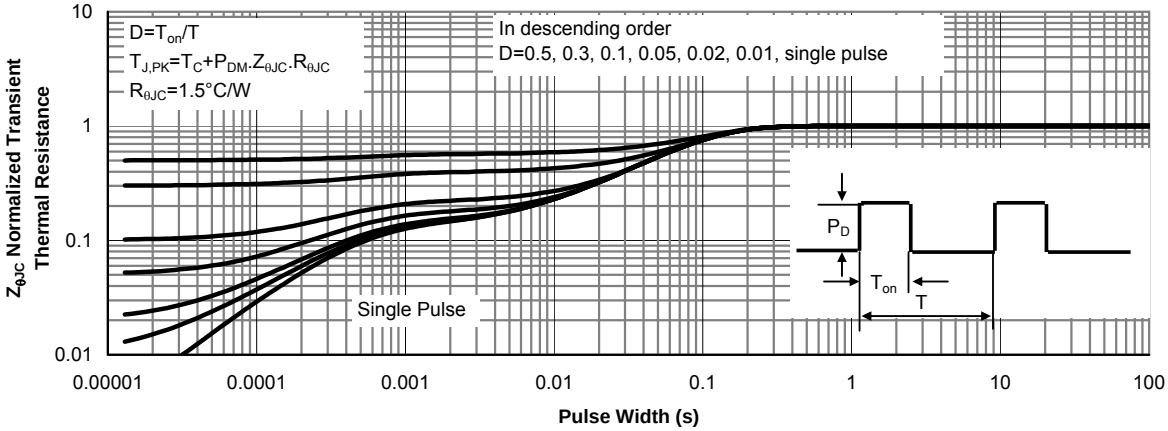


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

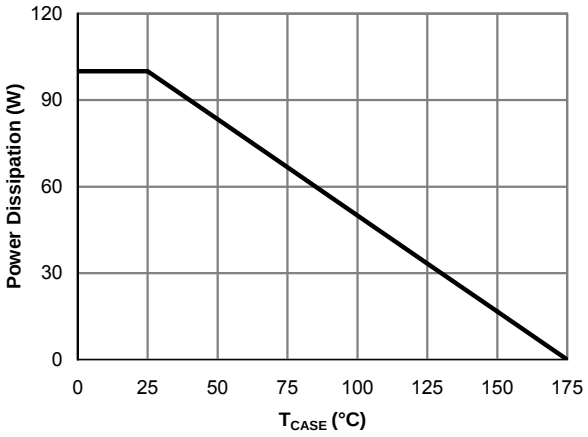


Figure 12: Power De-rating (Note B)

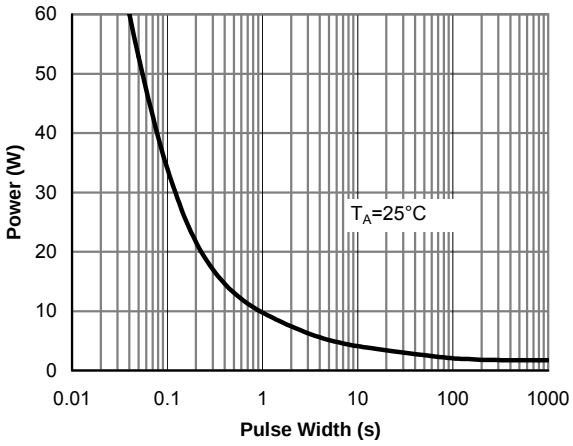


Figure 13: Single Pulse Power Rating Junction-to-Ambient (Note H)

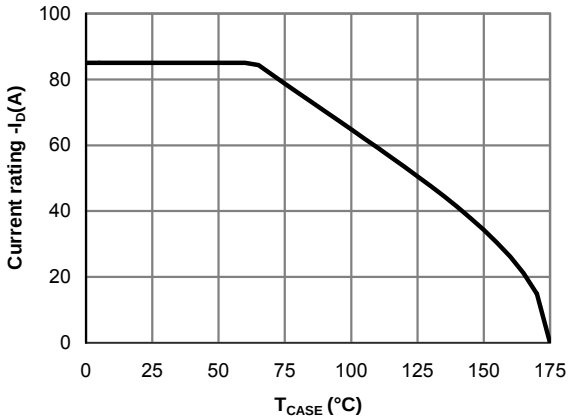


Figure 14: Current De-rating (Note B)

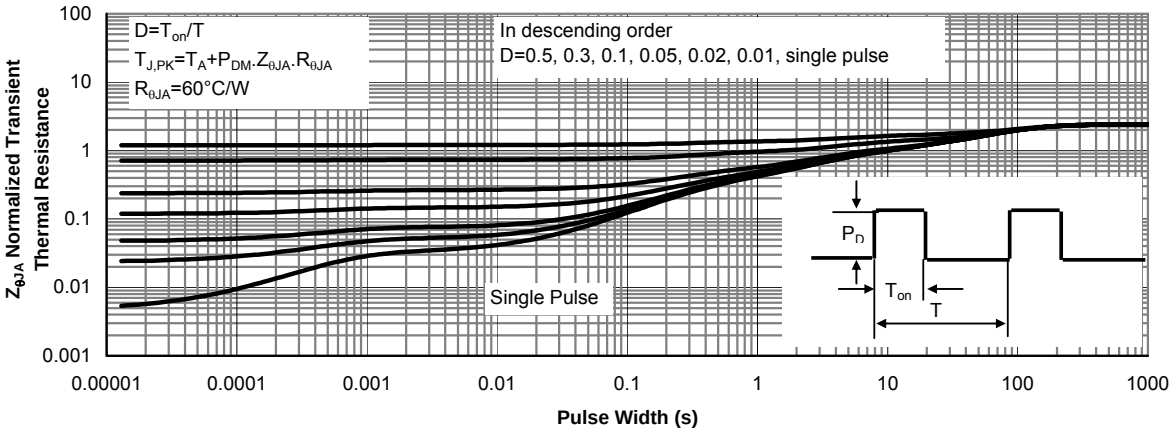
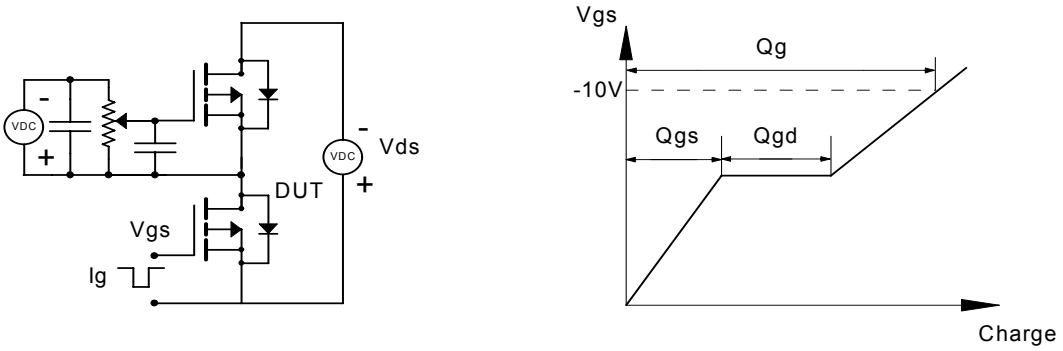
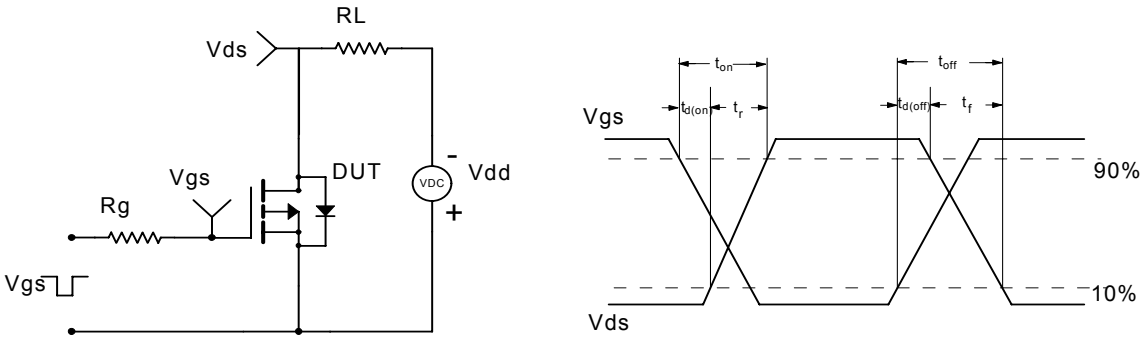


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

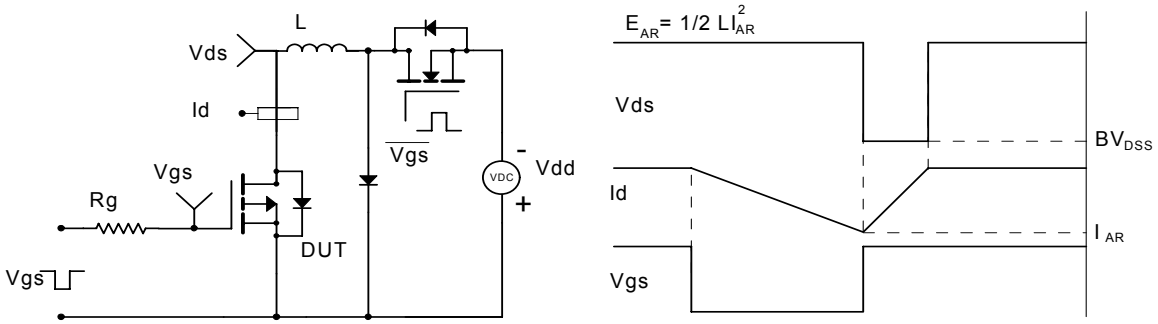
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms