



VNI4140K

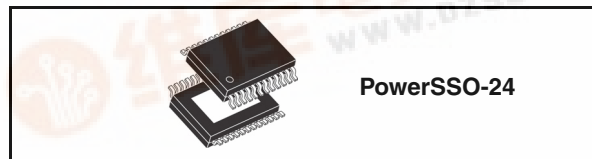
Quad high side smart power solid state relay

Features

Type	$V_{\text{demag}}^{(1)}$	$R_{\text{DSon}}^{(1)}$	$I_{\text{out}}^{(1)}$	V_{CC}
VNI4140K	$V_{\text{CC}}-41\text{ V}$	$0.08\ \Omega$	0.7 A	41 V

1. Per channel

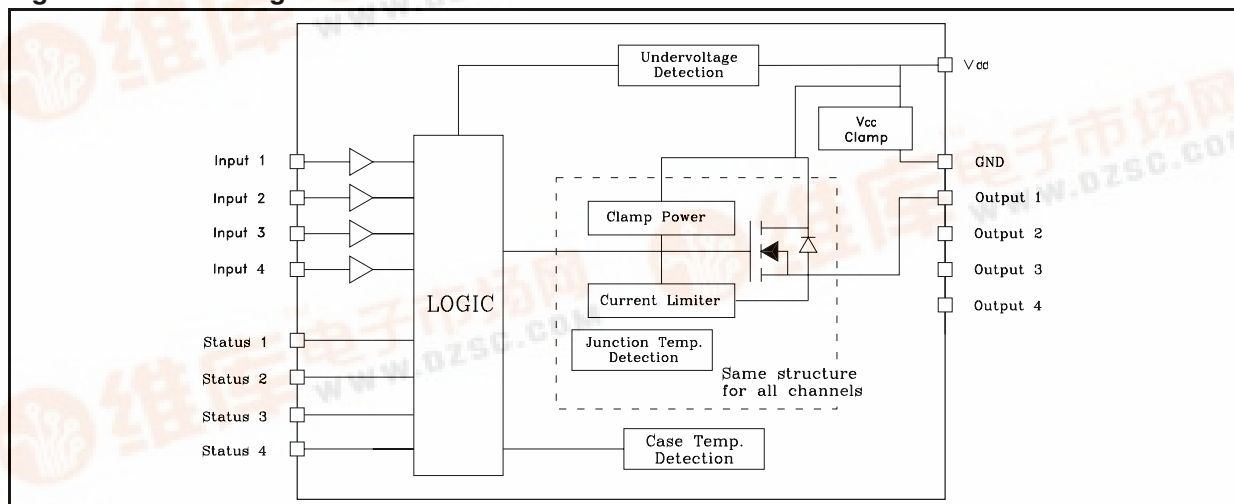
- Output current : 0.7 A per channel
- Shorted load protections
- Junction over-temperature protection
- Case overtemperature protection for thermal independence of the channels
- Thermal case shut-down restart not simultaneous for the various channels
- Protection against loss of ground
- Current limitation
- Undervoltage shut-down
- Open drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2



Description

The VNI4140K is a monolithic device made using STMicroelectronics VIPower technology, intended for driving four independent resistive or inductive loads with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shut-down protects the chip from overtemperature and short circuit. In overload condition, channel turns OFF and back ON automatically so as to maintain junction temperature between T_{TSD} and T_{R} . If this condition makes case temperature reach T_{CSD} , overloaded channel is turned OFF and will restart only when case temperature has decreased down to T_{CR} . In case of more than one channel in overload, re-start of the overloaded channels will not be simultaneous, in order to avoid high peak current from the supply. Non overloaded channels continue to operate normally. The open drain diagnostics outputs indicates over-temperature conditions.

Figure 1. Block diagram



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1 Pin connection

Figure 2. Pin connection (top view)

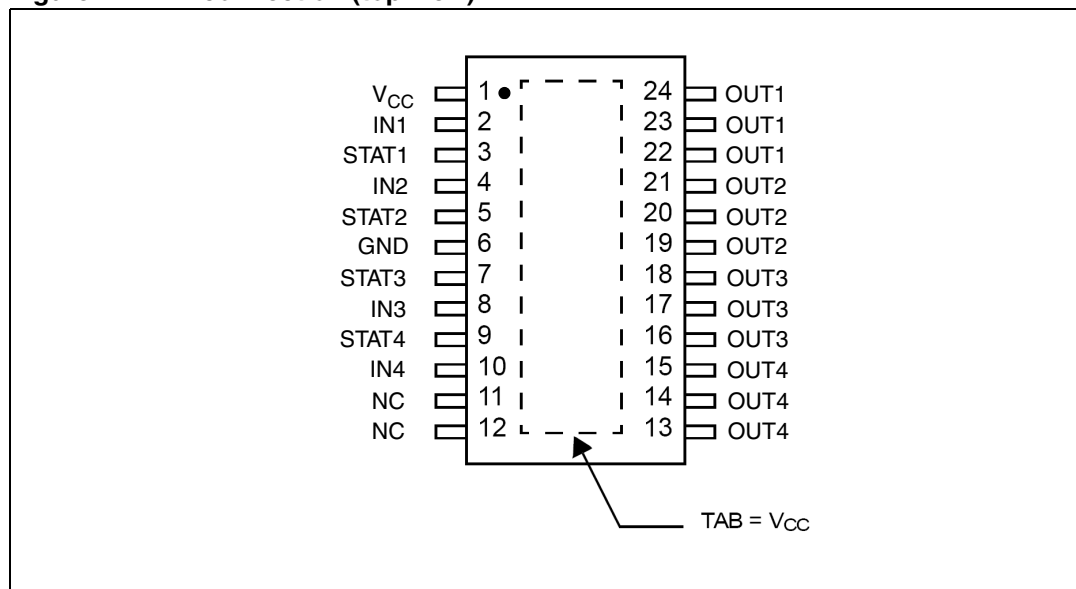


Table 1. Pin description

Pin	Name	Description
Tab	TAB	Exposed tab internally connected to Vcc
1	Vcc	Supply voltage
2	IN1	Channel 1 input 3.3V CMOS/TTL compatible
3	STAT1	Channel 1 status in open drain configuration
4	IN2	Channel 2 input 3.3V CMOS/TTL compatible
5	STA2	Channel 2 status in open drain configuration
6	GND	Device ground connection
7	STAT3	Channel 3 status in open drain configuration
8	IN3	Channel 3 input 3.3V CMOS/TTL compatible
9	STAT4	Channel 4 status in open drain configuration
10	IN4	Channel 4 input 3.3V CMOS/TTL compatible
11	NC	
12	NC	
13	OUT4	Channel 4 power stage output, internally protected
14	OUT4	Channel 4 power stage output, internally protected
15	OUT4	Channel 4 power stage output, internally protected
16	OUT3	Channel 3 power stage output, internally protected
17	OUT3	Channel 3 power stage output, internally protected

Table 1. Pin description (continued)

Pin	Name	Description
18	OUT3	Channel 3 power stage output, internally protected
19	OUT2	Channel 2 power stage output, internally protected
20	OUT2	Channel 2 power stage output, internally protected
21	OUT2	Channel 2 power stage output, internally protected
22	OUT1	Channel 1 power stage output, internally protected
23	OUT1	Channel 1 power stage output, internally protected
24	OUT1	Channel 1 power stage output, internally protected

2 Maximum ratings

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
I_{GND}	DC ground reverse current	-250	mA
I_{OUT}	Output current (continuous)	Internally limited	A
I_R	Reverse output current (per channel)	-5	A
I_{IN}	Input current (per channel)	± 10	mA
V_{IN}	Input voltage	$+V_{CC}$	V
V_{STAT}	Status pin voltage	$+V_{CC}$	V
I_{STAT}	Status pin current	± 10	mA
V_{ESD}	Electrostatic discharge ($R = 1.5\text{ K}\Omega$; $C = 100\text{ pF}$)	2000	V
E_{AS}	Single pulse avalanche energy per channel not simultaneously	300	mJ
P_{TOT}	Power dissipation at $T_c = 25\text{ }^\circ\text{C}$	Internally limited	W
T_J	Junction operating temperature	Internally limited	$^\circ\text{C}$
T_{STG}	Storage temperature	-55 to 150	$^\circ\text{C}$

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case ⁽¹⁾	Max 2	$^\circ\text{C/W}$
$R_{th(JA)}$	Thermal resistance junction-ambient	Max see Figure 10	$^\circ\text{C/W}$

1. Per channel

3 Electrical characteristics

(10.5 V < V_{CC} < 36 V; -25 °C < T_J < 125 °C; unless otherwise specified)

Table 4. Power section

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage		10.5		36	V
$R_{DS(ON)}$	On state resistance	$I_{OUT} = 0.5$ A at $T_J = 25$ °C $I_{OUT} = 0.5$ A			0.080 0.140	Ω Ω
V_{clamp}		$I_S = 20$ mA	41	45	52	V
I_S	Supply current	All channel in OFF state ON state with $V_{IN} = 5$ V ($T_J = 125$ °C)		250 2.4	4	μ A mA
$V_{OUT(OFF)}$	OFF state output voltage	$V_{IN} = 0$ V and $I_{OUT} = 0$ A			1	V
$I_{OUT(OFF)}$	OFF state output current	$V_{IN} = V_{OUT} = 0$ V	0		5	μ A
F_{CP}	Charge pump frequency	Channel in ON state ⁽¹⁾		1450		kHz

1. To cover EN55022 class A and class B normative

Table 5. Switching ($V_{CC} = 24$ V; -25 °C < T_J < 125 °C, $R_L = 48$ Ω , input rise time < 0.1 μ s)

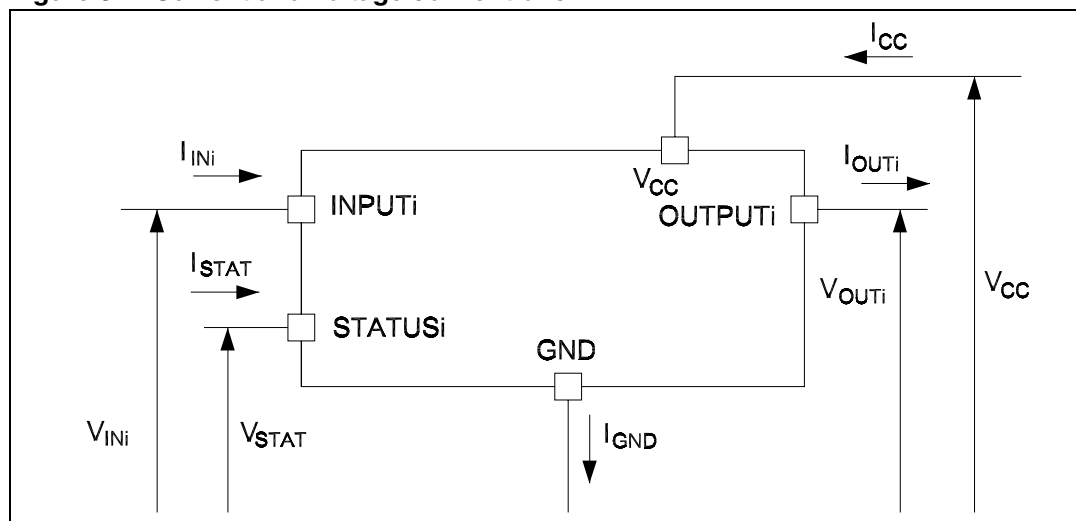
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{d(ON)}$	Turn ON delay			20		μ S
t_r	Rise time			10		μ S
$t_{d(OFF)}$	Turn OFF			30		μ S
t_f	Fall time			8		μ S
$dV/dt_{(ON)}$	Turn ON voltage slope			3		V/ μ S
$dV/dt_{(OFF)}$	Turn OFF voltage slope			4		V/ μ S

Table 6. Logical input

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.20			V
$V_{I(HYST)}$	Input hysteresis voltage			0.15		V
I_{IN}	Input current	$V_{IN} = 15\text{ V}$			10	μA
		$V_{IN} = 36\text{ V}$			210	

Table 7. Protection and diagnostic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{STAT}	Status voltage output low	$I_{STAT} = 1.6\text{ mA}$			0.6	V
V_{USD}	Undervoltage protection		7		10.5	V
V_{USDHYS}	Undervoltage hysteresis		0.4	0.5		V
I_{LIM}	DC short circuit current	$V_{CC} = 24\text{ V}$; $R_{LOAD} < 10\text{ m}\Omega$	0.7	1	1.7	A
I_{PEAK}	Maximum DC output Current	Dynamic load		1.3		A
Hyst	Traking limits			0.2		A
I_{LSTAT}	Status leakage current	$V_{CC} = V_{STAT} = 36\text{ V}$		30		μA
T_{TSD}	Junction shut down temperature		150	170	190	$^{\circ}\text{C}$
T_R	Junction reset temperature		135			$^{\circ}\text{C}$
T_{HIST}	Junction thermal hysteresis		7	15		$^{\circ}\text{C}$
T_{CSD}	Case shut-down temperature		125	130	135	$^{\circ}\text{C}$
T_{CR}	Case reset temperature		110			$^{\circ}\text{C}$
T_{CHYST}	Case thermal hysteresis		7	15		$^{\circ}\text{C}$
V_{demag}	Output voltage at turn-OFF	$I_{OUT} = 0.5\text{ A}$; $L_{LOAD} \geq 1\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 45$	$V_{CC} - 52$	V

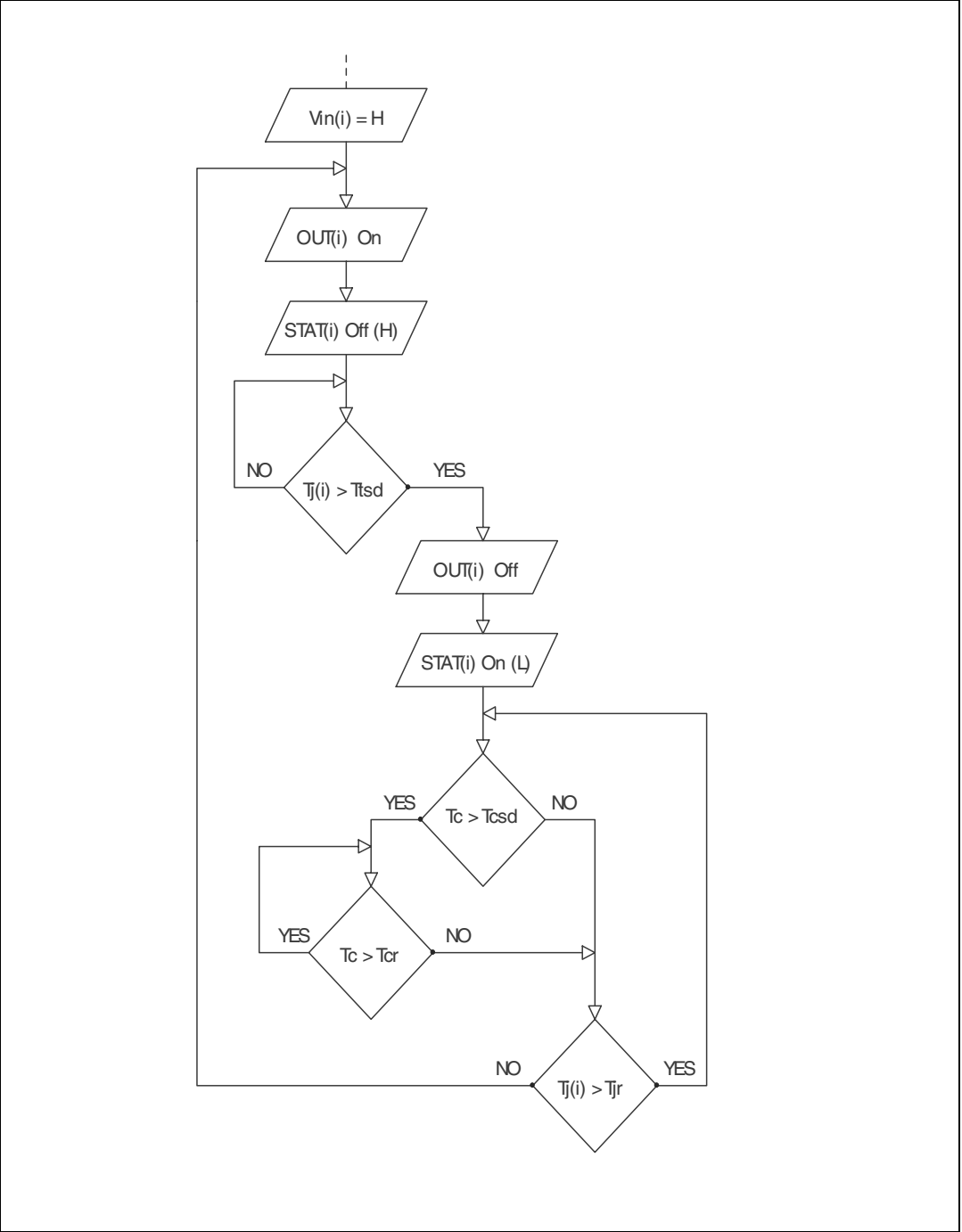
Figure 3. Current and voltage conventions

4 Truth table

Table 8. Truth table

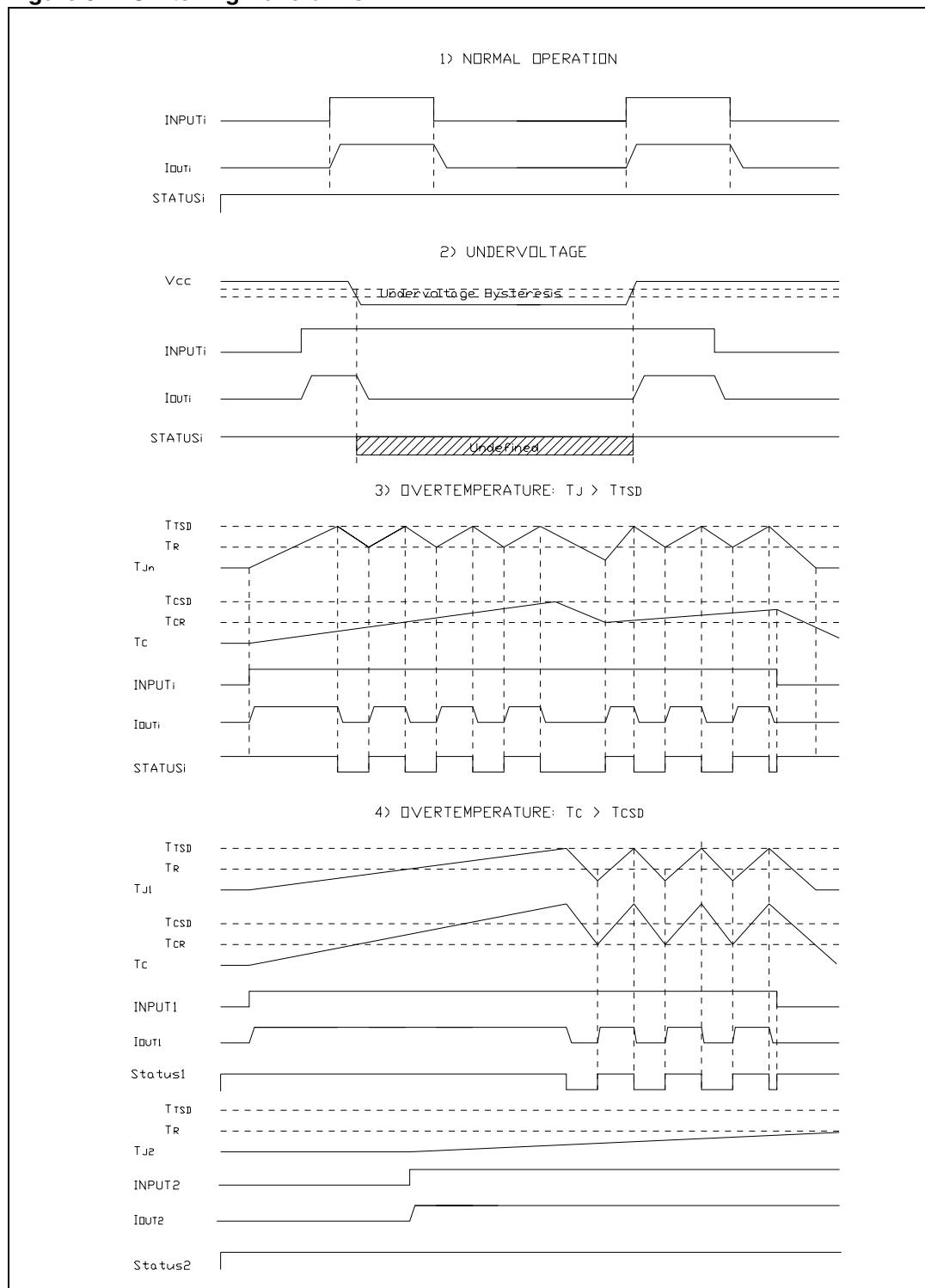
	INPUT _n	OUTPUT _n	STATUS _n
Normal operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Shorted load (Current limitation)	L	L	H
	H	X	H

Figure 4. Thermal behavior



5 Switching waveforms

Figure 5. Switching waveforms



6 Pin functions

Figure 6. Input circuit

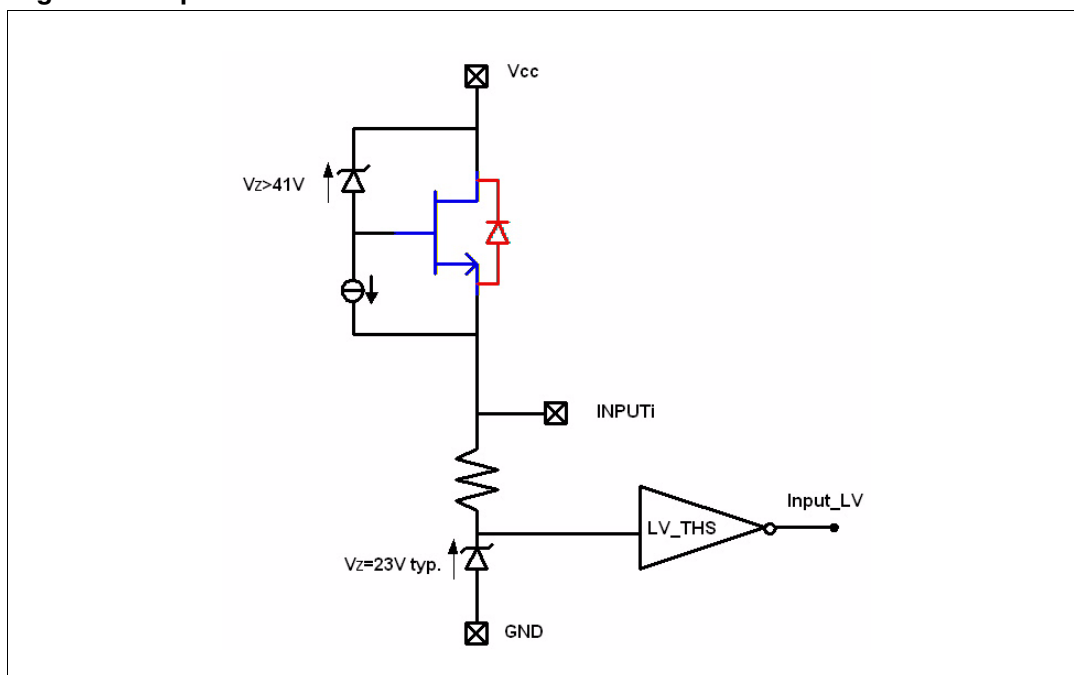


Figure 7. Status circuits

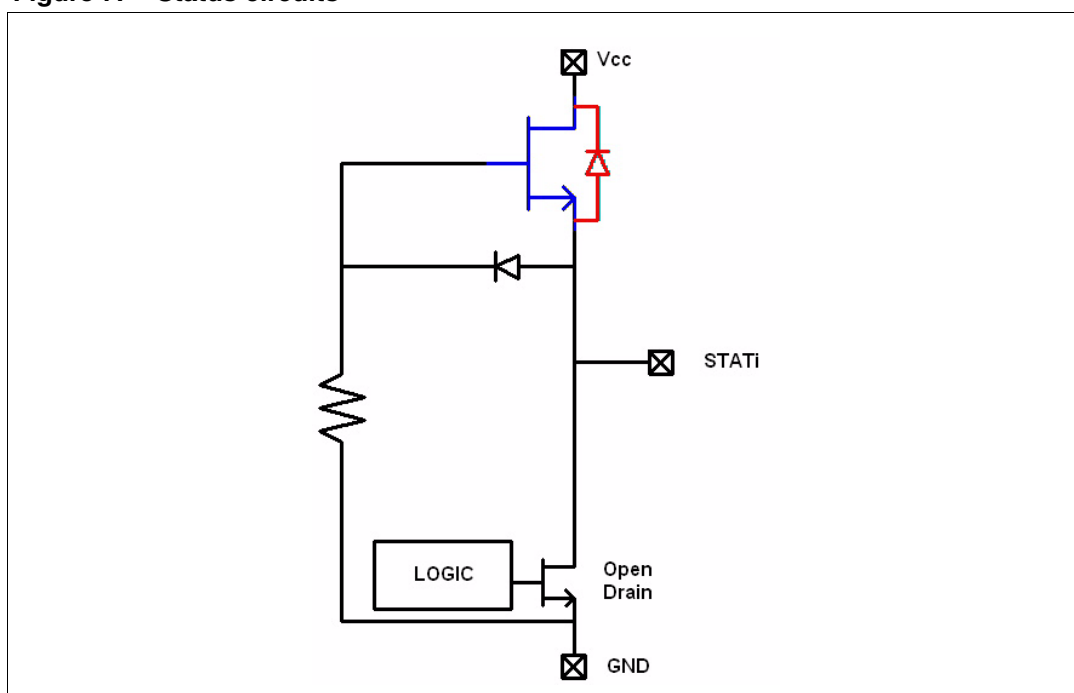
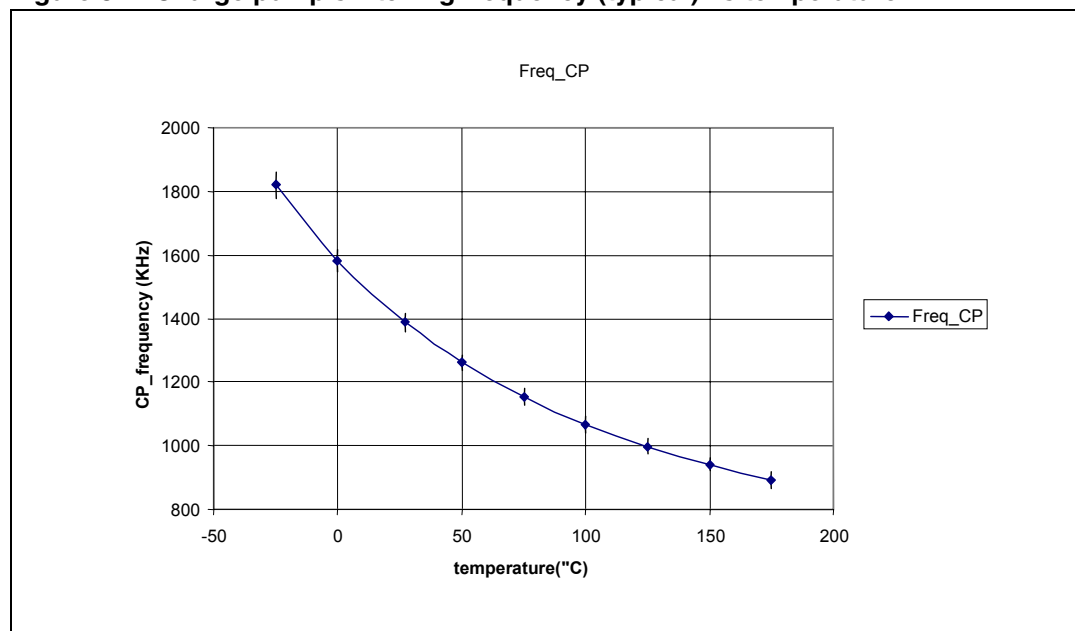
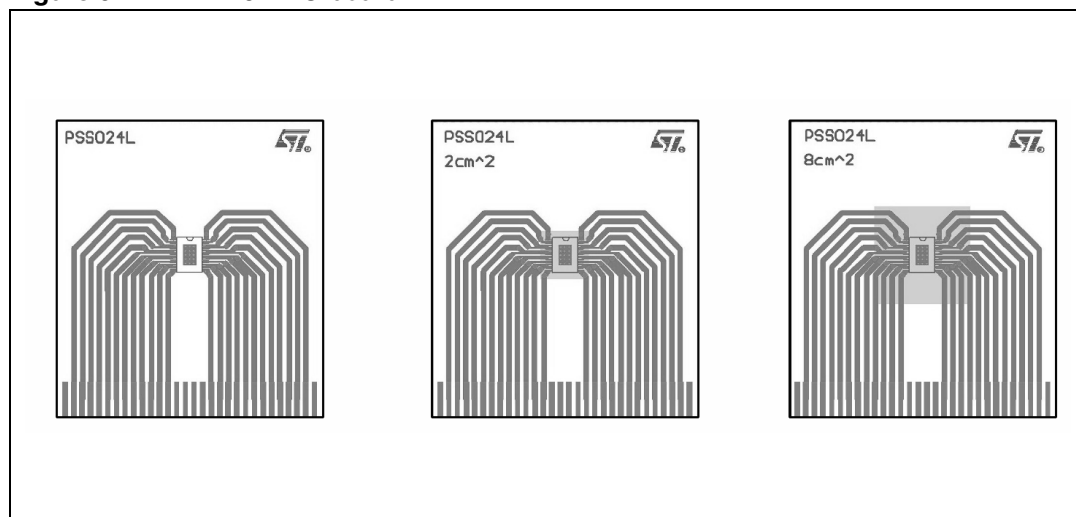


Figure 8. Charge pump switching frequency (typical) vs temperature

7 Package and PC board thermal data

7.1 VNI4140K thermal data

Figure 9. VNI4140K PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area = 77 mm x 86 mm, PCB thickness=1.6 mm, Cu thickness = 70 mm (front and back side), Copper areas: from minimum pad lay-out to 8 cm²).

Figure 10. R_{thJA} vs PCB copper area in open box free air condition (one channel ON)

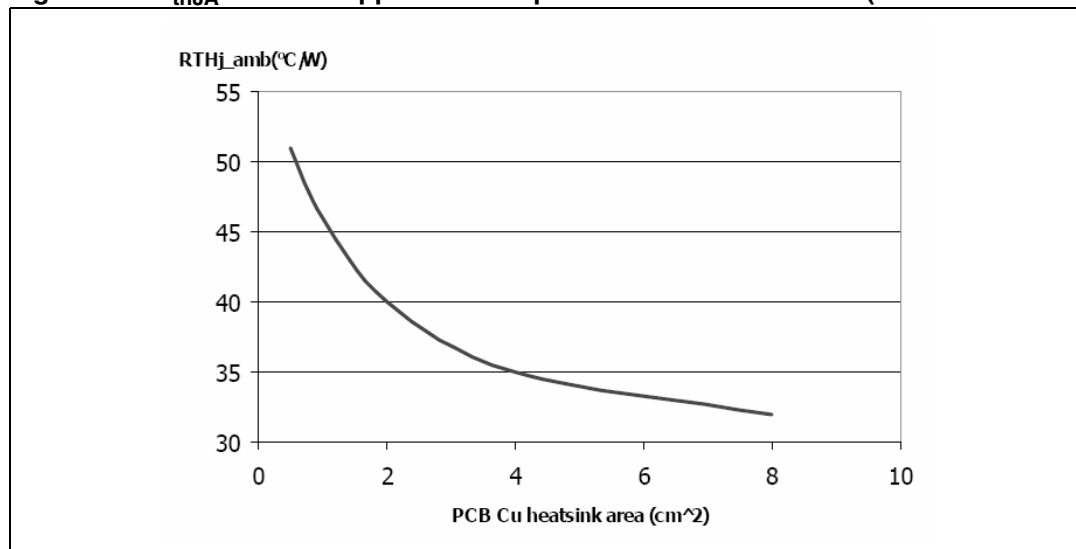
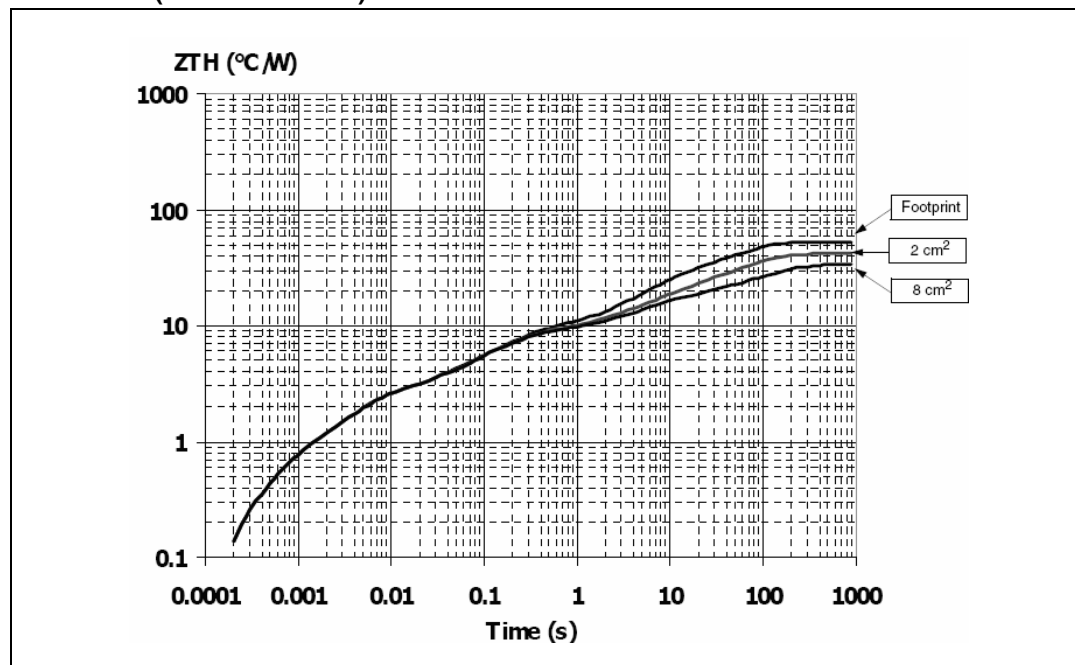


Figure 11. VNI4140K thermal impedance junction ambient single pulse
(one channel on)



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 9. PowerSSO-24™ mechanical data

Symbol	mm		
	Min	Typ	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

Figure 12. PowerSSO-24™ package dimensions

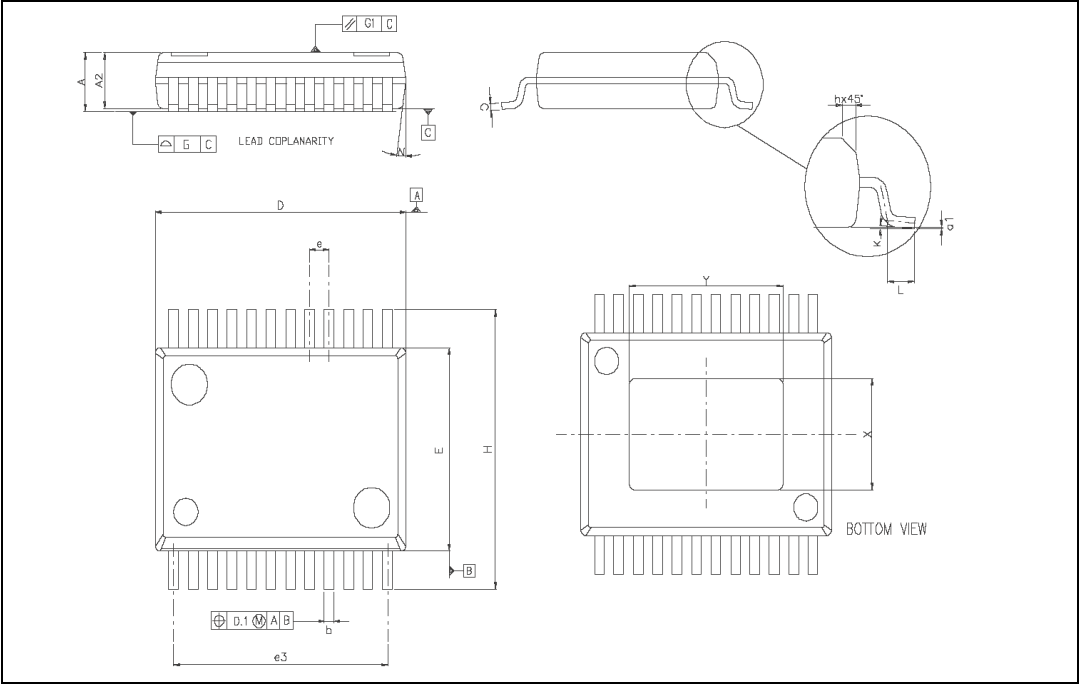
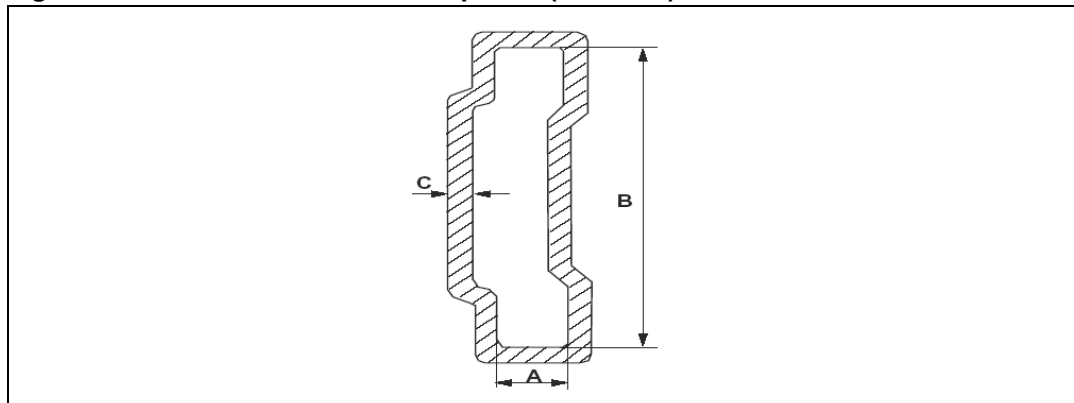


Figure 13. PowerSSO-24™ tube shipment (no suffix)**Table 10. PowerSSO-24™ tube shipment**

Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

Note: All dimensions are in mm.

Figure 14. PowerSSO-24™ reel shipment (suffix “TR”)

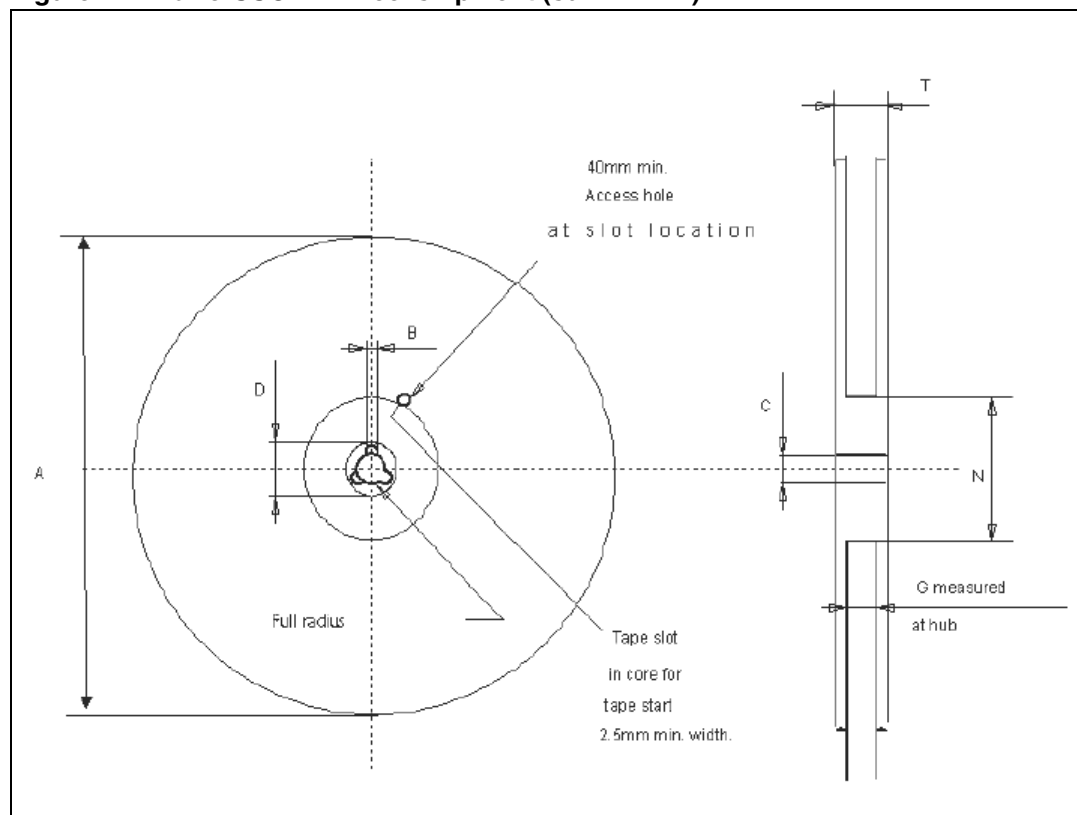


Table 11. PowerSSO-24™ reel dimensions

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (2 ± 0)	24.4
N (min)	100
T (max)	30.4

Figure 15. PowerSSO-24™ tape dimensions

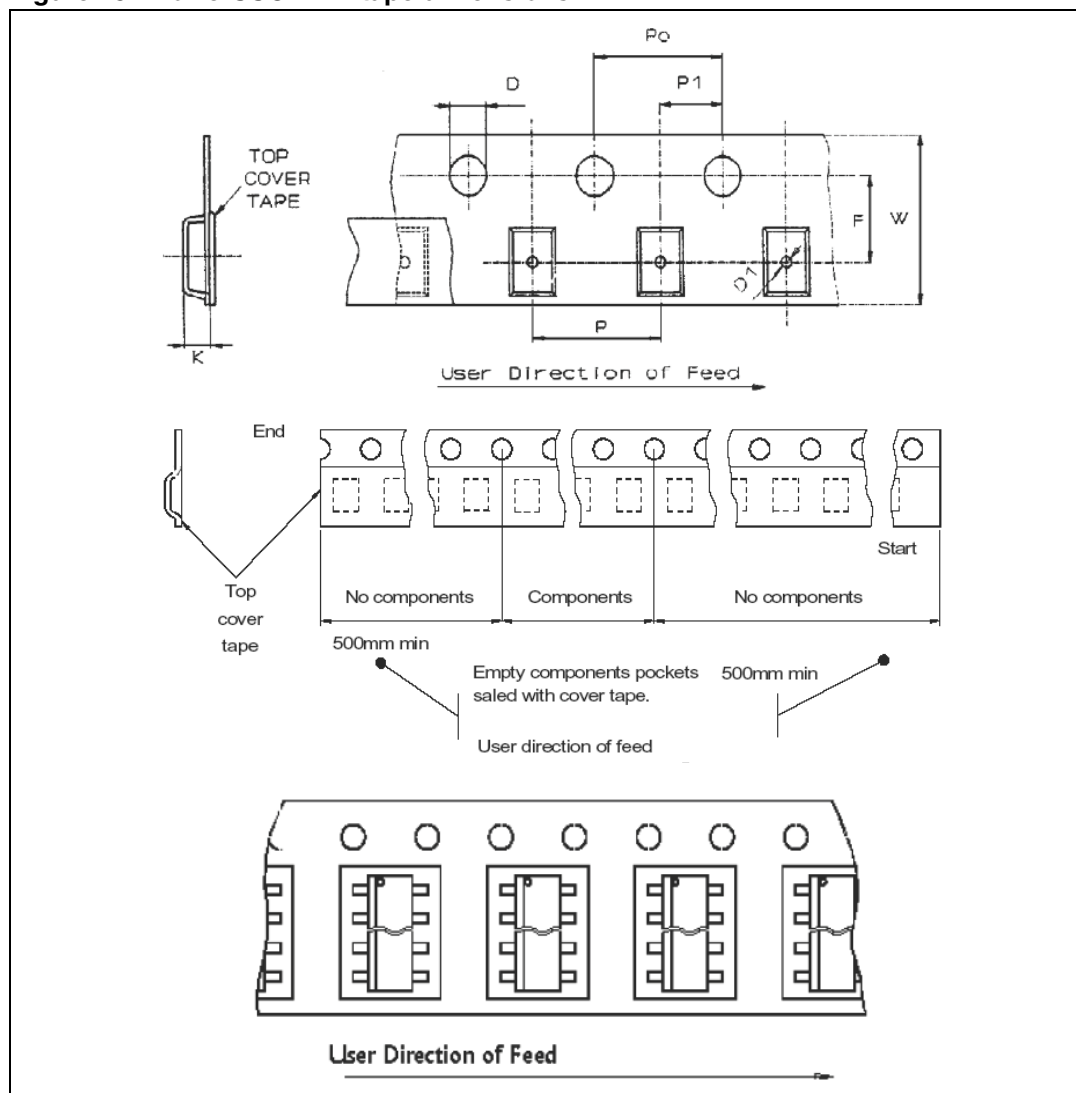


Table 12. PowerSSO-24™ tape dimensions

Tape width	W	24
Tape Hole Spacing	$P_0 (\pm 0.1)$	4
Component Spacing	P	12
Hole Diameter	$D (\pm 0.05)$	1.55
Hole Diameter	$D_1 (\text{min})$	1.5
Hole Position	$F (\pm 0.1)$	11.5
Compartment Depth	K (max)	2.85
Hole Spacing	$P_1 (\pm 0.1)$	2

Note: According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

9 Order codes

Table 13. Order codes

Part number	Package	Packaging
VNI4140K	PowerSSO-24	Tube
VNI4140KTR	PowerSSO-24	Tape and reel

10 Revision history

Table 14. Document revision history

Date	Revision	Changes
16-Nov-2007	1	Initial release
26-Nov-2007	2	Updated electrical parameters values

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