RTL8201 PCB Layout Guide

1. Introduction

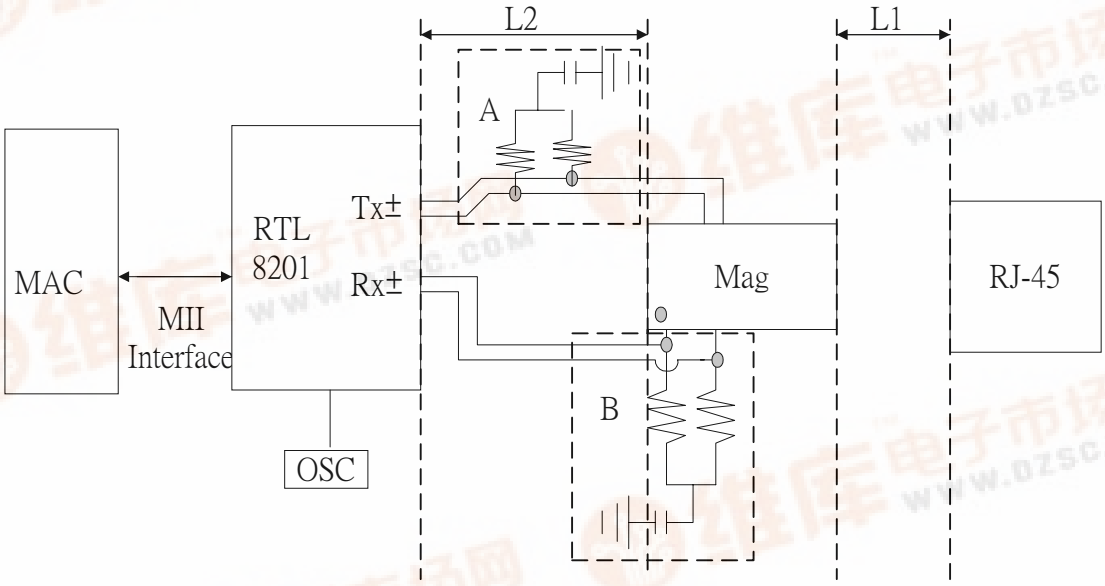
Goal : (1) Make a Noise-free, power-stable, environment that suitable for RTL8201.

(2) Reduce the possibility of EMI, EMC and their influence to the chip.

(3) Simplify the task of routing signal trace, so as to make a better circuit for RTL8201.

2. Placement

Ideally placement: as fellow



- Block A should place as close to RTL8201 as possible. Block B may be placed close to Mag. (Since when Tx, RTL8201 will sink current from Block A. When Rx, RTL8201 will take differential volt signal from Block B.
- The distance between RJ-45 to Mag. (L1) should be as short as possible.
- RTset of RTL8201 pin 28 should placed as close to RTL8201 as possible and if possible, it should be placed away from TX+/-,RX+/-, and clock signals.
- Crystal should not be placed near I/O ports and board edges and other high-freq. devices or traces (such as Tx , Rx and Power signals) or magnetic field device (such as magnetic).
- The outer shield of Crystal need well grounding to avoid EMC/EMI to induce extra noise, the retaining straps of the Crystal need well grounding, so as the case of Crystal.
- The magnetic device or devices with magnetic fields should be separated and

mounted at 90° to each others. High Current devices should be placed near to the Power source to reduce the trace length. Traces with high current will induce more EMI.

- Termination Resistors :

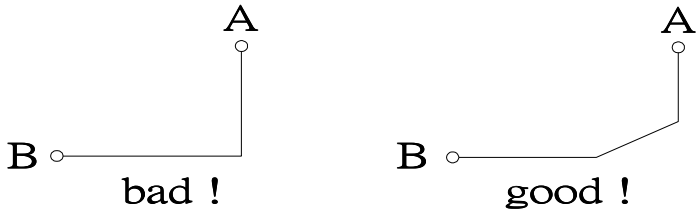
  As above in Block A and B, pull high resistors and cap of A need to be close to RTL8201 and the two receiving termination resistors (50Ω) may be placed close to Mag. For better impedence matching, these resistor/cap pairs should be chosen carefully.

- The traces between RTL8201 and Mag. (L2) are too, as short as possible. For practical implementation convenience, this could be sacrificed. But it is important to keep the Tx±, Rx± signal traces to be symmetry, and L2 is still needed to keep in a reasonable range, about 10~12cm Maximum.
- The signal trace length difference between Tx+ and Tx- (Rx+ and Rx-) should be kept within 2 cm.

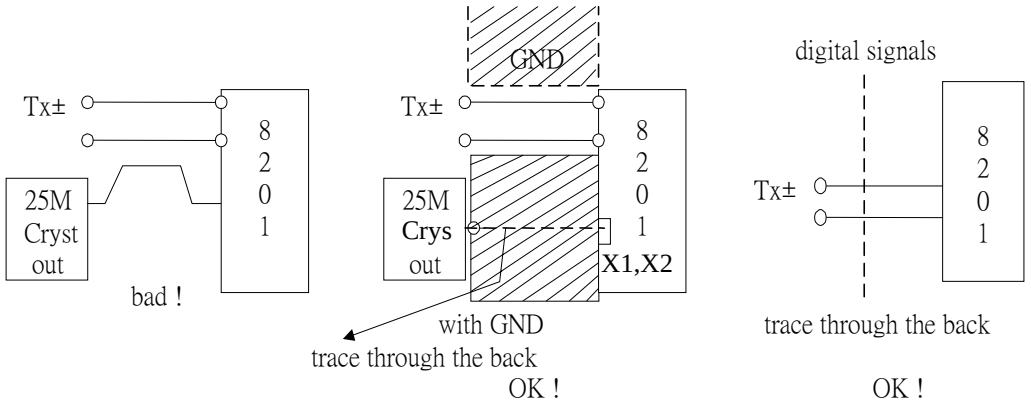
3. Trace Routing

Good routing of traces can reduce the propagation delay, cross-talk, high-freq. noise and improve the signal quality that receiver received and reduce the loss from transmit signals.

- Avoid right angle signal trace :



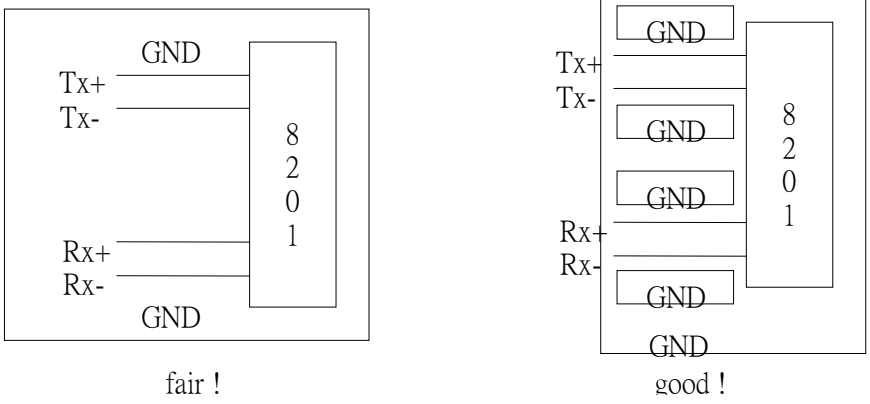
- Avoid digital signals (such as MII signals or CLOCKs) to interference with



analog signals (Tx±, Rx±, RTset trace) and Power trace! And if it is necessary to

cross the digital signals with Analog/Power, you had better a 90° cross.

- The trace length and the ratio of trace width to trace height above the ground planes should be consider carefully. The clocks and other high speed signal trace should be short and wide as possible. (compare with normal digital trace). It is better to have a ground plane under these traces, and if possible, with GND plane around.
- Trace length of a signal should not exceed 1/20 of the highest harmonic (about 10^{th}) wavelength. For example, the 25M clock trace should not exceed 30cm and the 125M signal traces should not exceed 12cm (Tx±, Rx±).
- The trace of Power signal (de-couple cap traces, power traces, grounding traces) should be short and wide, the VIAs of de-couple cap should be larger in diameter.
- Each cap should have a separated VIA to GND. GND VIA should be within 0.2 inch. Avoid the following de-couple cap connection :

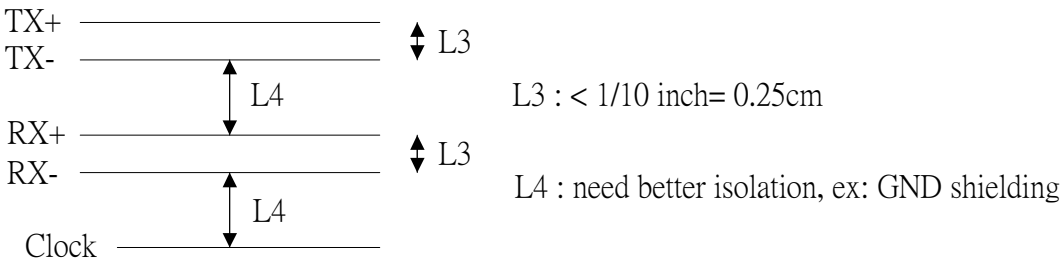


- De-couple cap

  Should be placed as close to IC as pos., the traces should be short. Every RTL8201 analog power need de-couple (pin 32, 36, 48). Every RTL8201 digital power with a de-couple cap will be better, especially, for 8, 14 pin (connected as follow).

- Ferrite Bead placement: The bead connected to 32, 36, 48 should be close to RTL8201, at least 48 pin must need beads (100M/100Ω).
- Tx±, Rx± traces should pay more attention :

- Avoid signal loss on these traces.
- Tx+, Tx- should be equal length as possible.
  Rx+, Rx- should be equal length as possible.
- The distance between Tx± and Rx± :



- Rx± had better not using via, i.e., the Rx± traces at the component side.
- Ferrite Beads should be close to chip pins and have the rating of 100Ω@100MHz

- Keep the distance between the Tx and Rx signal pairs large, decrease the portion of these two signal-pair traces going together in parallel. Furthermore, you can even separate Ground planes underneath Tx and Rx signal pairs.

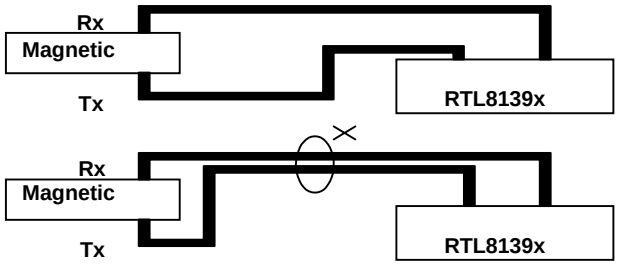


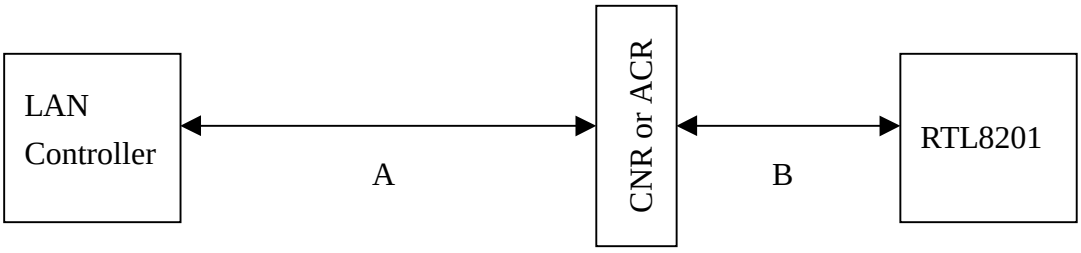
Fig 3. Separate Tx and Rx signal pairs

- Magnetic: Any Magnetic with Tx/Rx turn ration of 1:1/1:1 are suitable for RTL8201, such as Pulse PE68515/H1012, Valor ST6118, YCL 20PMT04, DELTA LF8221, BH16ST8515, TAIMIC HSIP-002.

4. Trace Connection of MII Interface to LAN Controller

- Following figure shows the RTL8201 Lan-on-Motherboard suggested trace lengths using an optional CNR or ACR connector. We suggest the trace length between LAN controller and RTL8201 should be as short as possible and if possible, and the maximum trace length must be shorter than 10 inch.
- As showed in following figure, please make sure that the length mismatch between data signals and its related clock doesn't exceed 1 inches, ex., the trace groups such as TXD[0-3] and TXCLK, RXD[0-3] and RXCLK.
- When RTL8201 links at 100M speed, the TXCLK and RXCLK is 25MHz clock to

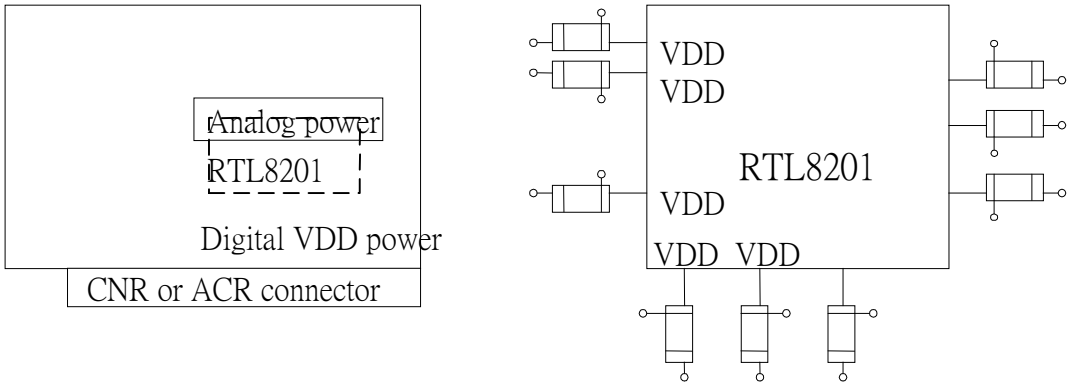
MAC. When link at 10M speed, the TXCLK and RXCLK is 2.5 MHz clock to MAC. Both TXData and Rxdata are latched at rising edge of clock. The detail MII timing description and specification can refer to IEEE802.3u clause 22.



Dimension A = 1 to 7 inch (optional)
Dimension B = 1 to 3 inch

5. Power and Ground Plane

- 3.3V power: support RTL8201 and other devices. Avoid using unnecessary power trace to RTL8201 and keep these traces as short and wide and make good use of via. Keep the 3.3V power plane as a whole, and leave some space for Analog power plane.



- As showed in RTL8201 schematic, we have reserved a region “Block A”, please reserve the components space and pads in your layout for future 2.5v core extension.
- GND plane

  We can separate the digital GND to Analog GND as follow:

  Partition of GND plane need experience and experiment, the key point is to keep analog GND's return path about equal to the common GND, if you do not have confidence on this, simply leave the GND plane unchanged, ie, no partition at all.
- For all partition on Power/GND plane, no right angle is recommend. The same to the signal/power/bus traces.
- Digital GND's of RTL8201 should use via from digital GND plane to device's pin and Analog GND's of RTL8201 and Tx±/Rx± peripheral circuit GND's should

connect to Analog GND plane.

Digital GND: all GND pin of RTL8201 except Analog GND pin.

Digital Power: all VDD pin of RTL8201 except Analog power pins.

Analog GND: 29, 35, 45

Analog Power: 32, 36, 48

- Both RJ-45 connector and the secondary side of the magnetic, which connects the RJ-45 connector, use their own isolated ground. No power and ground planes exist underneath this isolated area.

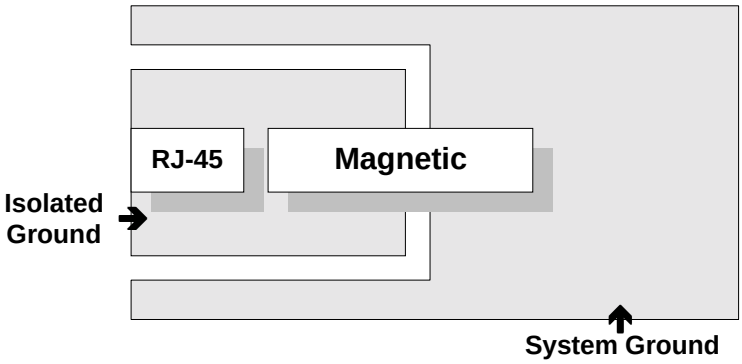
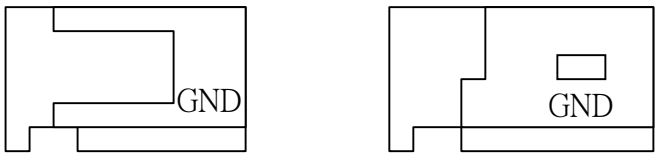


Fig 2. Isolate RJ-45 connector ground from system ground

6. Notice at ACR Card

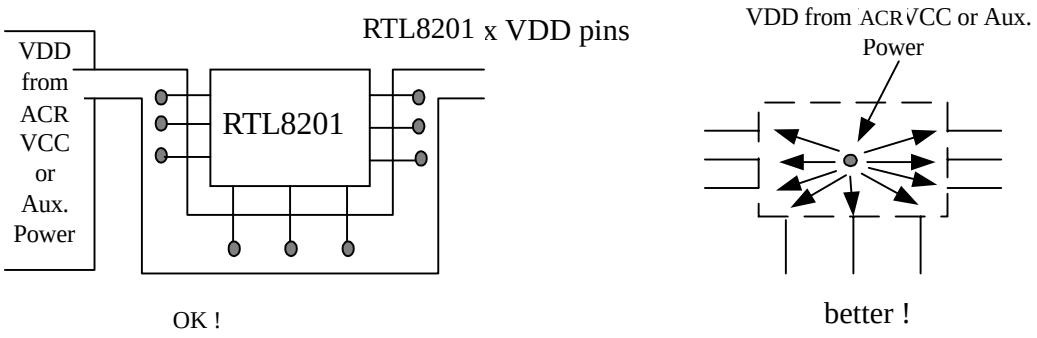
- If RTL8201 is connected to a controller watching for a wake-on-lan packet, you may use 3.3Vaux supported by ACR slot as your power source for RTL8201 and its related peripheral components. If other devices on ACR card also use the 3.3Vaux power at the same time, the total current consumption supplied by 3.3Vaux on your ACR card must lower than 0.375A to confirm to ACR specification.
- For better performance on GND plane at 2-Layer design, please follow as shown :



not good ! better !

- The MII interface of fast ethernet PHYceiver on ACR card is connected to primary MII showed as ACR specification. Because the ACR specification is not defined already, so if you want to produce the ACR card, please doubly check with the chipset vendors and motherboard vendors.

- For better performance on Power plane at 2-Layer design, please follow as shown:



7. For better and more stable analog performance:

- The analog GND pins (29, 35, 45) must maintain a good ground return path, so avoid using single ended ground, enlarge the analog GND plane, and try to keep the analog circuit's return current back to the real GND(from ACR slot) as soon as possible. This is especially important for 2-layer's layout.
- For EMI's consideration, if you find that the EMI is a bit serious when read/write from MII interface. You had better add some de-couple cap.(0.047uf, 22uf) between the system GND-Power planes.
- When using 25Mhz crystal as clock source, the spec. of crystal should pay more attention, please refer to the attached crystal spec. When using crystal as spec. two matching caps (20pF in schematic) should be attached to the X1 and X2 pin.
- When using oscillator as clock source (25Mhz), avoid attaching any cap on the clock trace.
- All analog power pins (pin 32, 36, 48) need a ferrite bead and these pins should be de-coupled as the schematic file’s suggestion. Please pay special attention on pin 48. These beads should be placed as close to RTL8201 as possible.
- No GND plane partition is recommended, please keep the GND plane as large and clear as possible.
- When using regulator as 5V -> 3.3V, the rated current of this regulator should be at least 300mA.