004958

DEVICE SPECIFICATION

APPLIED MICRO CIRCUITS CORPORATION

Q700 SERIES ECL/TTL LOGIC ARRAYS

FEATURES

VARIOUS ARRAY SIZES
250, 500, 1000 equivalent gate versions to support various circuit requirements.

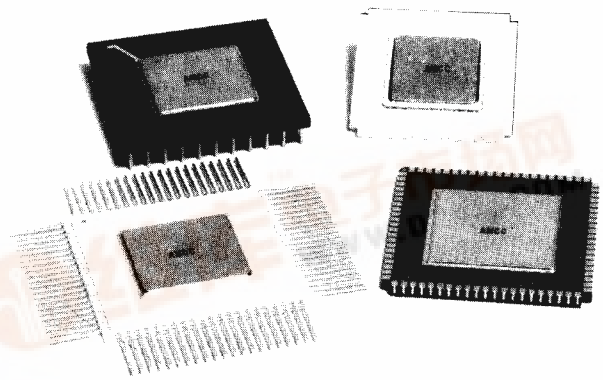
VERY HIGH SPEED
0.5 to 0.9 ns average gate delay within the internal array.

ECL & TTL COMPATIBILITY
The Q700 series logic arrays are compatible with ECL, TTL or simultaneous ECL/TTL systems, in both single and multiple power supply configurations. This flexible I/O structure eliminates the need for ECL/TTL and TTL/ECL translator logic in high performance applications.

MODERATE POWER
The Q700 series devices offer the advantage of low power ECL coupled with the very flexible I/O structure.

FULL MILITARY AVAILABILITY
These logic arrays are available for applications requiring MIL-STD-883C Class B screening including burn-in. The thermal transfer characteristics of the device packaging, and with the low overall power dissipation, allows operation over the military temperature range of −55° to +125°C.

RADIATION HARD TECHNOLOGY
This series features a washed emitter ECL process which is one of the most radiation tolerant technologies in production.



PERFORMANCE SUMMARY	
PARAMETER	**VALUE**
Typical gate delay*	0.5 to 0.9 ns
Maximum I/O frequency	100 MHZ
TTL output drive	20 ma
ECL output drive	50Ω
Average cell utilization	85%
*Based on complex macro functions	

TABLE 1

DESCRIPTION

The AMCC Q700 series consists of the Q720, Q710 and Q700 Logic arrays providing equivalent densities of up to 250, 500 and 1000 gates respectively. The series is optimized to provide a system approach to high performance semi-custom applications. High speed ECL logic and proven reliability are combined with an advanced, interactive CAD system to provide a quick and cost effective solution to discrete I.C. replacement.

Each device shares a common Internal Logic and I/O macro library. The Q700 series utilize advanced series gating techniques providing both density and speed improvements over gate oriented and other macro oriented designs.

The Q700 logic arrays offer a wide range of standard packaging and support up to 76 I/O signals and 8 power supply connections.

RESOURCE SUMMARY			
DESCRIPTION	**Q700**	**Q710**	**Q720**
Approximate gate complexity	1000	500	250
Internal logic cells	208	120	56
Input cells	38	28	8
I/O cells	38	28	26
Typical power dissipation per cell in MW.	5-8	5-8	5-8
Typical total circuit power dissipation in Watts	1.8	1.2	0.75

TABLE 2

Q700 SERIES DIE LAYOUTS

Q700 — Die Size 236 Mils x 243 Mils

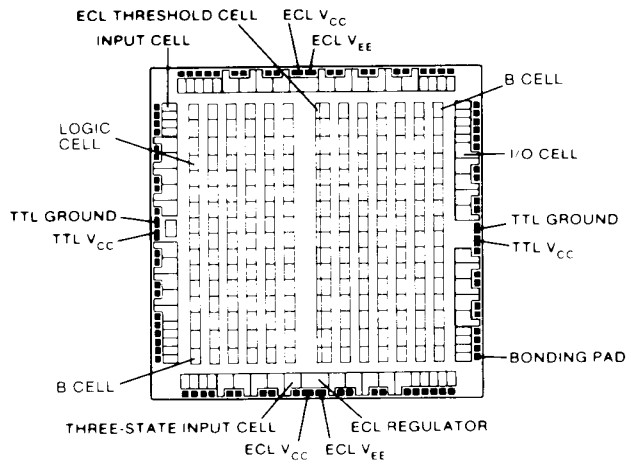


FIGURE 1

ARRAY STRUCTURE

The Q700 series logic arrays each have an internal structure comprised of 3 basic configurable cell types plus overhead logic such as voltage references, bias generators, and voltage regulators. The 3 configurable cell types are INPUT, I/O and INTERNAL LOGIC cells.

INTERNAL ARRAY

There are 208 internal logic cell positions for the Q700, 120 cells for the Q710, and 56 cells for the Q720. B cells occupy only the top and bottom rows in the internal array. Internal logic macros can be placed in either a Logic (L) or Buffer (B) cell, while ECL output buffer macros can only be placed in a B cell. Macro placement is performed automatically using AMCC CAD software. If a circuit requires critical timing considerations, these macros may be preplaced using interactive graphics.

TABLE 3
INTERNAL ARRAY CELL RESOURCE SUMMARY

	Q700	Q710	Q720
L Cells	182	100	42
B Cells	26	20	14
Total	208	120	56

The input and I/O cells are located around the periphery of the array and can be configured into many different combinations of circuit I/O. An INPUT CELL may be interconnected to form a TTL input or ECL input. An I/O cell may be interconnected to produce TTL or ECL input, output or bi-directional I/O.

Table 4 lists the available I/O resources for the Q700 series logic arrays. Each logic array requires a different number of power supply connections depending on the mode of operation.

Q710 — Die Size 195 mils x 197 Mils

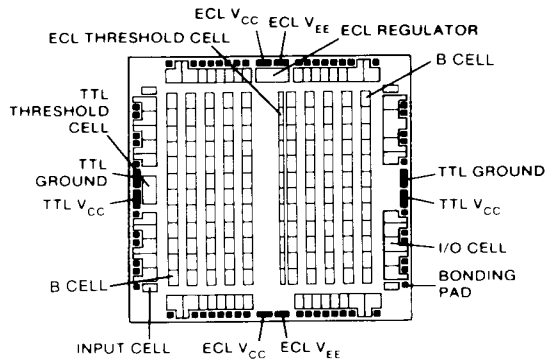


FIGURE 2

Q720 — Die Size 152 Mils x 148 Mils

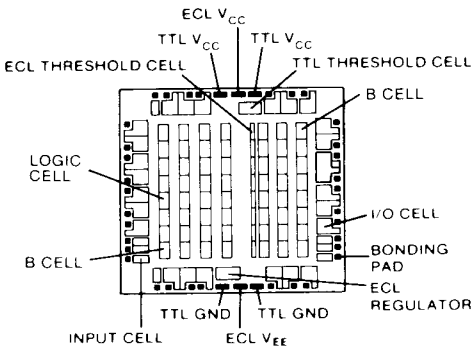


FIGURE 3

MODE	DESCRIPTION	Q700	Q710	Q720
TTL SYSTEMS	Input Cells (Max)	37*	27	8
	I/O Cells (Max)	38	28	26
	Dedicated 3-State Driver Cells	2	0	0
	V_{CC} (+5 V_{DC} nom.)	4	4	3
	Ground	5	5	3
ECL SYSTEMS	Input Cells (Max)	38*	28	8
	I/O Cells (Max)	38	28	26
	V_{EE} (−5.2 V_{DC} nom.)	2	2	1
	Ground	6	6	5
MIXED ECL/TTL SYSTEMS	Input Cells (Max ECL or TTL)	37*	27	8
	I/O Cells (Max ECL or TTL)	37	27	25
	3-State Driver Cells	2	0	0
	V_{CC} (+5V V_{DC} nom.)	3	3	3
	V_{EE} (−5.2V_{DC} nom.)	2	2	1
	TTL Ground	3	3	2
	ECL Ground	2	2	1

**Includes dedicated 3-state driver cells which are usable as simple inputs.*

TABLE 4
I/O RESOURCES

INTERNAL LOGIC CELL CAPABILITIES

The Q700 series logic arrays each have identically configured internal logic cells containing the components shown in Figure 4. These uncommitted cells are custom interconnected during metallization to provide the desired logic function defined by the macro library elements chosen.

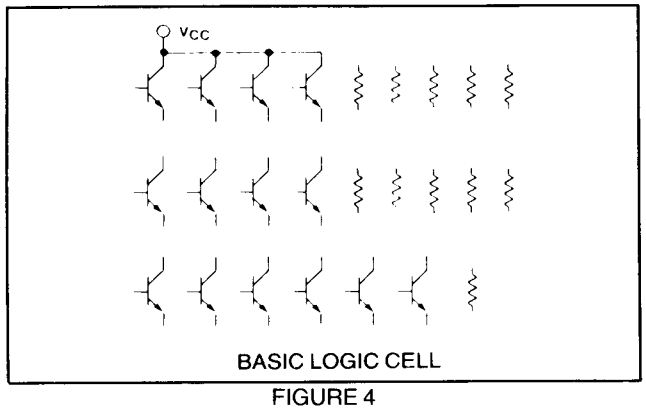


FIGURE 4

HIGH PERFORMANCE MACROS

Figure 5 shows the individual logic cell components configured as a 2 to 1 multiplexer, Figure 6 shows the multiplexer as configured in the library. To obtain high circuit density and performance, the circuit uses 2 level series gating; a technique which allows a second level of gating to be added to a macro without a significant increase in component count, circuit delay, or circuit power.

Many of the macros for the Q700 series arrays use series gating. Along with the I/O macros, they provide a powerful high speed library of circuit building blocks for virtually any circuit application.

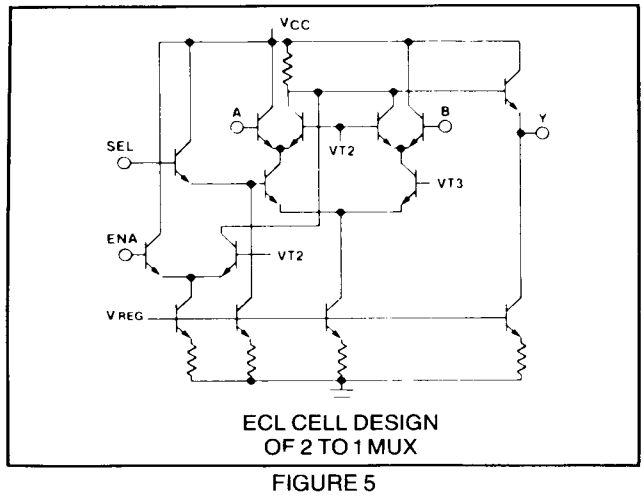


FIGURE 5

HIGH PERFORMANCE CIRCUIT DESIGN

The Q700 series internal macros have performance comparable to circuits designed with ECL 10K SSI and MSI logic devices. With the translation from TTL to ECL available directly on the Q700 series arrays, very high speed circuits can be realized with 100% TTL compatible I/O. Additionally, the mixed TTL/ECL capabilities allow the use of both technologies in a single design without the use of 10124 and 10125 ECL/TTL translators.

EASY TO USE MACRO LIBRARY

The Q700 series macro libraries are organized much like standard TTL or ECL logic catalogs. Figure 6 shows the 2 to 1 multiplexor as it is illustrated in the macro library. All the macros contained in the library are documented in a similar fashion, consisting of the type of macro, a functional description, and the speed and power requirements.

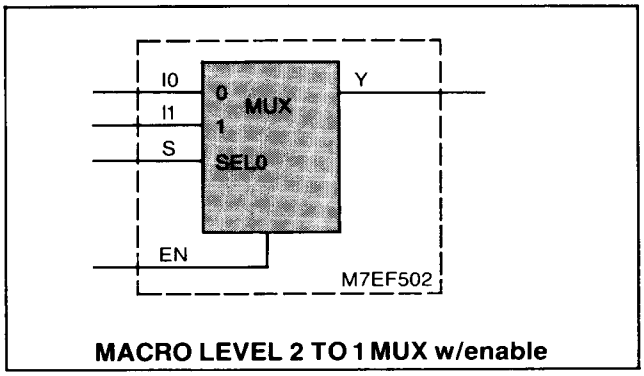


FIGURE 6

TYPICAL MACROS

The following macros are typical of those found in the INTERNAL LOGIC MACRO library. Each macro occupies one logic cell location and has its typical performance and power consumption specified. AMCC provides over 40 different INTERNAL LOGIC MACROS in the library, providing all the needed building blocks for complex logic design.

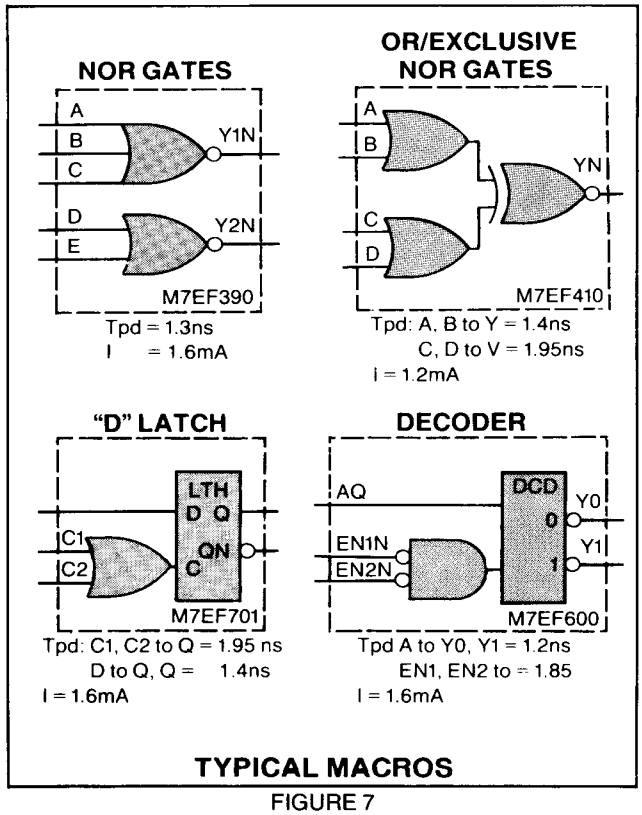


FIGURE 7

FLEXIBLE I/O CAPABILITY

The I/O structure of the Q700 series arrays has been designed to provide a very flexible I/O capability. The input cells are configurable to provide TTL input or ECL 10K input with either +5V or −5.2V DC power supply.

In addition to standard input cells, the Q700-1000 gate array has two special input cells which can also be used as high fanout 3-state enable drivers. These special drivers can directly drive up to 16 three-state enables, alleviating the need to use an I/O cell for 3-state enables in the Q700.

The I/O cells may be configured to operate in an input mode, output mode, or bi-directional I/O mode. In the input mode, the I/O cell operates identically to the I cell. When used in the output mode, the I/O cell can provide TTL totem pole output; TTL open collector output, or ECL 10K output capable of driving 200 ohms, 100 ohms, or 50 ohms.

The I/O cells can also be used to provide a driver for 3-state enables. When used in this manner, the I/O cell can be used with either internal or external signals and will drive up to 8 loads of 3-state enable.

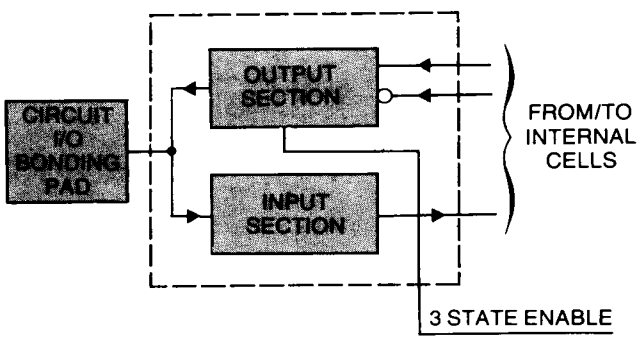
I CELL CAPABILITIES

The following modes of input are supported by the Q700 Series I cell.

- TTL compatible input
- ECL compatible input (V_{CC} = +5V V_{EE} = GND)
- ECL compatible input (V_{CC} = GND V_{EE} = −5.2V)
- 16 load 3-state driver (2 cells – Q700 only)

I/O CELL CAPABILITIES

Each I/O cell has two distinct sections which can be used independently or in combination.



The following I/O modes are supported:

INPUT ONLY
- TTL compatible INPUT
- ECL 10K compatible INPUT (V_{CC} = +5V V_{EE} = GND)
- ECL 10K compatible INPUT (V_{CC} = GND V_{EE} = −5.2V)
- External 3-state enable INPUT

OUTPUT ONLY
- TTL S/LS,TTL totem pole
- TTL OPEN COLLECTOR (.5V @ 20 mA IOL)
- ECL 10K @ 200 ohms, 100 ohms, 50 ohms (V_{CC} = 5V V_{EE} = GND)
- ECL 10K @ 200 ohms, 100 ohms, 50 ohms (V_{CC} = GND V_{EE} = −5.2V)
- Internal 3-state enable drive

BI-DIRECTIONAL I/O
- TTL LS/S TRANSCEIVER
- ECL 10K TRANSCEIVER (V_{CC} = GND V_{EE} = −5.2V)

DESIGN INTERFACE

The AMCC design interface has been structured to be highly flexible with respect to the customer's level of involvement. AMCC has developed an entire set of CAD tools providing an easy to understand, user-friendly interface.

AMCC CAD TOOLS

- Schematic capture
- Logic simulation
- Timing verifier
- Test vector generation with optional fault grading
- Auto place and route
- Design rule and interconnect verifier

These CAD tools provide the logic designer with the required support to design and develop a logic array from schematic diagrams through complete layout.

In addition to providing the required CAD to allow customer design of arrays, AMCC provides a number of services to support customer design.

AMCC PROVIDED SERVICES

- Logic conversion to AMCC macros
- Logic simulation with customer provided simulation vectors
- Custom macro development
- Hi-level engineering support

PACKAGING

The Q700 series logic arrays can be provided in a full variety of dual in-line, leaded and leadless chip carriers, and pin grid packages.

Pin Count	Package Type	Q720	Q710	Q700
24	DIP	•	•	
28	DIP	•	•	
40	DIP LCC	• •	• •	• •
44	LCC	•	•	•
48	DIP	•	•	•
64	FP LDCC		• •	• •
68	LCC PGA		• •	• •
84	FP PGA			• •

DIP—Dual In-line
LCC—Leadless Chip Carrier
FP—Flat Pack
LDCC—Leaded Chip Carrier
PGA—pin grid array

Q700 SERIES ECL MODE OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage (V_{EE}) V_{CC} = 0				
Military	−4.7	−5.2	−5.7	V
Commercial	−4.94	−5.2	−5.46	V
Input Signal Rise/Fall Time		2.0		nS
Junction Temperature				
Military			150	°C
Commercial			130	°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{EE}) V_{CC} = 0	−8.0 V DC
Input Voltage V_{CC} = 0	GND to V_{EE}
Output Source Current Continuous	−50 mA DC
Operating Temperature	−55°C (Ambient) to +125°C (Case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	−65°C to +150°C

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS V_{EE} = −5.2V[1]

	$T_{ambient}$				T_{case}	
	−55°C	0°C	25°C	75°C	125°C	UNIT
$V_{OH\,max}$	V_{CC}−850	V_{CC}−770	V_{CC}−730	V_{CC}−650	V_{CC}−575	mV
$V_{IH\,max}$	V_{CC}−800	V_{CC}−720	V_{CC}−680	V_{CC}−600	V_{CC}−525	mV
$V_{OH\,min}$	V_{CC}−1080	V_{CC}−1000	V_{CC}−980	V_{CC}−920	V_{CC}−850	mV
$V_{IH\,min}$	V_{CC}−1255	V_{CC}−1145	V_{CC}−1105	V_{CC}−1045	V_{CC}−1000	mV
$V_{IL\,max}$	V_{CC}−1510	V_{CC}−1490	V_{CC}−1475	V_{CC}−1450	V_{CC}−1400	mV
$V_{OL\,max}$	V_{CC}−1655	V_{CC}−1625	V_{CC}−1620	V_{CC}−1585	V_{CC}−1545	mV
$V_{OL\,min}$	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	V_{CC}−1980	mV
$V_{IL\,min}$	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	V_{CC}−2000	mV
$I_{in}H\,max$[2]	30	30	30	30	30	μA
$I_{in}L\,min$[2]	.5	.5	.5	.5	.5	μA

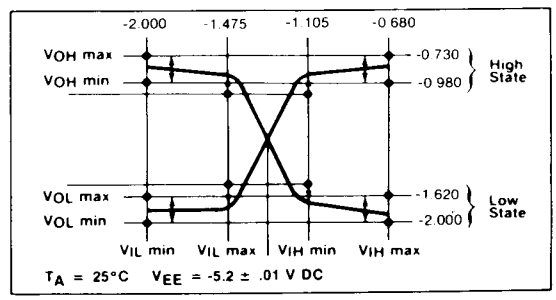
NOTES:
1. Data measured at thermal equilibrium. For +5V ref. ECL V_{CC} = +5.0V
2. Per fan-in

DEDICATED AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMM 0° C/+ 75° C			MIL-55° C/+ 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{IPD}	Input Propagation Delay through buffer			1.6			1.6		nS
t_{OPD}	Output Propagation Delay including buffer	C_L = 5 pf 50Ω to −2V		2.95			2.95		nS
t_{FPD}	Internal Equivalent Gate Delay[1]			0.9			0.9		nS
F_{MAXE}	Max. Internal Flip-Flop Toggle Frequency			250			250		MHz

NOTES:
1. Logic cell delays are for each gating level of a more complex logic function (i.e. D flip/flop, 4 to 1 mux, etc.)

INPUT/OUTPUT SWITCHING CHARACTERISTICS



Q700 SERIES TTL MODE OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC}) Military Commercial	 4.5 4.75	 5.0 5.0	 5.5 5.25	 V V
Output Current Low (IOL) Military Commercial			 20 20	 mA mA
Operating Temperature Military Commercial	 -55 (ambient) 0 (ambient)		 + 125 (case) 70 (ambient)	 °C °C
Junction Temperature T_J Military Commercial			 150 130	 °C °C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}),V_{EE} = 0	7.0V
Input Voltage	5.5V
Operating Temperature	– 55°C (Ambient) to + 125°C (Case)
Junction Temperature (Operating)	150°C
Storage Temperature	– 65°C to + 150°C

INPUT/OUTPUT DC CHARACTERISTICS

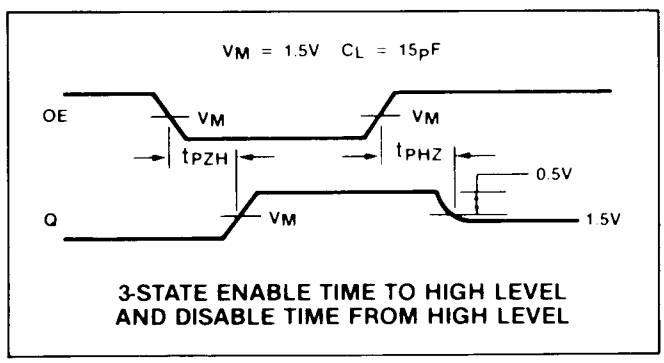
SYMBOL	PARAMETER	TEST CONDITIONS	COMM'L 0°/+70°C			MIL -55°/+125°C			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
V_{IH}[2]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			2.0			V
V_{IL}[2]	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = – 18mA		-.65	-1.2		-.65	-1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = – 1mA	2.7	3.4		2.4	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 4mA			0.4			0.4	V
		I_{OL} = 20mA			0.5			0.5	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V	-145		145	-145		145	µA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V	-145		145	-145		145	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V			50			50	µA
I_I	Input HIGH current at Max input voltage	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V			-0.4			-0.4	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0.5V	-30		-100	-30		-100	mA
I_{CC}[3]	Supply current Q700	V_{CC} = Max, 85% utilization		350			350		mA
	Supply current Q710			220			220		mA
	Supply current Q720			150			150		mA

NOTES:
1. Typical limits are at 25°C, V_{CC} = 5.0V
2a. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
2b. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
3. Maximum power supply currents vary with each circuit design implemented and can only be determined after macro level circuit designs are complete.

Q700 SERIES TTL MODE OPERATING CONDITIONS

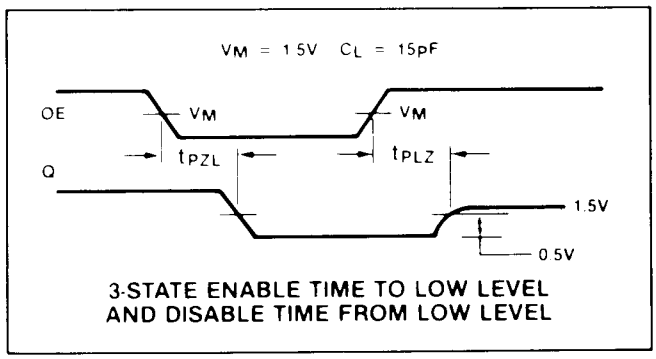
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMM 0°/+75°C			MIL 55°/+125°C			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{IPD}	Input propagation delay through input buffer			3.3			3.3		nS
t_{OPD}	Output propagation delay (I/O cell)	R_L = 280Ω , C_L = 15 pF Load[2]		6.6			6.6		nS
$t_{FPD'}$	Internal equivalent gate delay			.9			.9		nS
F_{MAXT}	Max internal flip/flop toggle frequency			250			250		MHz
t_{PZH}	Enable time to high level	Figure 8 3-state output		6.0			6.0		nS
t_{PZL}	Enable time to low level	Figure 9 3-state output		9.0			9.0		nS
t_{PHZ}	Disable time from high level	Figure 8 3-state output		6.0			6.0		nS
t_{PLZ}	Disable time from low level	Figure 9 3-state output		9.0			9.0		nS



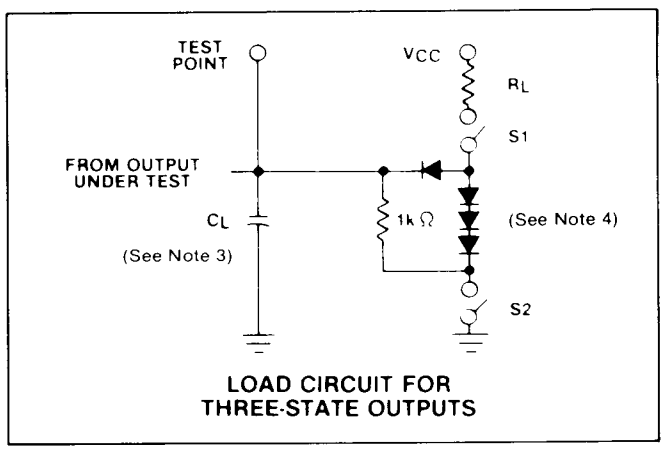
3-STATE ENABLE TIME TO HIGH LEVEL
AND DISABLE TIME FROM HIGH LEVEL

FIGURE 8



3-STATE ENABLE TIME TO LOW LEVEL
AND DISABLE TIME FROM LOW LEVEL

FIGURE 9



LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

FIGURE 10

TEST CIRCUIT SWITCH TABLE

TEST FUNCTIONS	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

NOTES:
1. Logic cell delays are for each gate level of a more complex logic function (i.e. D flip/flop, 4 to 1 mux, etc.)
2. Standard TTL load circuit used, see Figure 10 (S1 and S2 closed)
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or 1N3064.

NOTES:

REPRESENTED BY:

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