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Short Form Specification

Near Field Communication PN531- µC based Transmission module

Objective Short Form Specification

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Revision 2.0

Public

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CONTENTS

1 INTRODUCTION

1.1 Scope

The PN531 is a highly integrated transmission module for contactless communication at 13.56 MHz including µ-controller functionality based on an 80C51 core with 32 kbyte of ROM and 1 kbyte of RAM. This µc-based transmission module combines an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz with an easy to use firmware for the different supported modes and the required host interfaces.

The embedded firmware handles the ISO 14443A and MIFARE® reader protocol as well as the basic FeliCa™ reader protocol and the complete NFC IP-1 protocol.
Furthermore the embedded firmware and the internal hardware support the handling and the host protocols for the different interfaces as

- USB 2.0
- I2C
- SPI and
- Serial UART

The PN531 supports 3 different operating modes

- Reader/writer mode for FeliCa™ and ISO14443A cards
- Supports Card interface mode for FeliCa™ and ISO14443A/MIFARE® in combination with secure µC
- NFC IP-1 mode

In reader/ writer mode the PN531's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO14443A /MIFARE® or FeliCa™ cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO14443A compatible cards and transponders. The digital part handles the complete ISO14443A framing and error detection (Parity & CRC).

The PN531 supports MIFARE® Classic (e.g. MIFARE® Standard) products. The PN531 supports contactless communication using MIFARE® Higher Baudrates up to 424kbit/s in both directions. In the reader/ writer mode the PN531 transmission module supports the FeliCa™ communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa™ coded signals. The digital part handles the FeliCa™ framing and error detection like CRC.

The PN531 supports contactless communication using FeliCa™ Higher Baudrates up to 424kbit/s in both directions.

In card mode the PN531 is able to answer a reader/writer command either in FeliCa™ or ISO14443A/MIFARE® card mode. The PN531 generates the proper digital load modulated signals and with an external circuit, can respond to commands sent by the reader/writer.

The PN531 offers the possibility to directly communicate with several NFC enabled devices in the NFC IP-1 mode. The NFC IP-1 mode offers different baudrates up to 424kbit/s. The PN531 handles the complete NFC framing and error detection.

1.1 Features

- 80C51 microcontroller core with 32 kbyte ROM and 1 kbyte RAM
- Highly integrated analog circuitry for transmission and reception
- Output drivers to connect an antenna with minimum number of external components
- Integrated RF Level detector
- Integrated mode detector
- Hardware and embedded Firmware support for
    - ISO 14443A reader/writer mode
    - MIFARE® Classic encryption and MIFARE® higher baudrate communication up to 424 kbit/s
    - Contactless communication according to the FeliCa™ scheme at 212 kbit/s and 424 kbit/s
    - NFC standard ECMA 340 and ISO 18092: NFC IP-1 interface and protocol
    - Host protocol on following interfaces
        - USB 2.0 full speed compliant device
        - SPI
        - I2C
        - High speed serial UART
- Optional interrupt line to the host
- Hard reset with low power function
- Flexible Power down mode or power reduction mode per software
- Internal oscillator to connect a 27.12 MHz quartz
- Internal oscillator to connect a 4 MHz quartz for the USB interface
- 2.5 - 3.6 V power supply
- USB bus powered (In USB mode)
- Specific IO ports and interrupt sources for external devices control

1.2 Application

The PN531 is tailored to fulfil the requirements of various applications using contactless communication based on the ECMA340 (NFC IP-1) Interface and protocol standard, the ISO14443A reader and FeliCa reader protocol. NFC IP-1 is also standardised in ISO/IEC 18092.
Compatible to current RFID infrastructure the NFC technology offers a new direct communication link between two NFC enhanced devices. This peer-to-peer communication enables a direct data exchange between devices.
The integrated microcontroller and embedded firmware of the PN 531 means a fast and easy integration in a contactless system. The high-level abstraction commands and the complete handling of RF communication protocols free the host CPU of all real time related constraints.

NFC technology is designed to meet requirements for consumer markets, as well as handheld and PC markets.

Typical devices to integrate the PN531 are

- Mobile phones
- PDAs
- PCs
- Intelligent remote controls
- PC peripherals e.g. printers and mice
- Consumer electronic devices like digital cameras

2 BLOCK DIAGRAM

2.1 Simplified PN531 Block Diagram

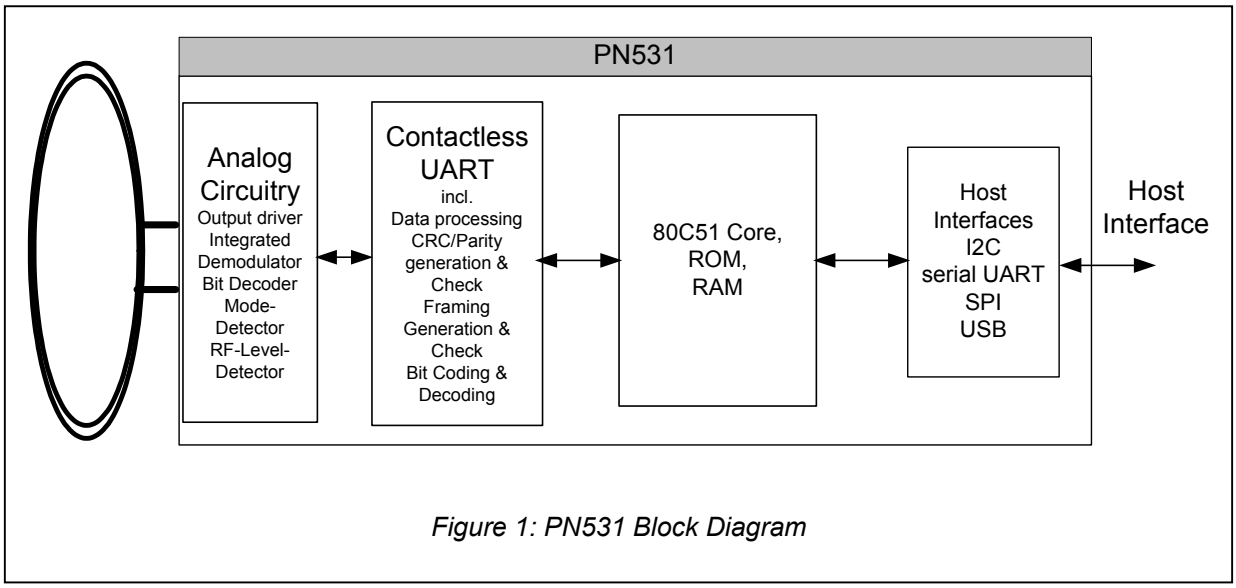

Figure 1: PN531 Block Diagram

The Analog circuitry handles the modulation and demodulation of the analog signals according to the card mode, reader /writer mode and NFC mode communication scheme.

The RF level detector detects the presence of an external RF field at 13.56 MHz.

The mode detector detects a MIFARE®, FeliCa™ or NFC coding of an incoming signal in order to prepare the internal receiver to demodulate signals that are sent to the PN531.

The integrated contactless UART and the firmware handle the protocol requirements for the communication schemes including the RF based protocols as well as the protocols for host communication.
The microcontroller with its embedded firmware allows autonomous management of communication both on the RF interface and with the host.

Various host interfaces are implemented to fulfil different customer requirements.

3 PN531 PINNING INFORMATION

3.1 Pinning Diagram

The device is available in an HVQFN40 package.

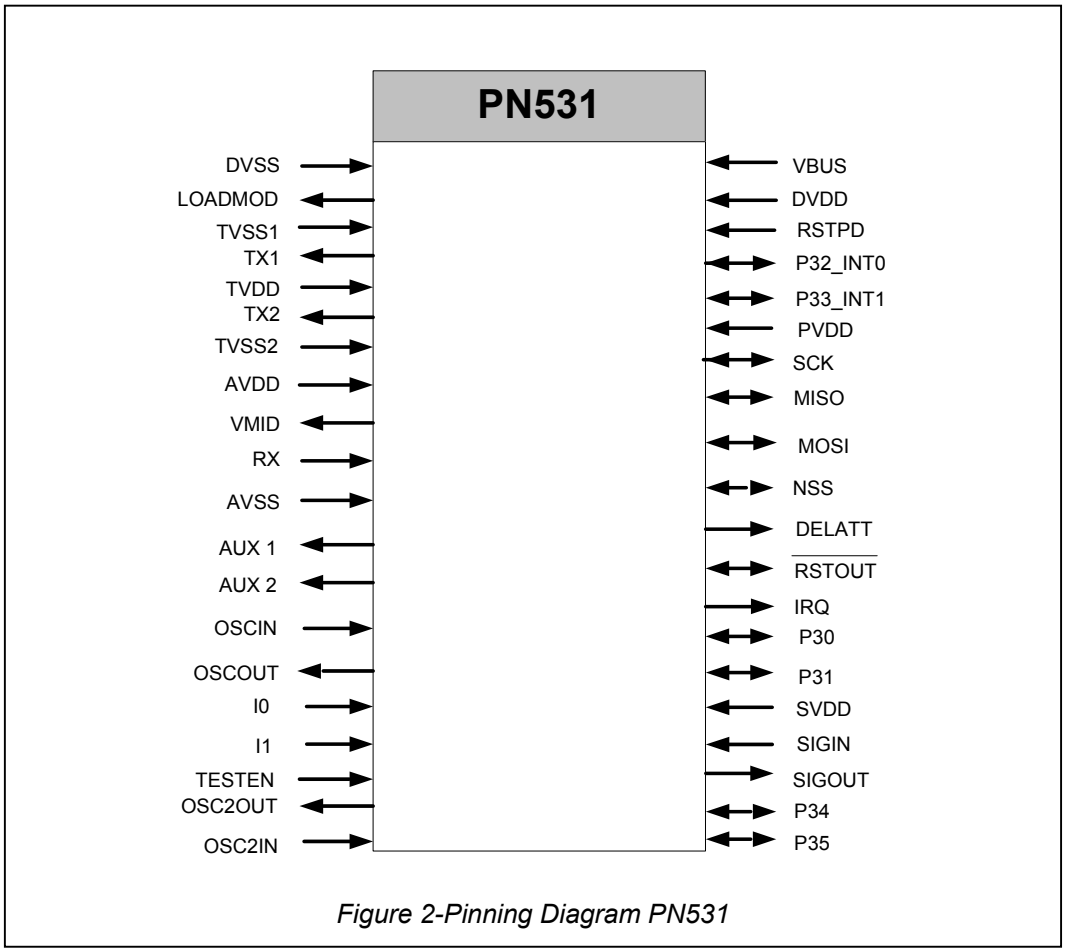

Figure 2-Pinning Diagram PN531

The device operates with six individual power supplies for best performance in terms of EMC behaviour and signal de-coupling. This gives outstanding RF performance and maximum flexibility to adapt to different operating voltages of digital and analog parts.

3.2 Pin Description

Pin	Symbol	Type	Pad Ref Voltage	Description
1	DVSS	PWR		Digital Ground
2	LOADMOD	O	DVDD	Load Modulation output provides digital signal for FeliCa and MIFARE® card operating mode
3	TVSS1	PWR		Transmitter Ground: supplies the output stage of TX1 and TX2
4	TX1	O	TVDD	Transmitter 1: delivers the modulated 13.56 MHz energy carrier
5	TVDD	PWR		Transmitter power supply: supplies the output stage of TX1 and TX2
6	TX2	O	TVDD	Transmitter 2: delivers the modulated 13.56 MHz energy carrier
7	TVSS2	PWR		Transmitter Ground: supplies the output stage of TX1 and TX2
8	AVDD	PWR		Analog Power Supply
9	VMID	PWR	AVDD	Internal Reference Voltage: This pin delivers the internal reference voltage.
10	RX	I	AVDD	Receiver Input: Input pin for the reception signal, which is the load modulated 13.56 MHz energy carrier from the antenna circuit.
11	AVSS	PWR		Analog Ground
12	AUX1	O	DVDD	Auxiliary Output: This pin delivers analog and digital test signals.
13	AUX2	O	DVDD	Auxiliary Output: This pin delivers analog and digital test signals.
14	OSCIN	I	AVDD	Crystal Oscillator Input: input to the inverting amplifier of the oscillator. This pin is also the input for an externally generated clock (fosc = 27.12 MHz).
15	OSCOUT	O	AVDD	Crystal Oscillator output: Output of the inverting amplifier of the oscillator.
16	I0	I	DVDD	Interface mode lines: selects the used host interface. In test mode I0 is used as test signals.
17	I1	I	DVDD	Interface mode lines: selects the used host interface. In test mode I0 is used as test signals.
18	TESTEN	I	DVDD	Test enable pin: When set to 1 enable the test mode. When set to 0 reset the TCB and disable the access to the test mode.
19	OSC2OUT	O	DVDD	Crystal Oscillator output: Output of the inverting amplifier of the oscillator for the USB clock.
20	OSC2IN	I	DVDD	Crystal Oscillator Input: input to the inverting amplifier of the oscillator for the USB clock generation. This pin is also the input for an externally generated clock (f_{osc} =4 MHz). In test mode this signal is used as test clock input
21	P35	IO	DVDD	General purpose IO signal
22	P34	IO	SVDD	General purpose IO signal or clk signal for the SAM
23	SIGOUT	O	SVDD	Contactless communication interface output: delivers a serial data stream according to NFCIP-1 and output signal for the SAM. In test mode this signal is used as test signal output.
24	SIGIN	I	SVDD	Contactless communication interface input: accepts a digital, serial data stream according to NFCIP-1 and input signal from the SAM. In test mode

Pin	Symbol	Type	Pad Ref Voltage	Description
				this signal is used as test signal input.
25	SVDD	PWR		Connected to SAM power supply; used as a reference for communication with the SAM.
26	P31	IO	PVDD	General purpose IO signal. Can be configured to act either as TX line of the second serial interface or general purpose IO. In test mode this signal is used as input and output test signal.
27	P30	IO	PVDD	General purpose IO signal. Can be configured to act either as RX line of the second serial interface or general purpose IO. In test mode this signal is used as input and output test signal.
28	IRQ	O	PVDD	Interrupt request: Output to signal an interrupt event to the host (Port 7 bit 0)
29	RSTOUT	IO	PVDD	Output reset signal. When Low it indicates that the circuit is in reset state.
30	DELATT	O	PVDD	Optional output for an external 1.5 KOhms resistor connection on D+.
31	NSS	IO	PVDD	Not Slave Select. In test mode this signal is used as input and output test signal.
32	MOSI	IO	PVDD	Master Out Slave In. In test mode this signal is used as input and output test signal
33	MISO	IO	PVDD	Master In Slave Out. In test mode this signal is used as input and output test signal
34	SCK	IO	PVDD	Serial interface clock. In test mode this signal is used as input and output test signal
35	PVDD	PWR		Pad power supply
36	P33_INT1	IO	PVDD	General purpose IO signal. Can be used to generate an HZ state on the output of the selected interface for the Host communication and to enter TAMA into power down mode without resetting the internal state of TAMA. In test mode this signal is used as input and output test signal.
37	P32_INT0	IO	PVDD	General purpose IO signal. Can also be used as an interrupt source In test mode this signal is used as input and output test signal.
38	RSTPD	I	PVDD	Reset and Power Down: When High, internal current sources are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
39	DVDD	PWR		Digital Power Supply
40	VBUS	PWR		USB power supply.

4 OPERATING MODES

PN531 supports the following operating modes:

- Reader/Writer mode supporting ISO14443A/MIFARE® and FeliCa™ scheme
- Card Operating mode supporting ISO14443A/MIFARE® and FeliCa™ scheme
- NFC mode including 106, 212 and 424kbit/s.

The modes support different baudrates and modulation schemes. The following chapters will explain the different modes in more detail.

4.1 Reader/Writer Operating mode

The PN531 can act as a reader / writer for ISO14443A/MIFARE® or FeliCa™ cards.

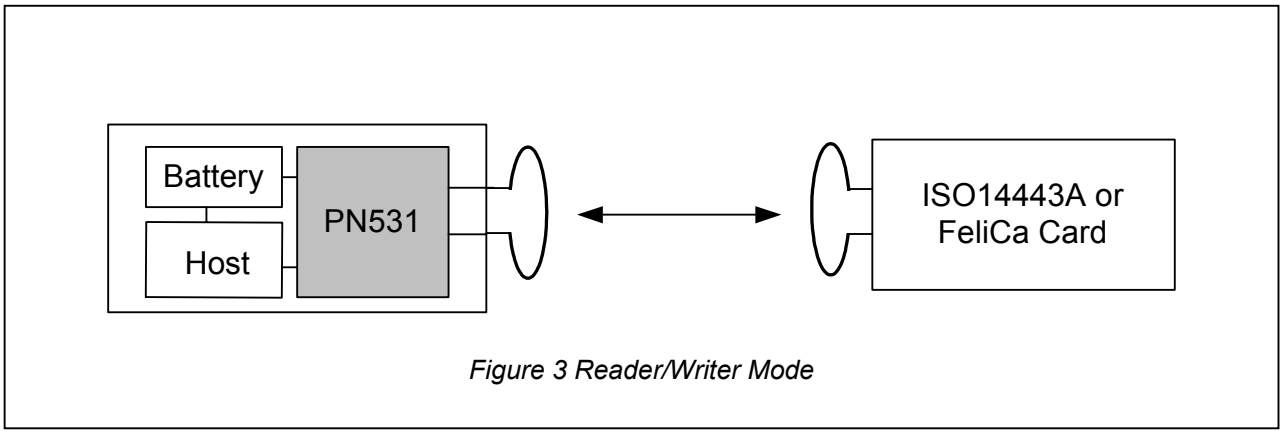

Figure 3 Reader/Writer Mode

In the reader/ writer mode the PN531 enables communication to a passive ISO14443A/MIFARE® or FeliCa™ card.

The PN531's firmware and contactless UART handle the ISO 14443A/MIFARE® and FeliCa™ protocol.

4.2 NFC MODE

NFC communication differentiates between an active and a passive communication.

- Active NFC Mode means both the initiator and the target are using their own RF field for the communication.
- Passive NFC Mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active i.e. generating the RF field.

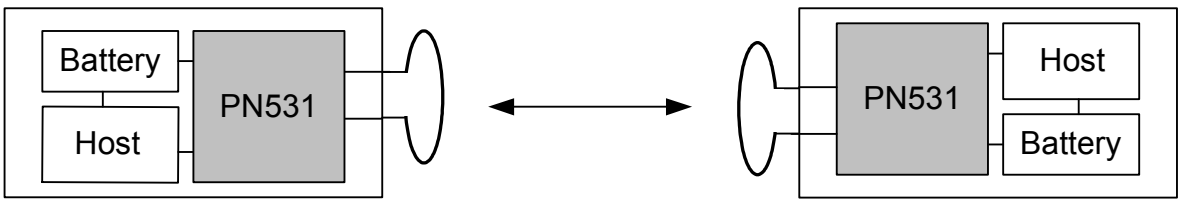

Figure 4 NFC Mode

- Initiator: generates RF field @ 13.56 MHz and starts the NFC communication
- Target: responds to initiator commands either using load modulation scheme (RF field continuously generated by Initiator) or using modulation of self generated RF field (no RF field generated by initiator)

4.2.1 ACTIVE NFC MODE

Active NFC Mode means both the initiator and the target use their own RF field to enable the communication.

- Communication Diagrams for active NFC communication

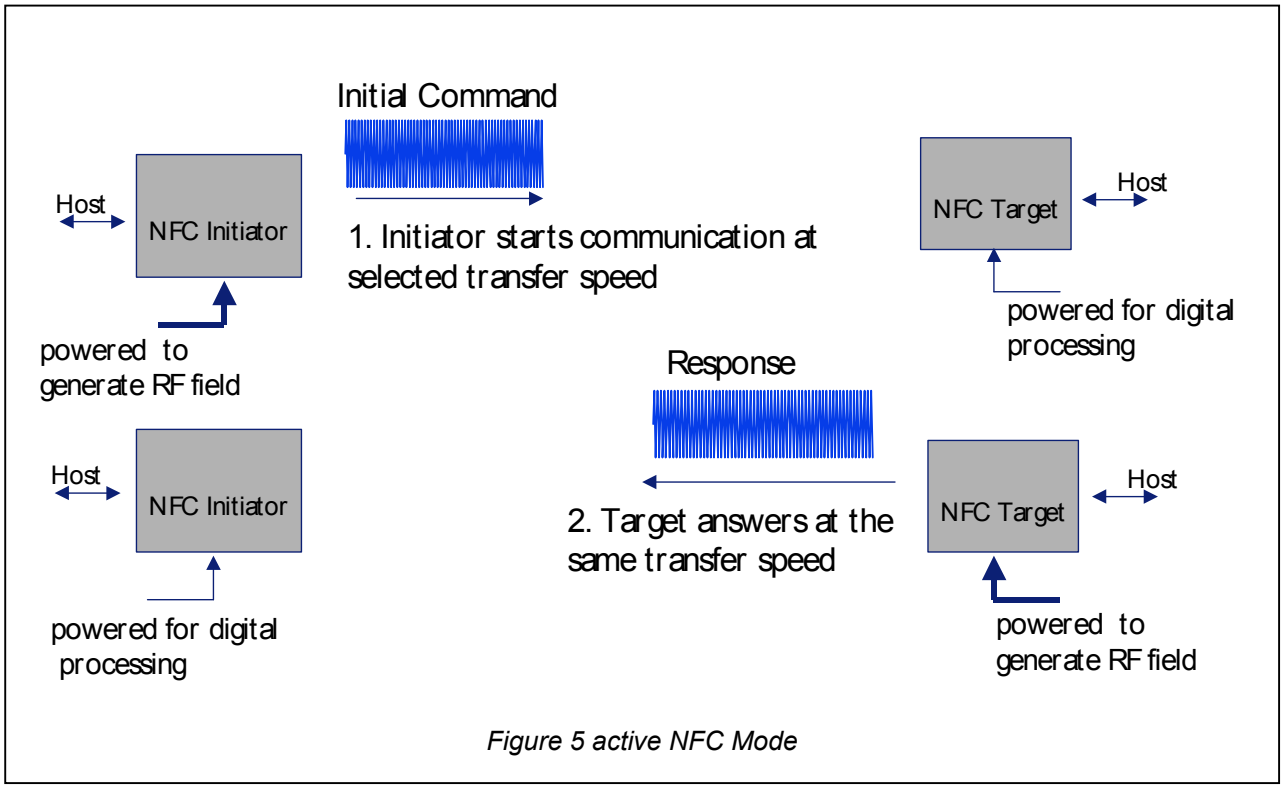

Figure 5 active NFC Mode

The PN531's firmware and contactless UART handle the NFC protocol.

4.2.2 PASSIVE NFC MODE

Passive NFC Mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active i.e. generating the RF field.

- Communication Diagrams for passive NFC communication

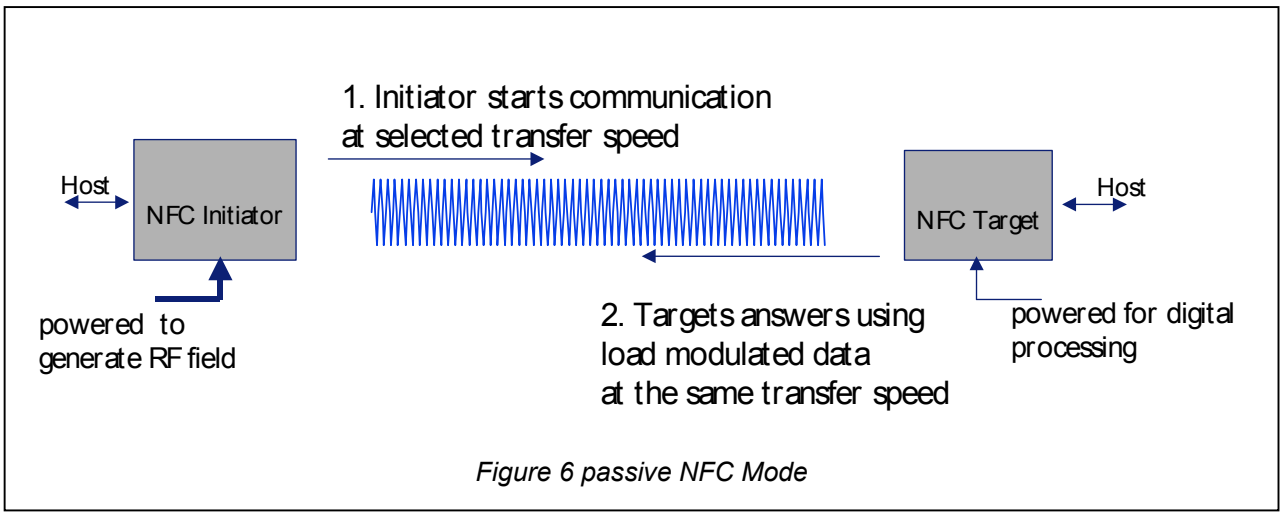

Figure 6 passive NFC Mode

The PN531's firmware and contactless UART handle the NFC protocol.

4.3 Card Operating mode

The PN531 can be addressed like a FeliCa™ or ISO14443A/ MIFARE® card. This means that the PN531 in combination with a secure µC may acts as an ISO14443A /MIFARE® or FeliCa™ card.

- Communication diagram

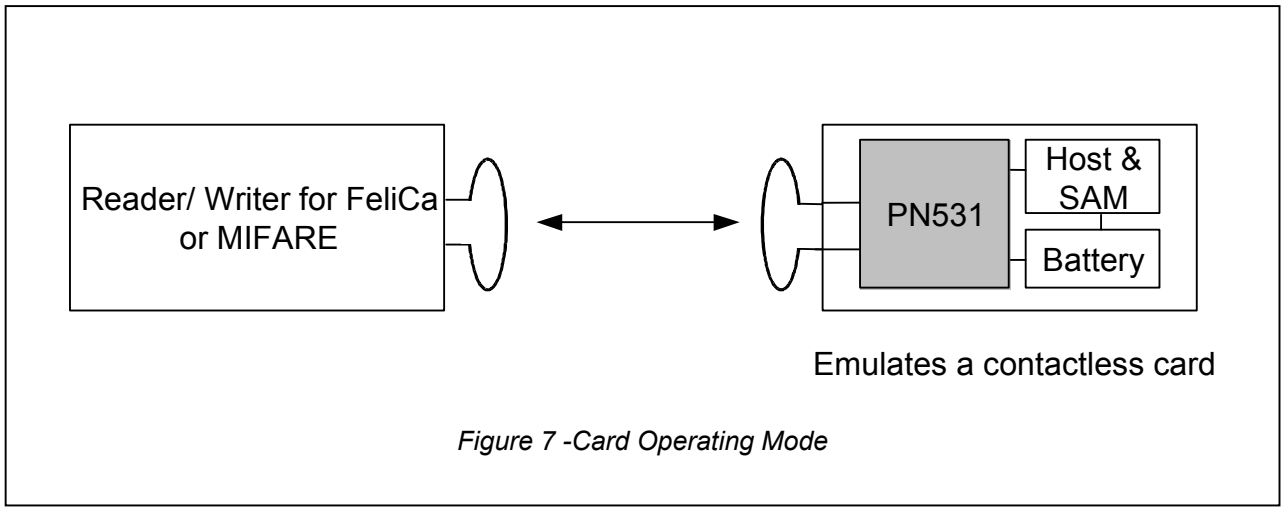

Figure 7 -Card Operating Mode

5 TYPICAL APPLICATION

5.1 Circuit Diagram

5.1.1 CIRCUIT BASED ON SPI, SERIAL UART OR I2C HOST INTERFACE

The figure below shows a typical application, where the antenna is directly connected to the PN531. The used host interface is SPI, Serial UART or I2C.

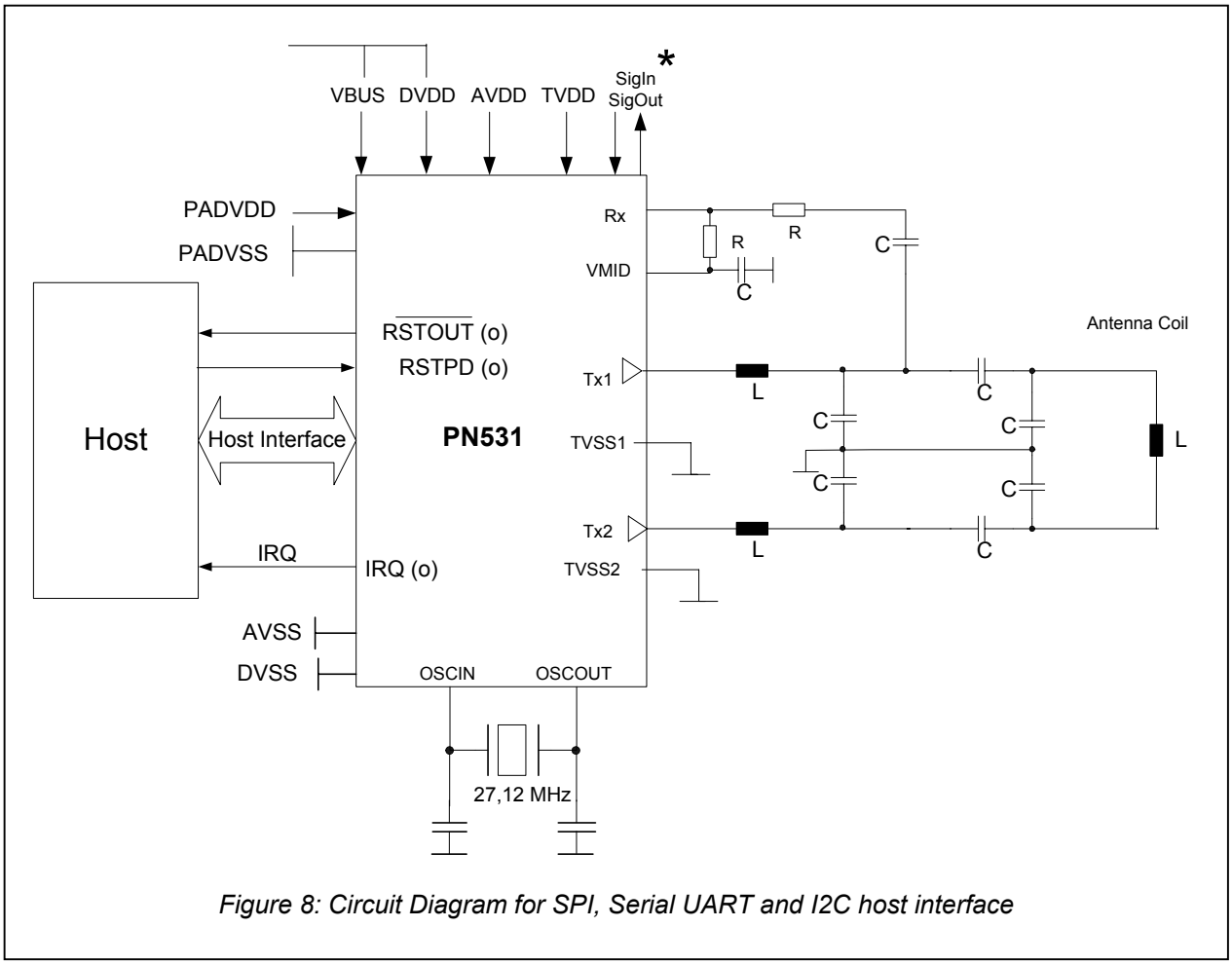

Figure 8: Circuit Diagram for SPI, Serial UART and I2C host interface

Note:

1. * Can be used in the card operating mode to connect to SAM

2. (o) Optional

5.1.2 CIRCUIT BASED ON USB HOST INTERFACE

The figure below shows a typical application where the antenna is directly connected to the PN531. The host interface is USB.

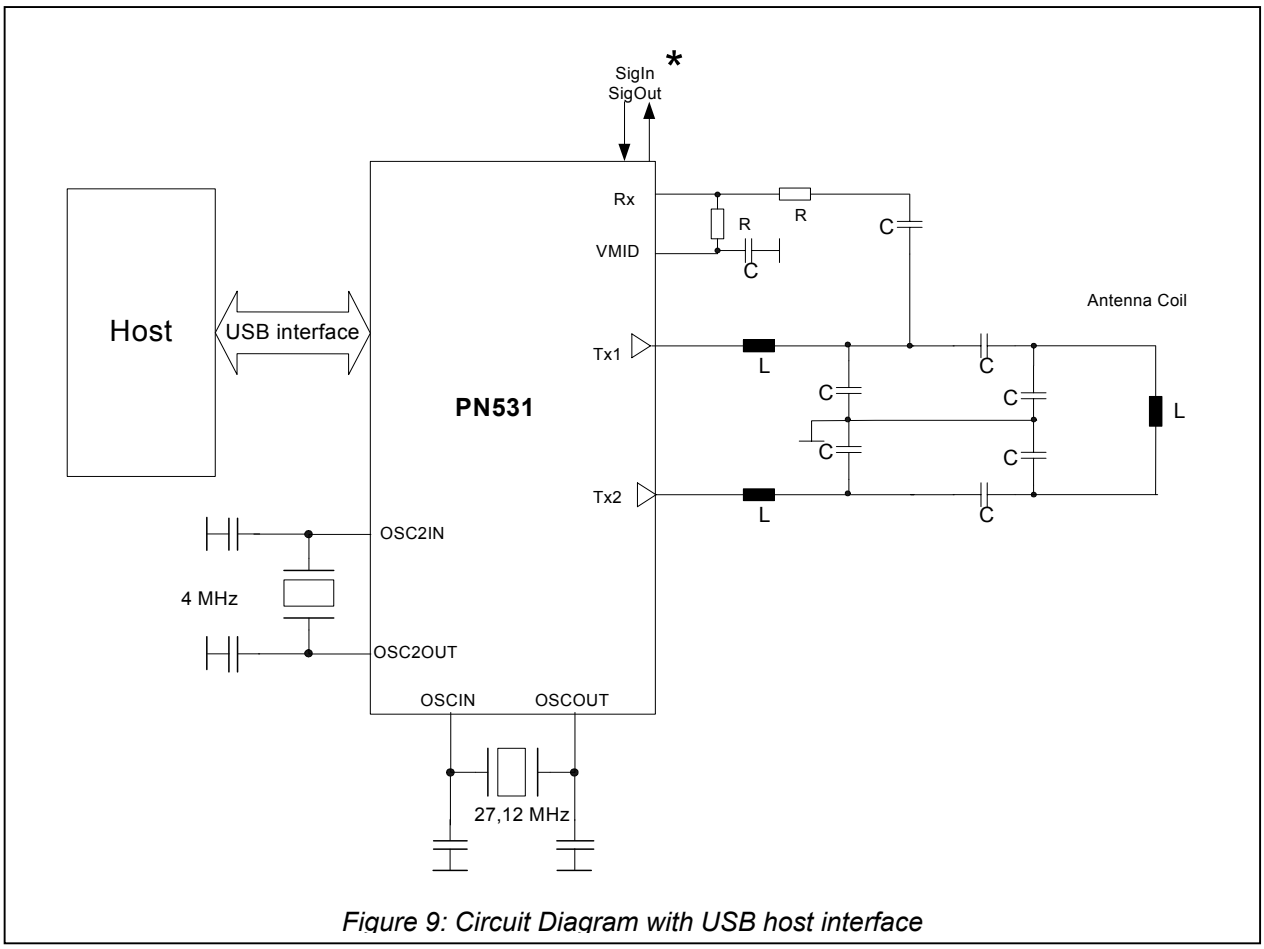

Figure 9: Circuit Diagram with USB host interface

Note:

1. * Can be used for the card operating mode to connect to SAM

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Continuous Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
AVDD DVDD PVDD SVDD TVDD	Supply Voltages	-0.5	4.0	V
VBUS	USB Supply Voltage	-0.5	5.5	V

Table 6-1: Absolute Maximum Continuous Ratings

6.2 Operating Condition Range

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Tamb	Ambient Temperature		-30	+25	+85	°C
VBUS	USB Supply Voltage (USB mode)	VSS = 0V	4.2	5	5.25	V
	Supply Voltage (Non USB mode)	VBUS= DVDD VSS = 0V	2.5	3.3	3.6	V
TVDD, AVDD, DVDD	Supply Voltages	TVDD= AVDD= DVDD VSS = 0V	2.5	3.3	3.6	V
PVDD	Supply Voltage for host interface	VSS = 0V	1.6	1.8 – 3.3	3.6	V
SVDD	Supply Voltage for SAM interface	VSS = 0V	1.6	1.8 – 3.3	3.6	V

Table 6-2: Operating Condition Range

Note:

1. TVDD<3V reduces the performance (e.g. the achievable operating distance).
2. VSS represents DVSS, AVSS, TVSS1 and TVSS2

6.3 Current Consumption

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{HPD}	Hard Power Down Current (Not powered from USB)	AVDD=DVDD=TVDD=PVDD=SVDD=3V, RF level detector off			10	µA
I_{SPD}	Soft Power down Current (Not powered from USB)	AVDD=DVDD=TVDD=PVDD=SVDD=3V, RF level detector on			30	µA
I_{supend}	USB suspend Current	AVDD=DVDD=TVDD=PVDD=SVDD=3V, RF level detector on (without resistor on D+/D-)			250	µA
I_{DVDD}	Digital Supply Current	AVDD=DVDD=TVDD=PVDD=SVDD=3V, RF level detector on		15		mA
I_{AVDD}	Analog Supply Current	AVDD=DVDD=TVDD=PVDD=SVDD=3V, RF level detector on		6	tbd	mA
	Analog Supply Current	AVDD=DVDD=TVDD=PVDD=SVDD=3V, RF level detector off		3	tbd	mA
I_{PVDD}	Pad Supply Current				tbd	mA
I_{SVDD}	Pad Supply Current for SAM interface				tbd	mA
I_{TVDD}	Transmitter Supply Current	Continuous Wave, TVDD=3V		60	100	mA

Table 6-3: Current Consumption

Note:

1. TVDD depends on TVDD and the external circuitry connected to Tx1 and Tx2.
2. DVDD depends on the system configuration.
3. PVDD depends on the overall load at the digital pins.
4. SVDD depends on the overall load at the digital pins.
5. During operation with a typical circuitry the overall current is below 100 mA. Typical value using a complementary driver configuration and an antenna matched to 40 Ohm between TX1 and TX2 at 13.56 MHz.

7 REVISION HISTORY

REVISION	DATE	DESCRIPTION
2.0	February 2004	Second published version, change to public
1.0	April2003	First published version

Table 7: Document Revision History

8 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

9 LIFE SUPPORT APPLICATIONS

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