12-BIT, 170 MSPS ADC WITH DDR LVDS/CMOS OUTPUTS

FEATURES

- **Maximum Sample Rate: 170 MSPS**
- **12-Bit Resolution**
- **No Missing Codes**
- **Total Power Dissipation 1.1 W**
- **Internal Sample and Hold**
- **69.5-dBFS SNR at 70-MHz IF**
- **82-dBc SFDR at 70-MHz IF, 0 dB gain**
- **Double Data Rate (DDR) LVDS and Parallel CMOS Output Options**
- **Programmable Gain up to 6 dB for SNR/SFDR Trade-Off at High IF**
- **Reduced Power Modes at Lower Sample Rates**
- **Supports input clock amplitude down to 400 mV_{PP}**
- **Clock Duty Cycle Stabilizer**
- **No External Reference Decoupling Required**
- **Internal and External Reference Support**
- **Programmable Output Clock position to ease data capture**
- **3.3-V Analog and Digital Supply**
- **48-QFN Package (7 mm × 7 mm)**

APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**
- **802.16d/e**
- **Test and Measurement Instrumentation**
- **High Definition Video**
- **Medical Imaging**
- **Radar Systems**

DESCRIPTION

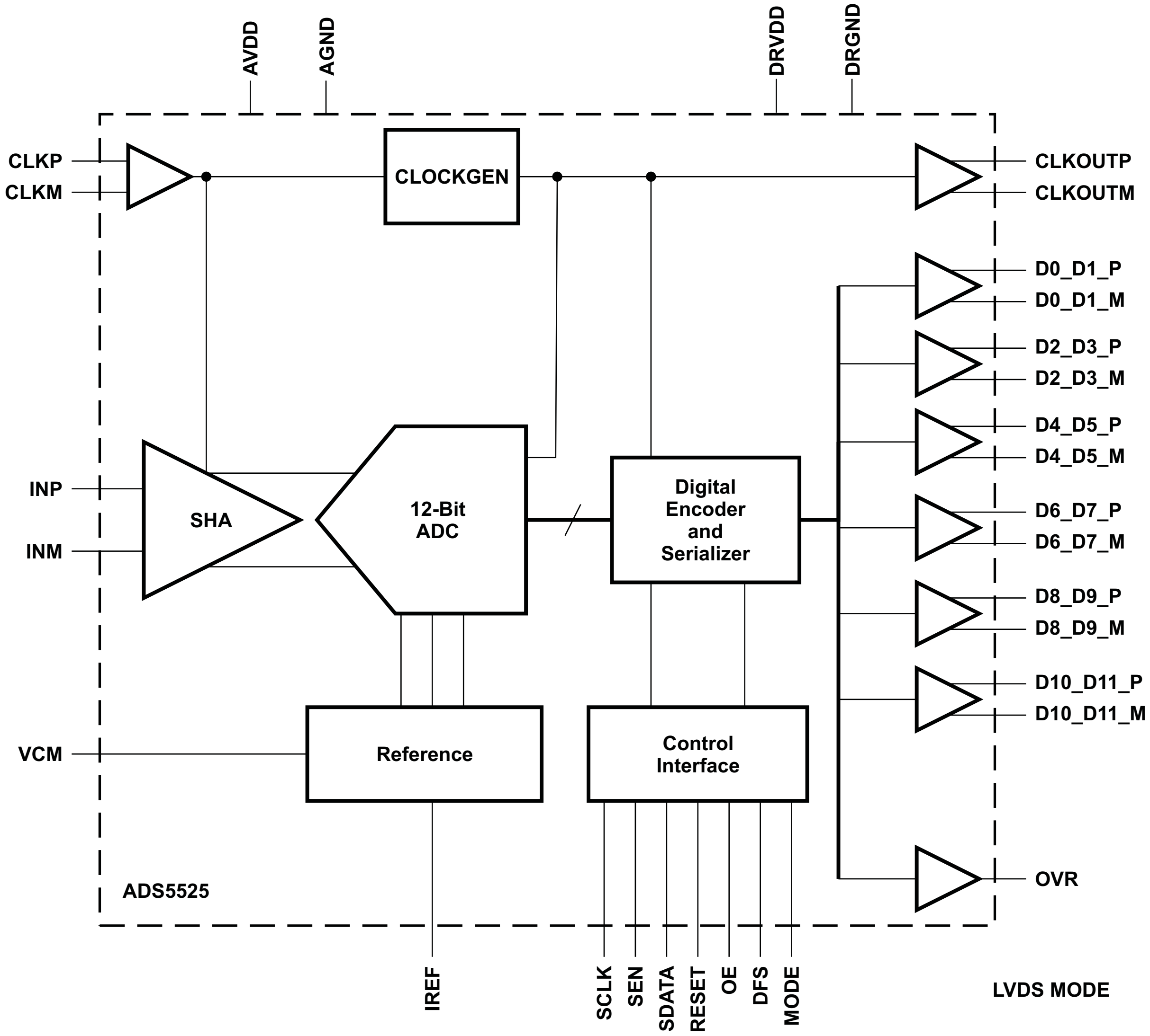
ADS5525 is a high performance 12-bit, 170-MSPS A/D converter. It offers state-of-the art functionality and performance using advanced techniques to minimize board space. Using an internal sample and hold and low jitter clock buffer, the ADC supports both high SNR and high SFDR at high input frequencies. It features programmable gain options that can be used to improve SFDR performance at lower full-scale analog input ranges.

In a compact 48-pin QFN, the device offers fully differential LVDS DDR (Double Data Rate) interface while parallel CMOS outputs can also be selected. Flexible output clock position programmability is available to ease capture and trade-off setup for hold times. At lower sampling rates, the ADC can be operated at scaled down power with no loss in performance. ADS5525 includes an internal reference, while eliminating the traditional reference pins and associated external decoupling. The device also supports an external reference mode.

The device is specified over the industrial temperature range (-40°C to 85°C).

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and



PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5525	QFN-48[2]	RGZ	–40°C to 85°C	AZ5525	ADS5525IRGZT	Tape and Reel, 250
					ADS5525IRGZR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. θ_{JA} = 25.41°C/W (0 LFM air flow), θ_{JC} = 16.5°C/W when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in x 3 in PCB.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Supply voltage range, AVDD	–0.3 V to 3.9	V
	Supply voltage range, DRVDD	–0.3 V to 3.9	V
	Voltage between AGND and DRGND	-0.3 to 0.3	V
	Voltage between AVDD to DRVDD	-0.3 to 3.3	V
	Voltage applied to VCM pin (in external reference mode)	-0.3 to 1.8	V
	Voltage applied to analog input pins, INP and INM	–0.3 V to minimum (3.6, AVDD + 0.3 V)	V
	Voltage applied to input clock pins, CLKP and CLKM	-0.3 V to AVDD + 0.3 V	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
SUPPLIES					
	Analog supply voltage, AVDD	3	3.3	3.6	V
	Digital supply voltage, DRVDD	3	3.3	3.6	V
ANALOG INPUTS					
	Differential input voltage range		2		V_{PP}
	Input common-mode voltage		1.5 ±0.1		V
	Voltage applied on VCM in external reference mode	1.45	1.5	1.55	V
CLOCK INPUT					
	Input clock sample rate	1		170	MSPS
	Input clock amplitude differential ($V_{(CLKP)}$ - $V_{(CLKM)}$)				
	Sine wave, ac-coupled	0.4	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
	LVCMOS, single-ended, ac-coupled		3.3		V
	Input clock duty cycle (See Figure 34)	35%	50%	65%	
DIGITAL OUTPUTS					
C_L	Maximum external load capacitance from each output pin to DRGND (LVDS and CMOS modes)		5		pF
R_L	Differential load resistance between the LVDS output pairs (LVDS mode)		100		Ω
	Operating free-air temperature	–40		85	°C

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0dB gain, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION				12		bits
ANALOG INPUT						
	Differential input voltage range			2		V_{PP}
	Differential input capacitance			7		pF
	Analog input bandwidth	–3 dB, source impedance 50 Ω		500		MHz
	Analog input common mode current (per input pin)			280		µA
REFERENCE VOLTAGES						
$V_{(REFB)}$	Internal reference bottom voltage	Internal reference mode		0.5		V
$V_{(REFT)}$	Internal reference top voltage	Internal reference mode		2.5		V
V_{CM}	Common mode output voltage	Internal reference mode		1.5		V
	VCM output current capability	Internal reference mode		±4		mA
DC ACCURACY						
	No Missing Codes			Specified		
DNL	Differential non-linearity		–0.9	0.5	TBD	LSB
INL	Integral non-linearity			± 1		LSB
	Offset error			5		mV
	Offset temperature coefficient			0.002		ppm/°C
	Gain error			±1		%FS
	Gain temperature coefficient			0.01		Δ%/°C
PSRR	DC Power supply rejection ratio			0.6		mV/V
POWER SUPPLY						
$I_{(AVDD)}$	Analog supply current			284		mA
$I_{(DRVDD)}$	Digital supply current	LVDS mode, I_O = 3.5 mA, R_L = 100 Ω, C_L = 5 pF		49		mA
		CMOS mode, F_{IN} = 2.5 MHz, C_L = 5 pF		39		mA
I_{CC}	Total supply current	LVDS mode		333		mA
	Total power dissipation	LVDS mode		1.1	TBD	W
	Standby power	In STANDBY mode with clock running		100	TBD	mW
	Clock stop power	With input clock stopped		100	TBD	mW

ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0dB gain, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC CHARACTERISTICS							
SNR	Signal to noise ratio	F_{IN} = 10 MHz			70		dBFS
		F_{IN} = 40 MHz			69.7		
		F_{IN} = 70 MHz		TBD	69.5		
		F_{IN} = 100 MHz			69.2		
		F_{IN} = 150 MHz			68.7		
		F_{IN} = 225 MHz	0 dB gain, 2 V_{PP} FS(1)		67		
			3 dB gain, 1.4 V_{PP} FS		TBD		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		66.1		
			3 dB gain, 1.4 V_{PP} FS		TBD		
	RMS output noise	Inputs tied to common-mode			0.39		LSB
SFDR	Spurious free dynamic range	F_{IN} = 10 MHz			87		dBc
		F_{IN} = 40 MHz			83		
		F_{IN} = 70 MHz		TBD	82		
		F_{IN} = 100 MHz			81		
		F_{IN} = 150 MHz			80		
		F_{IN} = 225 MHz	0 dB gain, 2 V_{PP} FS		74		
			3 dB gain, 1.4 V_{PP} FS		TBD		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		70		
			3 dB gain, 1.4 V_{PP} FS		TBD		
SINAD	Signal to noise and distortion ratio	F_{IN} = 10 MHz			69.8		dBFS
		F_{IN} = 40 MHz			69.2		
		F_{IN} = 70 MHz		TBD	69		
		F_{IN} = 100 MHz			68.6		
		F_{IN} = 150 MHz			68		
		F_{IN} = 225 MHz	0 dB gain, 2 V_{PP} FS		66.1		
			3 dB gain, 1.4 V_{PP} FS		TBD		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		65		
			3 dB gain, 1.4 V_{PP} FS		TBD		
HD2	Second harmonic	F_{IN} = 10 MHz			92		dBc
		F_{IN} = 40 MHz			91		
		F_{IN} = 70 MHz		TBD	90		
		F_{IN} = 100 MHz			89		
		F_{IN} = 150 MHz			87		
		F_{IN} = 225 MHz	0 dB gain, 2 V_{PP} FS		76		
			3 dB gain, 1.4 V_{PP} FS		TBD		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		73		
			3 dB gain, 1.4 V_{PP} FS		TBD		

(1) FS = Full scale range

ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0dB gain, DDR LVDS data output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD3	Third harmonic	F_{IN} = 10 MHz			87		dBc
		F_{IN} = 40 MHz			83		
		F_{IN} = 70 MHz		TBD	82		
		F_{IN} = 100 MHz			81		
		F_{IN} = 150 MHz			80		
		F_{IN} = 225 MHz	0 dB gain, 2 V_{PP} FS		74		
			3 dB gain, 1.4 V_{PP} FS		TBD		
		F_{IN} = 300 MHz	0 dB gain, 2 V_{PP} FS		70		
			3 dB gain, 1.4 V_{PP} FS		TBD		
Worst harmonic (other than HD2, HD3)		F_{IN} = 10 MHz			TBD		dBc
		F_{IN} = 40 MHz			TBD		
		F_{IN} = 70 MHz			TBD		
		F_{IN} = 100 MHz			TBD		
		F_{IN} = 150 MHz			TBD		
		F_{IN} = 225 MHz			TBD		
		F_{IN} = 300 MHz			TBD		
THD	Total harmonic distortion	F_{IN} = 10 MHz			82		dBc
		F_{IN} = 40 MHz			81		
		F_{IN} = 70 MHz		TBD	79		
		F_{IN} = 100 MHz			78		
		F_{IN} = 150 MHz			77		
		F_{IN} = 225 MHz			73		
		F_{IN} = 300 MHz			68		
ENOB	Effective number of bits	F_{IN} = 10 MHz			11.3		bits
IMD	Two-tone intermodulation distortion	F_{IN1} = 50.09 MHz, F_{IN2} = 46.09 MHz, -7 dBFS each tone			TBD		dBFS
		F_{IN1} = 135.08 MHz, F_{IN2} = 130.08 MHz, -7 dBFS each tone			TBD		
PSRR	AC power supply rejection ratio	30 MHz, 200 mV_{PP} signal on 3.3-V supply			TBD		dBc
	Voltage overload recovery time	Recovery to 1% (of final value) for 6-dB overload with sine-wave input at Nyquist frequency			1		Clock cycles

DIGITAL CHARACTERISTICS(1)

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = DRVDD = 3.3 V, I_O = 3.5 mA, R_L = 100 Ω(2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		µA
Low-level input current			–33		µA
Input capacitance			4		pF
DIGITAL OUTPUTS – CMOS MODE					
High-level output voltage			3.3		V
Low-level output voltage			0		V
Output capacitance	Output capacitance inside the device, from each output to ground		2		pF
DIGITAL OUTPUTS – LVDS MODE					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $\lvert V_{OD} \rvert$		225	350		mV
V_{OS} Output offset voltage, single-ended	Common-mode voltage of OUTP and OUTM		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

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(1) All LVDS and CMOS specifications are characterized, but not tested at production.

(2) I_O refers to the LVDS buffer current setting, R_L is the differential load resistance between the LVDS output pair.

TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V, sampling frequency = 170 MSPS, sine wave input clock, 1.5 V_{PP} clock amplitude, C_L = 5 pF(2), I_O = 3.5 mA, R_L = 100 Ω(3), no internal termination, unless otherwise noted.

For timings at lower sampling frequencies, see the *Output Timing* section in the APPLICATION INFORMATION of this data sheet.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			1.2		ns
t_j	Aperture jitter			150		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode			100	µs
		Time to valid data after stopping and restarting the input clock			100	
	Latency			14		clock cycles

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(1) Timing parameters are specified by design and characterization and not tested in production.

(2) C_L is the effective external single-ended load capacitance between each output pin and ground.

(3) I_O refers to the LVDS buffer current setting; R_L is the differential load resistance between the LVDS output pair.

TIMING CHARACTERISTICS – LVDS AND CMOS MODES (continued)

For timings at lower sampling frequencies, see the *Output Timing* section in the APPLICATION INFORMATION of this data sheet.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DDR LVDS MODE(4)						
t_{su}	Data setup time(5)	Data valid (6) to zero-cross of CLKOUTP		1.8		ns
t_h	Data hold time(5)	Zero-cross of CLKOUTP to data becoming invalid(6)		1.0		ns
t_{PDI}	Clock propagation delay	Input clock rising edge zero-cross to output clock rising edge zero-cross		4.6		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) 80 ≤ Fs ≤ 170 MSPS		50%		
t_r , t_f	Data rise time, Data fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 170 MSPS	50	100	200	ps
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –50 mV to 50 mV Fall time measured from 50 mV to –50 mV 1 ≤ Fs ≤ 170 MSPS	50	100	200	ps
t_{OE}	Output enable (OE) to valid data delay	Time to valid data after OE becomes active			1	µs
PARALLEL CMOS MODE						
t_{su}	Data setup time (5)	Data valid(7) to 50% of CLKOUT rising edge		3.3		ns
t_h	Data hold time (5)	50% of CLKOUT rising edge to data becoming invalid(7)		1.2		ns
t_{PDI}	Clock propagation delay	Input clock rising edge zero-cross to 50% of CLKOUT rising edge		2.7		ns
	Output clock duty cycle	Duty cycle of output clock (CLKOUT) 80 ≤ Fs ≤ 170 MSPS		45%		
t_r , t_f	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 170 MSPS	0.8	1.5	2	ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1 ≤ Fs ≤ 170 MSPS	0.4	0.8	1.2	ns
t_{OE}	Output enable (OE) to valid data delay	Time to valid data after OE becomes active			50	ns

(4) Measurements are done with a transmission line of 100 Ω characteristic impedance between the device and the load.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
(6) Data valid refers to logic high of +50 mV and logic low of –50 mV.
(7) Data valid refers to logic high of 2 V and logic low of 0.8 V

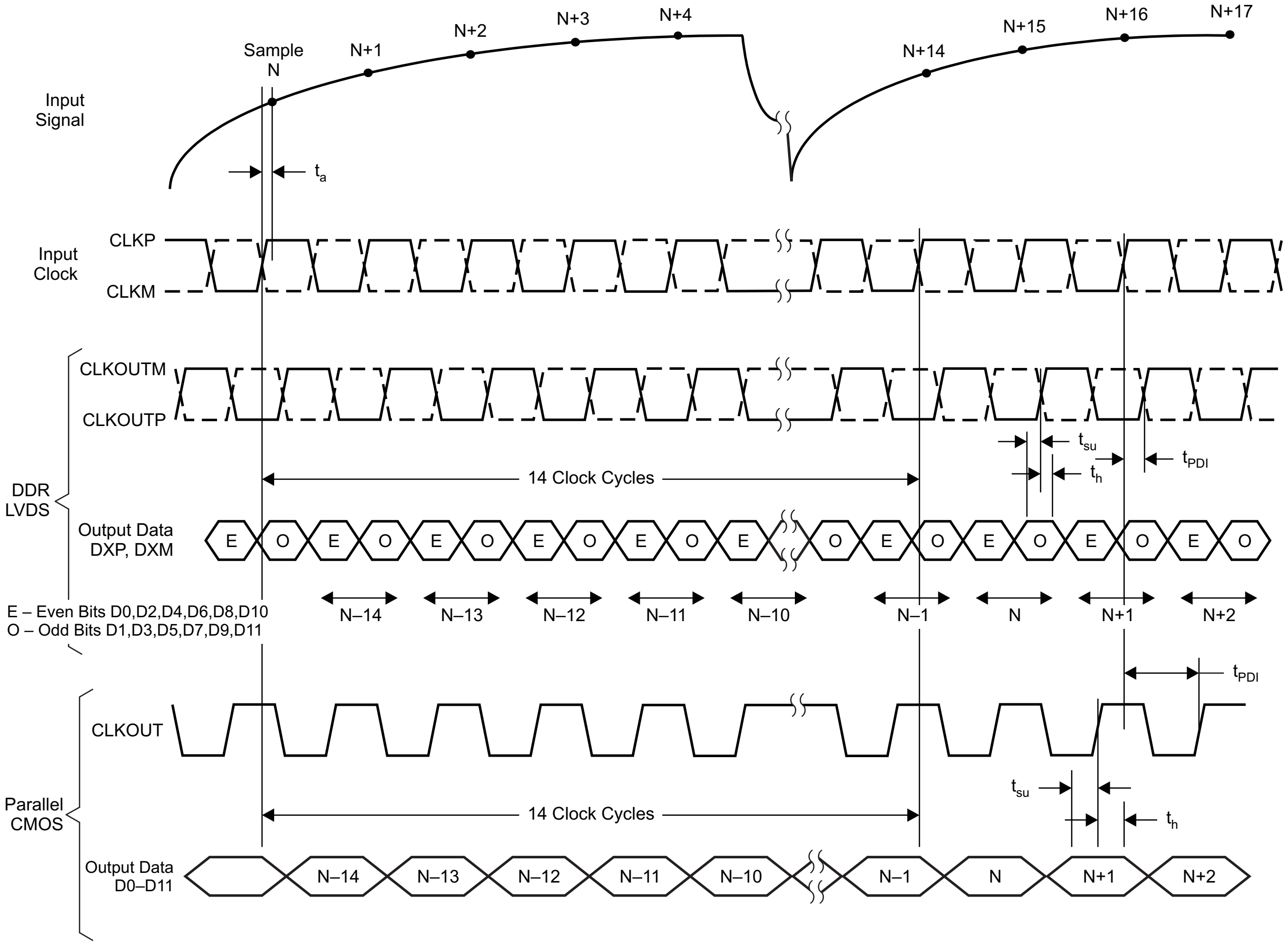
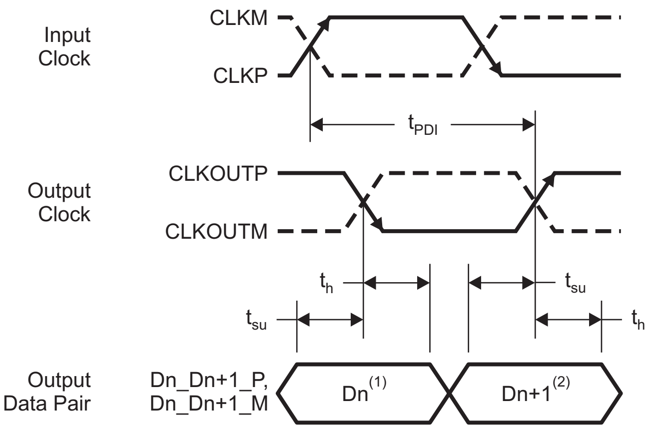


Figure 1. Latency

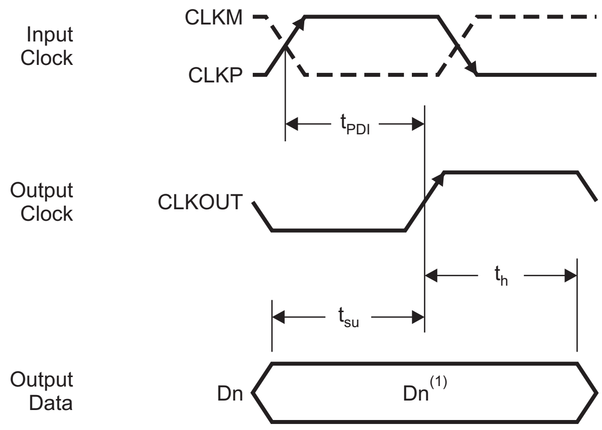


(1) Dn – Bits D0, D2, D4, D6, D8, D10

(2) Dn+1 – Bits D1, D3, D5, D7, D9, D11

Figure 2. LVDS Mode Timing

PRODUCT PREVIEW



(1)Dn – Bits D0–D11

Figure 3. CMOS Mode Timing

DEVICE CONFIGURATION

ADS5525 offers flexibility with several programmable features that are easily configured.

The device can be configured independently using either a parallel interface control or a serial interface programming.

In addition, the device supports a third configuration mode, where both the parallel interface and the serial control registers are used. In this mode, the priority between the parallel and serial interfaces is determined by a priority table (Table 2). If this additional level of flexibility is not required, the user can select either the serial interface programming or the parallel interface control.

PARALLEL CONFIGURATION ONLY

To place the device in parallel configuration mode, keep RESET tied to **high** (DRVDD). Pins DFS, MODE, SEN, and SDATA are used to directly control certain modes of the ADC. The device is configured by connecting the parallel pins to the correct voltage levels (as described in Table 3 to Table 6). There is no need to apply reset.

In this mode, SEN and SDATA function as parallel interface control pins. Frequently used functions are controlled in this mode—standby, selection between LVDS/CMOS output format, internal/external reference, two's complement/straight binary output format, and position of the output clock edge.

Table 1 has a description of the modes controlled by the four parallel pins.

Table 1. Parallel Pin Definition

PIN	CONTROL MODES
DFS	DATA FORMAT and the LVDS/CMOS output interface
MODE	Internal or external reference
SEN	CLKOUT edge programmability
SDATA	STANDBY mode – Global (ADC, internal references and output buffers are powered down)

SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, the serial registers must first be reset to their default values, and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on the RESET pin, or by a **high** setting on the <RST> bit (D1 in register 0x6C). The *serial interface section* describes the register programming and register reset in more detail.

Since the parallel pins DFS and MODE are not used in this mode, they must be tied to ground.

CONFIGURATION USING BOTH THE SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, an additional configuration mode is supported. A combination of serial interface registers and parallel pin controls (DFS, MODE) are used to configure the device.

To exercise this mode, the serial registers must first be reset to their default values, and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on RESET pin or by a **high** setting on the <RST> bit (D1 in register 0x6C). The *serial interface section* describes the register programming and register reset in more detail.

The parallel interface control pins DFS and MODE are used, and their function is determined by the appropriate voltage levels as described in Table 5 and Table 6. The voltage levels are derived by using a resistor string as illustrated in Figure 4. Since some functions are controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table (Table 2).

Table 2. Priority Between Parallel Pins and Serial Registers

PIN	FUNCTIONS SUPPORTED	PRIORITY
MODE	Internal/External reference	When using the serial interface, bit <REF> (register 0x6D, bit D4) controls this mode, ONLY if the MODE pin is tied low.
DFS	DATA FORMAT	When using the serial interface, bit <DF> (register 0x63, bit D3) controls this mode, ONLY if the DFS pin is tied low.
	LVDS/CMOS	When using the serial interface, bit <ODI> (register 0x6C, bits D3-D4) controls LVDS/CMOS selection independent of the state of DFS pin

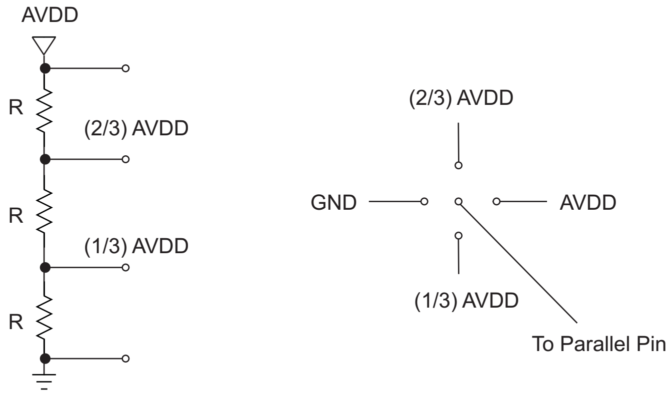


Figure 4. Simple Scheme to Configure Parallel Pins

DESCRIPTION OF PARALLEL PINS

Table 3. SDATA Control Pin

SDATA (Pin 28)	DESCRIPTION
0	Normal operation (Default)
DRVDD	STANDBY. This is a global power down, where ADC, internal references and the output buffers are powered down.

Table 4. SEN Control Pin

SEN (Pin 27)	DESCRIPTION
0	**CMOS mode**: CLKOUT edge later by (3/12)Ts (1); **LVDS mode**: CLKOUT edge aligned with data transition
(1/3)DRVDD	**CMOS mode**: CLKOUT edge later by (2/12)Ts (1); **LVDS mode**: CLKOUT edge aligned with data transition
(2/3)DRVDD	**CMOS mode**: CLKOUT edge later by (1/12)Ts (1); **LVDS mode**: CLKOUT edge earlier by (1/12)Ts (1)
DRVDD	Default CLKOUT position

(1) Ts = 1/Sampling Frequency

Table 5. DFS Control Pin

DFS (Pin 6)	DESCRIPTION
0	2's complement data and DDR LVDS output (Default)
(1/3)DRVDD	2's complement data and parallel CMOS output
(2/3)DRVDD	Offset binary data and parallel CMOS output
DRVDD	Offset binary data and DDR LVDS output

Table 6. MODE Control Pin

MODE (Pin 23)	DESCRIPTION
0	Internal reference
(1/3)AVDD	External reference
(2/3)AVDD	External reference
AVDD	Internal reference

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed through the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock), SDATA (Serial Interface Data) and RESET. After device power-up, the internal registers must be reset to their default values by applying a high-going pulse on RESET (of width greater than 10 ns).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data is loaded in multiples of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits form the register data.

REGISTER INITIALIZATION

After power-up, the internal registers *must* be reset to their default values. This is done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10 ns) as shown in Figure 5.

   OR

2. By applying software reset. Using the serial interface, set the <RST> bit (D1 in register 0x6C) to **high**. This initializes the internal registers to their default values and then self-resets the <RST> bit to **low**. In this case the RESET pin is kept **low**.

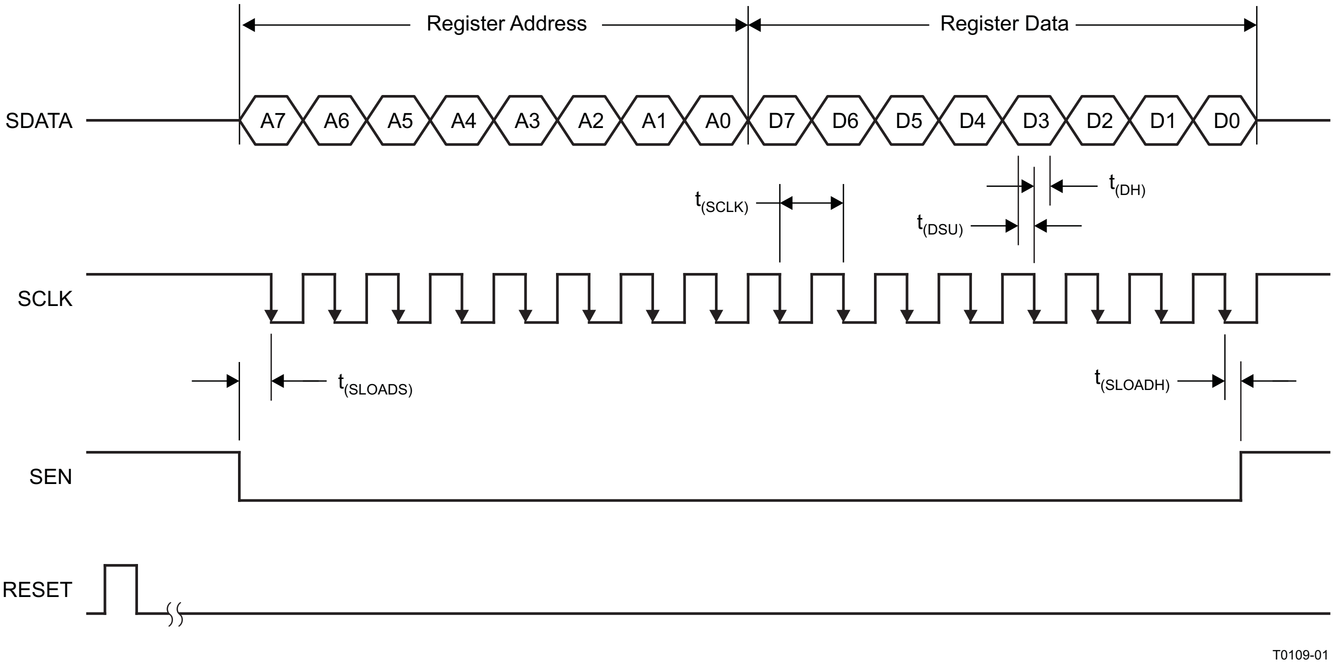


Figure 5. Serial Interface Timing Diagram

SERIAL INTERFACE TIMING CHARACTERISTICS

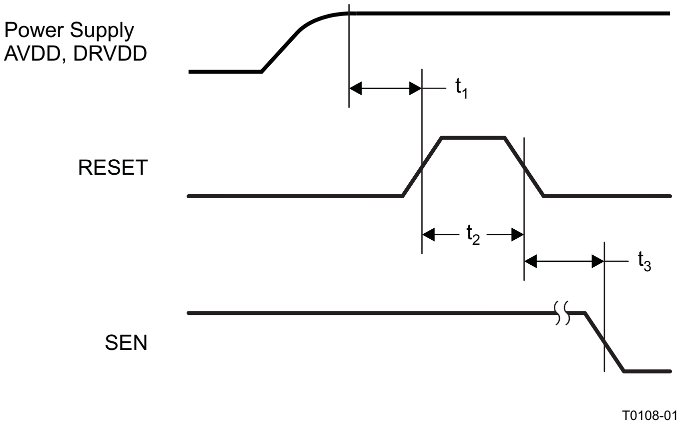
Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{SCLK}	SCLK period	50			ns
	SCLK duty cycle		50%		
t_{SLOADS}	SEN to SCLK setup time		25		ns
t_{SLOADH}	SCLK to SEN hold time		25		ns
t_{DSU}	SDATA setup time		25		ns
t_{DH}	SDATA hold time		25		ns

RESET TIMING

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up time	Delay from power-up of AVDD and DRVDD to output stable		6.5		ms



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 6. Reset Timing Diagram

PRODUCT PREVIEW

DESCRIPTION OF SERIAL REGISTERS

Table 7 gives a summary of all the modes that can be programmed through the serial interface.

Table 7. Serial Interface Register Map

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<STBY> – Global Power Down																
0	1	1	0	0	0	1	1	**0**	0	0	0	0	0	0	0	NORMAL converter operation (Default after reset)
0	1	1	0	0	0	1	1	**1**	0	0	0	0	0	0	0	STANDBY
<RST> – Software Reset																
0	1	1	0	1	1	0	0	0	0	0	0	0	0	**1**	0	Resets all registers to default values
<DF> – Output Data Format																
0	1	1	0	0	0	1	1	0	0	0	0	**0**	0	0	0	2's complement output format (Default after reset)
0	1	1	0	0	0	1	1	0	0	0	0	**1**	0	0	0	Straight binary output format
<ODI> – Output Data Interface																
0	1	1	0	1	1	0	0	0	0	0	**0**	**1**	0	0	0	DDR LVDS outputs (D4:D3 defaults to 00 after reset)
0	1	1	0	1	1	0	0	0	0	0	**1**	**1**	0	0	0	Parallel CMOS outputs
<REF> –Internal/External reference mode																
0	1	1	0	1	1	0	1	0	0	0	**0**	0	0	0	0	Internal reference (Default after reset)
0	1	1	0	1	1	0	1	0	0	0	**1**	0	0	0	0	External reference – Force voltage on VCM pin
<TEST PATTERN> – Output test pattern on data outputs																
0	1	1	0	0	1	0	1	**0**	**0**	**0**	0	0	0	0	0	Normal operation (Default after reset)
0	1	1	0	0	1	0	1	**0**	**0**	**1**	0	0	0	0	0	All zeros
0	1	1	0	0	1	0	1	**0**	**1**	**0**	0	0	0	0	0	All ones
0	1	1	0	0	1	0	1	**0**	**1**	**1**	0	0	0	0	0	Toggle pattern Alternate 1s and 0s on each data output and across the data outputs.
0	1	1	0	0	1	0	1	**1**	**0**	**0**	0	0	0	0	0	Ramp pattern – Output data ramps from 0x000 to 0xFFF every clock cycle
0	1	1	0	0	1	0	1	**1**	**0**	**1**	0	0	0	0	0	Custom pattern. Write the custom pattern in CUSTOM PATTERN registers A and B.
0	1	1	0	0	1	0	1	**X**	**X**	**X**	0	0	0	0	0	NOT USED
<CUSTOM PATTERN> – Output custom pattern on data outputs																
0	1	1	0	1	0	0	1	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	0	0	CUSTOM PATTERN D5-D0
0	1	1	0	1	0	1	0	0	0	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	CUSTOM PATTERN D11-D6
<CLK GAIN> – Clock Buffer gain programmability, Gain decreases monotonically from Gain 4 to Gain 0																
0	1	1	0	1	0	1	1	0	0	**1**	**1**	**0**	**0**	**1**	**0**	Gain 4
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**1**	**0**	**1**	**0**	Gain 3
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**1**	**1**	**0**	Gain 2
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**0**	**0**	Gain 1 (Default after reset)
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**1**	**1**	Gain 0 Minimum gain
<POWER SCALING> Power scaling vs sampling frequency. The ADC can be operated at reduced power at lower sampling rates with no loss in performance.																
0	1	1	0	1	1	0	1	**0**	**0**	**1**	0	0	0	0	0	Default Fs > 150 MSPS (Default after reset)
0	1	1	0	1	1	0	1	**1**	**0**	**1**	0	0	0	0	0	Power Mode 1 – 105 < Fs ≤ 150 MSPS
0	1	1	0	1	1	0	1	**0**	**1**	**1**	0	0	0	0	0	Power Mode 2 – 50 < Fs ≤ 105 MSPS
0	1	1	0	1	1	0	1	**1**	**1**	**1**	0	0	0	0	0	Power Mode 3 – Fs ≤ 50 MSPS

Table 7. Serial Interface Register Map (continued)

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<GAIN> Gain programming - Channel gain can be programmed from 0 to 6 dB for SFDR/SNR trade-off. For each gain setting, the input full-scale range has to be proportionally scaled. For 6 dB gain, the full-scale range will be 1 V_{PP} compared to 2 V_{PP} at 0 dB gain.																
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**0**	**0**	0 dB (Default after reset)
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**0**	**1**	1 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**1**	**0**	2 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**1**	**1**	3 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**1**	**0**	**0**	4 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**1**	**0**	**1**	5 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**1**	**1**	**0**	6 dB
<LVDS CURRENT> – LVDS Output data and clock buffers nominal current programmability																
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**0**	3.5 mA (Default after reset)
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**1**	2.5 mA
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**0**	4.5 mA
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**1**	1.75 mA
<CURRENT DOUBLE> – The output data and clock buffer currents are doubled from the value selected by the <LVDS CURRENT> register.																
0	1	1	1	1	1	1	1	**0**	**0**	0	0	0	0	0	0	value specified by <LVDS CURRENT> (Default after reset)
0	1	1	1	1	1	1	1	**0**	**1**	0	0	0	0	0	0	2x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**0**	0	0	0	0	0	0	1x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**1**	0	0	0	0	0	0	2x data, 4x clock currents
<DATA TERM> Internal termination - Option to terminate the LVDS DATA buffers inside the ADC to improve signal integrity. By default, internal termination is disabled.																
0	1	1	1	1	1	1	0	**0**	**0**	**0**	0	0	0	0	0	No termination (Default after reset)
0	1	1	1	1	1	1	0	**0**	**0**	**1**	0	0	0	0	0	325 Ω
0	1	1	1	1	1	1	0	**0**	**1**	**0**	0	0	0	0	0	200 Ω
0	1	1	1	1	1	1	0	**0**	**1**	**1**	0	0	0	0	0	125 Ω
0	1	1	1	1	1	1	0	**1**	**0**	**0**	0	0	0	0	0	170 Ω
0	1	1	1	1	1	1	0	**1**	**0**	**1**	0	0	0	0	0	120 Ω
0	1	1	1	1	1	1	0	**1**	**1**	**0**	0	0	0	0	0	100 Ω
0	1	1	1	1	1	1	0	**1**	**1**	**1**	0	0	0	0	0	75 Ω
<CLK TERM> Internal termination - Option to terminate the LVDS CLK buffers inside the ADC to improve signal integrity. By default, internal termination is disabled.																
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**0**	0	0	No termination (Default after reset)
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**1**	0	0	325 Ω
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**0**	0	0	200 Ω
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**1**	0	0	125 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**0**	0	0	170 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**1**	0	0	120 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**0**	0	0	100 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**1**	0	0	75 Ω
<CLKOUT POSN CMOS> – Output clock rising edge programmability in CMOS mode [1]																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	CLKOUT rising edge later by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**0**	**1**	CLKOUT rising edge later by (3/12)Ts
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**1**	**1**	CLKOUT rising edge later by (2/12)Ts

[1] Ts = 1/Sampling Frequency

Table 7. Serial Interface Register Map (continued)

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
<CLKOUT POSN CMOS> – Output clock falling edge programmability in CMOS mode (2)																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	**1**	CLKOUT falling edge later by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	**1**	**0**	0	0	**1**	CLKOUT falling edge later by (3/12)Ts
0	1	1	0	0	0	1	0	0	0	0	**1**	**1**	0	0	**1**	CLKOUT falling edge later by (2/12)Ts
<CLKOUT POSN LVDS> – Output clock rising edge programmability in LVDS mode (2)																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	CLKOUT rising edge earlier by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**0**	**1**	CLKOUT rising edge aligned with data transition
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**1**	**1**	CLKOUT rising edge aligned with data transition
<CLKOUT POSN LVDS> – Output clock falling edge programmability in LVDS mode (2)																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	**1**	CLKOUT falling edge earlier by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	**1**	**0**	0	0	**1**	CLKOUT falling edge aligned with data transition
0	1	1	0	0	0	1	0	0	0	0	**1**	**1**	0	0	**1**	CLKOUT falling edge aligned with data transition

(2) Ts = 1/Sampling Frequency

PIN CONFIGURATION (LVDS MODE)

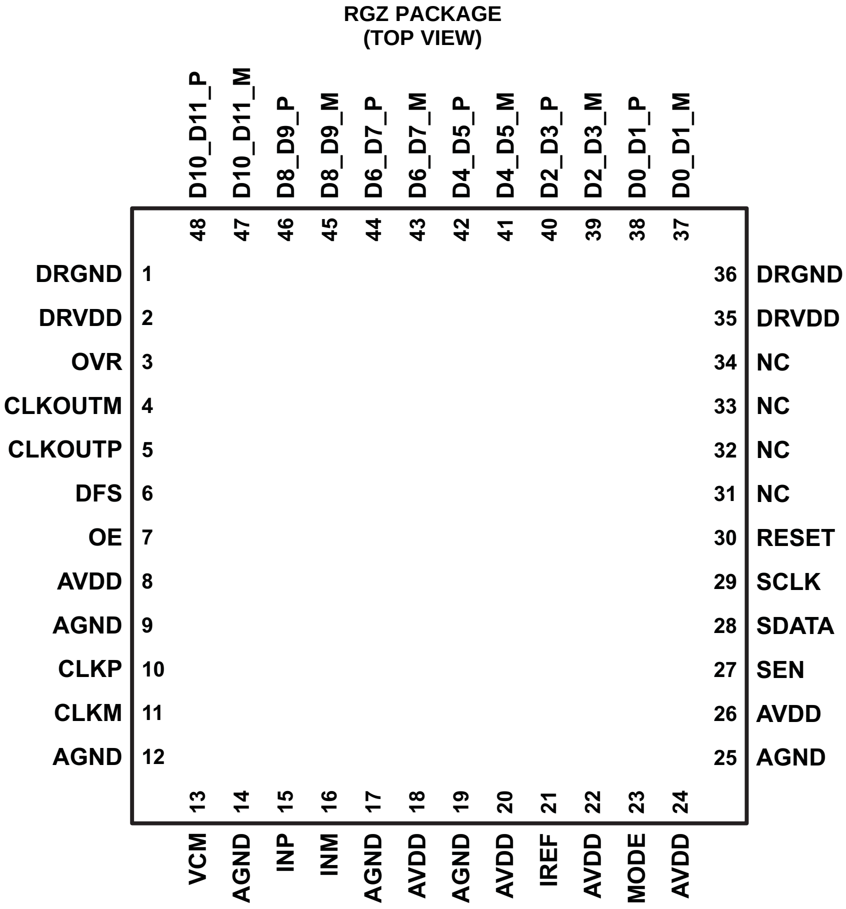


Figure 7. LVDS Mode Pinout

PIN ASSIGNMENTS – LVDS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.	I/O	13	1
IREF	Current-set resistor, 56.2-kΩ resistor to ground.	I	21	1
RESET	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin, or by using the software reset option. See the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie the RESET pin permanently HIGH. (SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100-kΩ pull-down resistor.	I	30	1
SCLK	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.	I	29	1

PIN CONFIGURATION (LVDS MODE) (continued)

PIN ASSIGNMENTS – LVDS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 3 for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 4 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 5 for detailed information.	I	6	1
MODE	Mode select input. This pin selects the Internal or External reference mode. See Table 6 for detailed information.	I	23	1
CLKOUTP	Differential output clock, true	O	5	1
CLKOUTM	Differential output clock, complement	O	4	1
D0_D1_P	Differential output data D0 and D1 multiplexed, true	O	38	1
D0_D1_M	Differential output data D0 and D1 multiplexed, complement.	O	37	1
D2_D3_P	Differential output data D2 and D3 multiplexed, true	O	40	1
D2_D3_M	Differential output data D2 and D3 multiplexed, complement	O	39	1
D4_D5_P	Differential output data D4 and D5 multiplexed, true	O	42	1
D4_D5_M	Differential output data D4 and D5 multiplexed, complement	O	41	1
D6_D7_P	Differential output data D6 and D7 multiplexed, true	O	44	1
D6_D7_M	Differential output data D6 and D7 multiplexed, complement	O	43	1
D8_D9_P	Differential output data D8 and D9 multiplexed, true	O	46	1
D8_D9_M	Differential output data D8 and D9 multiplexed, complement	O	45	1
D10_D11_P	Differential output data D10 and D11 multiplexed, true	O	48	1
D10_D11_M	Differential output data D10 and D11 multiplexed, complement	O	47	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
NC	Do not connect		31, 32, 33, 34	4

PIN CONFIGURATION (CMOS MODE)

RGZ PACKAGE
(TOP VIEW)

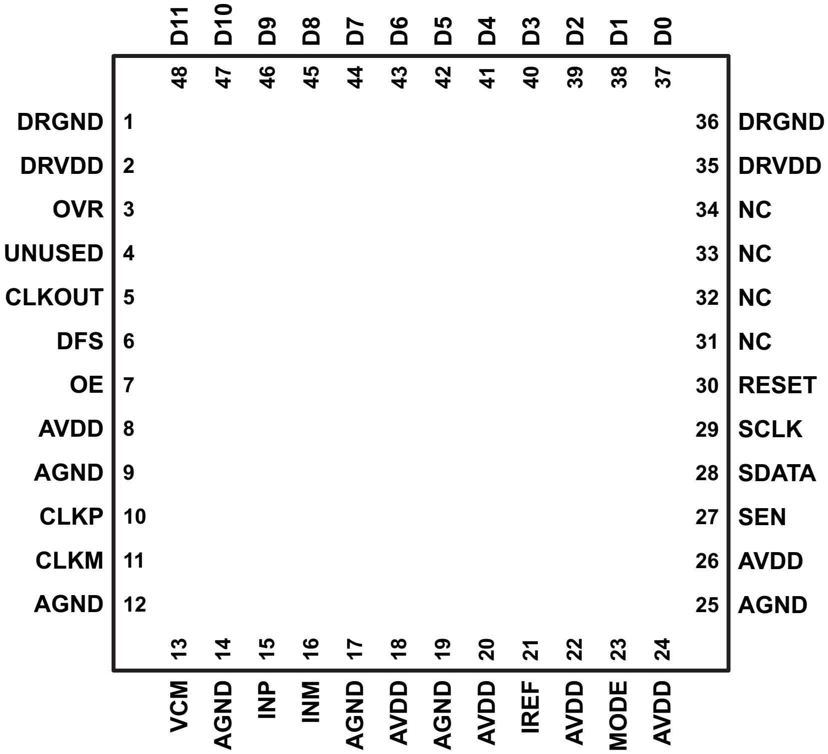


Figure 8. CMOS Mode Pinout

PIN ASSIGNMENTS – CMOS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	8, 18, 20, 22, 24, 26	6
AGND	Analog ground	I	9, 12, 14, 17, 19, 25	6
CLKP, CLKM	Differential clock input	I	10, 11	2
INP, INM	Differential analog input	I	15, 16	2
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.	I/O	13	1
IREF	Current-set resistor, 56.2-kΩ resistor to ground.	I	21	1
RESET	Serial interface RESET input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin, or by using the software reset option. See the *SERIAL INTERFACE* section. In parallel interface mode, the user has to tie RESET pin permanently HIGH. (SDATA and SEN are used as parallel pin controls in this mode). The pin has an internal 100-kΩ pull-down resistor.	I	30	1
SCLK	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.	I	29	1

PIN CONFIGURATION (CMOS MODE) (continued)

PIN ASSIGNMENTS – CMOS Mode (continued)

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
SDATA	This pin functions as serial interface data input when RESET is low. It functions as STANDBY control pin when RESET is tied high. See Table 3 for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	28	1
SEN	This pin functions as serial interface enable input when RESET is low. It functions as CLKOUT edge programmability when RESET is tied high. See Table 4 for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	27	1
OE	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	7	1
DFS	Data Format Select input. This pin sets the DATA FORMAT (Twos complement or Offset binary) and the LVDS/CMOS output mode type. See Table 5 for detailed information.	I	6	1
MODE	Mode select input. This pin selects the internal or external reference mode. See Table 6 for detailed information.	I	23	1
CLKOUT	CMOS output clock	O	5	1
D0	CMOS output data D0	O	37	1
D1	CMOS output data D1	O	38	1
D2	CMOS output data D2	O	39	1
D3	CMOS output data D3	O	40	1
D4	CMOS output data D4	O	41	1
D5	CMOS output data D5	O	42	1
D6	CMOS output data D6	O	43	1
D7	CMOS output data D7	O	44	1
D8	CMOS output data D8	O	45	1
D9	CMOS output data D9	O	46	1
D10	CMOS output data D10	O	47	1
D11	CMOS output data D11	O	48	1
OVR	Out-of-range indicator, CMOS level signal	O	3	1
DRVDD	Digital and output buffer supply	I	2, 35	2
DRGND	Digital and output buffer ground	I	1, 36	2
UNUSED	Unused pin in CMOS mode		4	1
NC	Do not connect		31, 32, 33, 34	4

TYPICAL CHARACTERISTICS

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

FFT for 10 MHz INPUT SIGNAL

TBD

Figure 9.

FFT for 40 MHz INPUT SIGNAL

TBD

Figure 10.

FFT for 70 MHz INPUT SIGNAL

TBD

Figure 11.

FFT for 100 MHz INPUT SIGNAL

TBD

Figure 12.

FFT for 130 MHz INPUT SIGNAL

TBD

Figure 13.

FFT for 150 MHz INPUT SIGNAL

TBD

Figure 14.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

FFT for 200 MHz INPUT SIGNAL

TBD

Figure 15.

FFT for 225 MHz INPUT SIGNAL

TBD

Figure 16.

FFT for 300 MHz INPUT SIGNAL

TBD

Figure 17.

FFT for 375 MHz INPUT SIGNAL

TBD

Figure 18.

FFT for 500 MHz INPUT SIGNAL

TBD

Figure 19.

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

TBD

Figure 20.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

INTERMODULATION DISTORTION (IMD) vs FREQUENCY

TBD

Figure 21.

SFDR vs INPUT FREQUENCY

TBD

Figure 22.

SNR vs INPUT FREQUENCY

TBD

Figure 23.

SNR vs INPUT FREQUENCY

TBD

Figure 24.

SFDR vs GAIN

TBD

Figure 25.

SNR vs GAIN

TBD

Figure 26.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

PERFORMANCE vs AVDD

TBD

Figure 27.

PERFORMANCE vs DRVDD

TBD

Figure 28.

PERFORMANCE vs TEMPERATURE

TBD

Figure 29.

SNR vs SAMPLING FREQUENCY ACROSS POWER SCALING MODES

TBD

Figure 30.

POWER DISSIPATION vs SAMPLING FREQUENCY

TBD

Figure 31.

PERFORMANCE vs INPUT AMPLITUDE

TBD

Figure 32.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

PERFORMANCE vs CLOCK AMPLITUDE

TBD

Figure 33.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

TBD

Figure 34.

OUTPUT NOISE HISTOGRAM WITH INPUTS SHORTED TO COMMON-MODE

TBD

Figure 35.

PERFORMANCE IN EXTERNAL REFERENCE MODE

TBD

Figure 36.

COMMON-MODE REJECTION RATIO vs FREQUENCY

TBD

Figure 37.

TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = 170 MSPS, sine wave input clock, 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, DDR LVDS data output (unless otherwise noted)

TBD

f_{IN} - Input Frequency - MHz

SNR - dBFS

Figure 38. SNR Contour in dBFS

TBD

f_{IN} - Input Frequency - MHz

SFDR - dBc

Figure 39. SFDR Contour in dBc

APPLICATION INFORMATION

THEORY OF OPERATION

ADS5525 is a low power 12-bit 170 MSPS pipeline ADC in a CMOS process. ADS5525 is based on switched capacitor technology and runs off a single 3.3-V supply. The conversion process is initiated by a rising edge of the external input clock. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 14 clock cycles. The output is available as 12-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2’s complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 40.

This differential topology results in good ac-performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V available on VCM pin 13. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5 V nominal) and REFM (0.5 V, nominal).

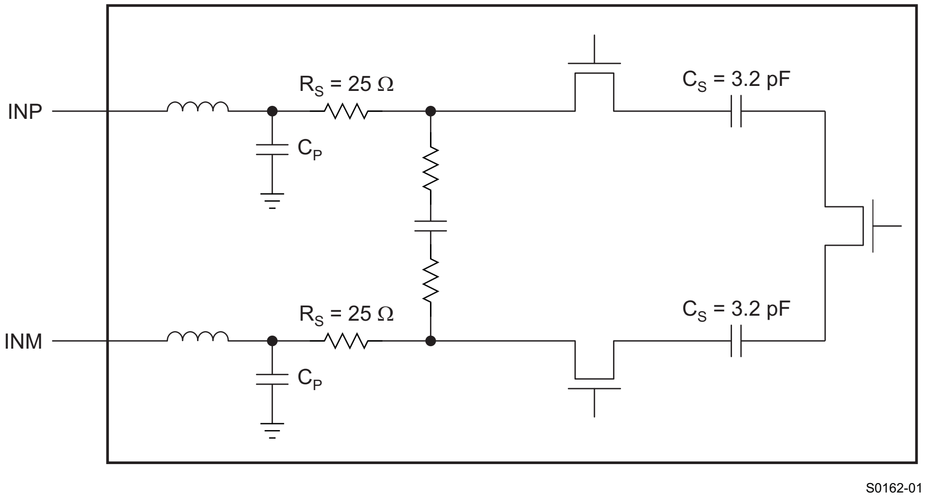
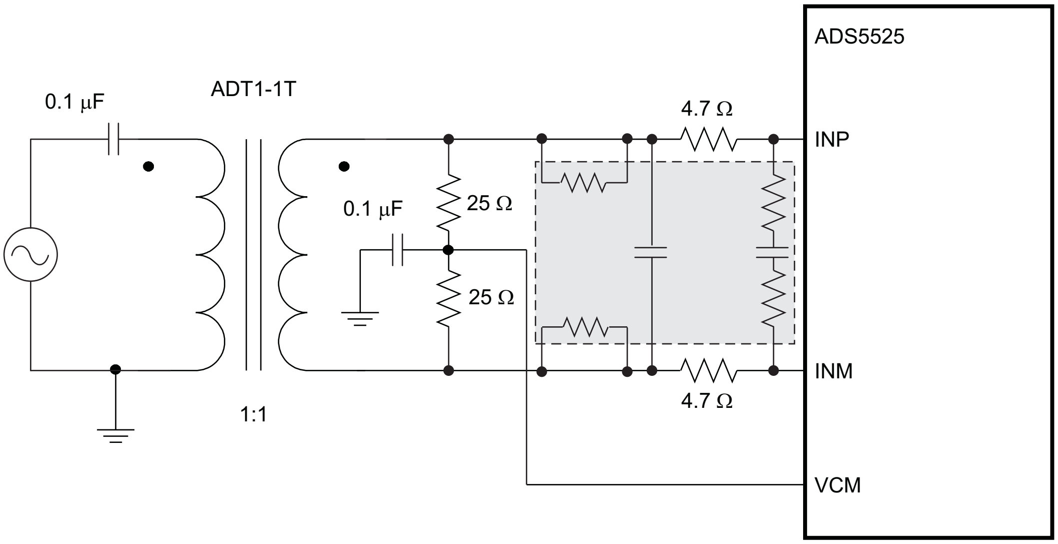


Figure 40. Input Stage

Driving Circuit

For optimum performance, the analog inputs have to be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. Input configurations using RF transformers suitable for low and high input frequencies are shown in Figure 41 and Figure 42. The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated by 50-Ω on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the input sampling capacitors from the RF transformer’s leakage inductances. The termination is accomplished by two 25 Ω connected in series, with the center point connected to the 1.5-V common-mode (VCM pin 13). The 4.7-Ω resistor in series with each input pin is required to dampen the ringing caused by the device package parasitics (shown in Figure 40).

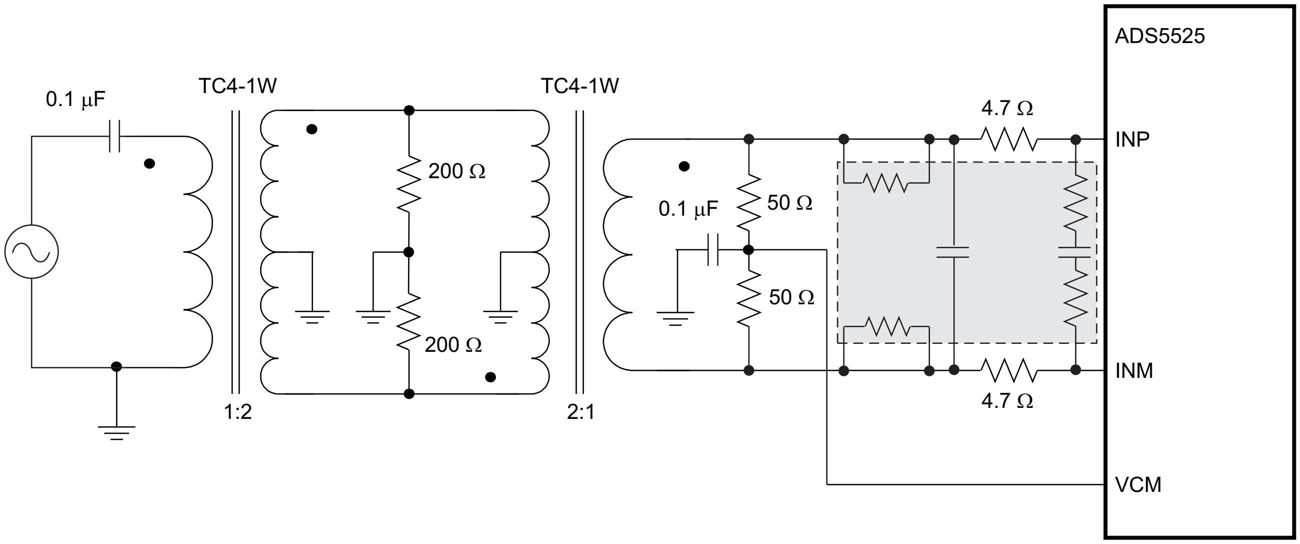
APPLICATION INFORMATION (continued)



A. Components shown inside the shaded box are NOT required for the ADS5525. It is ONLY a provision that allows seamless transition to potential derivatives of the ADS5525.

Figure 41. Drive Circuit at Low Input Frequencies

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair is required between the two transformers as shown in the Figure 42. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to get an overall 50 Ω (in the case of 50-Ω source impedance).



A. Components shown inside the shaded box are NOT required for the ADS5525. It is ONLY a provision that allows seamless transition to potential derivatives of the ADS5525.

Figure 42. Drive Circuit at High Input Frequencies

APPLICATION INFORMATION (continued)

Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 280 µA (at 170 MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{(280\ \mu A)\ \times\ Fs}{170\ MSPS} \qquad (1)$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

Reference

ADS5525 has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the integration of the requisite reference capacitors on-chip eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by controlling the MODE pin 23 (see Table 6 for details) or by programming the serial interface register bit **<REF>**.

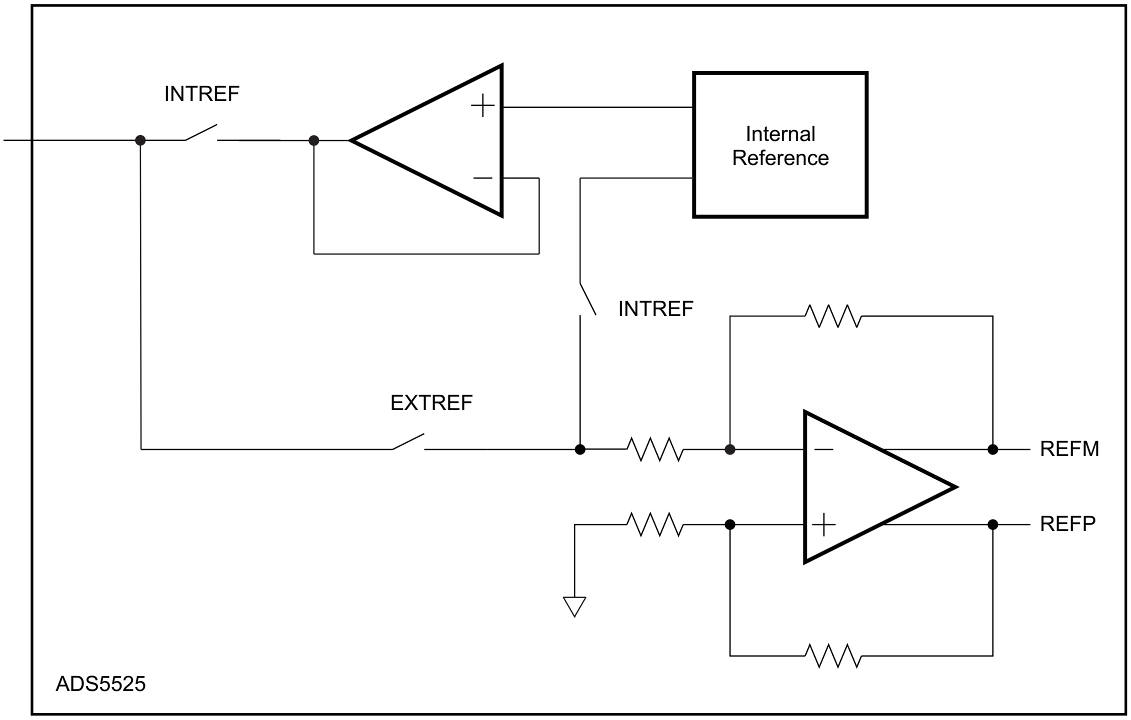


Figure 43. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

APPLICATION INFORMATION (continued)

$$\text{Full–scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (2)$$

In this mode, the 1.5 V common-mode voltage to bias the input pins has to be generated externally. There is no change in performance compared to internal reference mode.

Clock Input

ADS5525 clock inputs can be driven differentially (SINE, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors as shown in Figure 44. This allows the use of transformer-coupled drive circuits for sine wave clock, or ac-coupling for LVPECL, LVDS clock sources (Figure 45 and Figure 46)

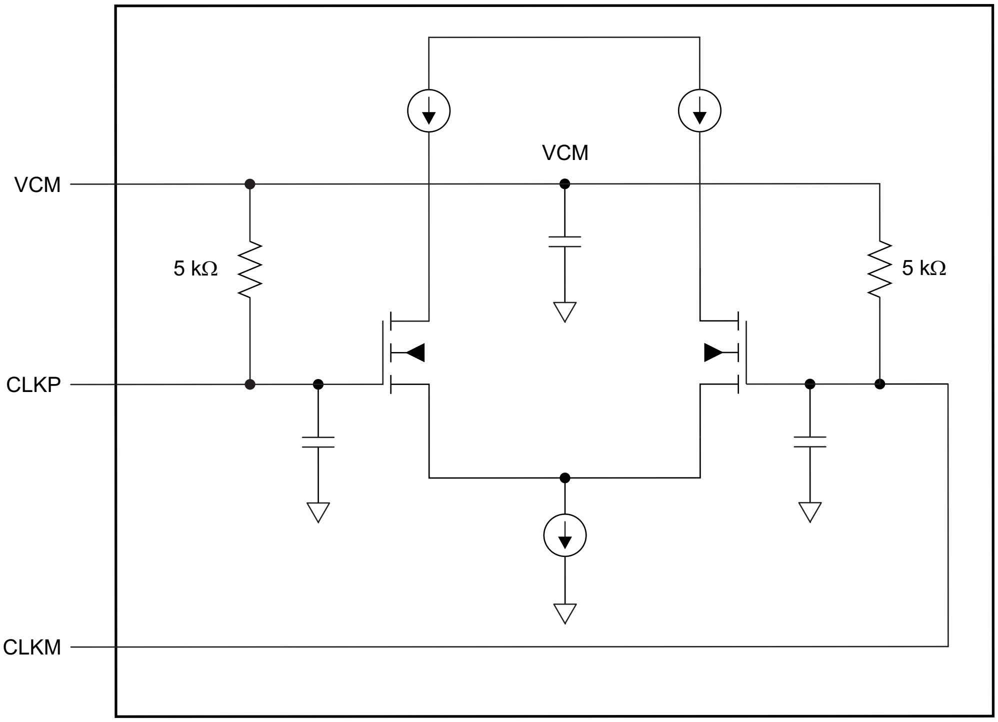


Figure 44. Internal Clock Buffer

For best performance, it is recommended to drive the clock inputs differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.1-µF capacitors, as shown in Figure 45.

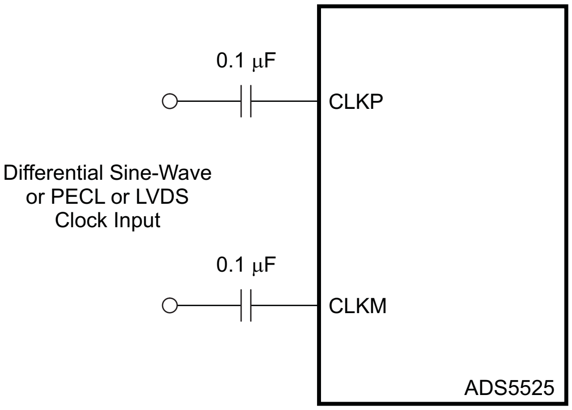


Figure 45. Differential Clock Driving Circuit

APPLICATION INFORMATION (continued)

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM (pin 11) connected to ground with a 0.1-µF capacitor, as shown in Figure 46.

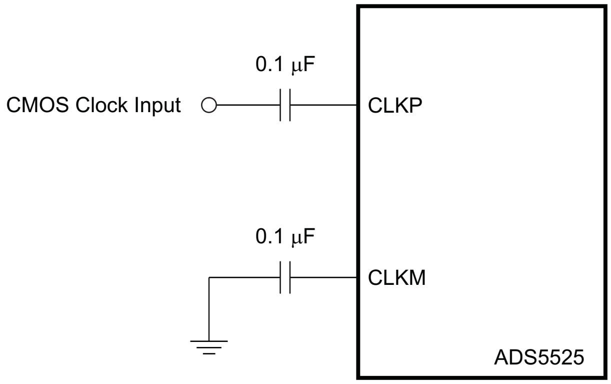


Figure 46. Single-Ended Clock Driving Circuit

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 34 shows the performance variation of the ADC versus clock duty cycle

Clock Buffer Gain

When using a sinusoidal clock input, the noise contributed by clock jitter improves as the clock amplitude is increased. Therefore, using a large amplitude clock is recommended. In addition, the clock buffer has a programmable gain option to amplify the input clock. The clock buffer gain can be set by programming the register bits **<CLK GAIN>**. The clock buffer gain decreases monotonically from Gain 4 to Gain 0 settings.

APPLICATION INFORMATION (continued)

Table 8. Clock Buffer Gain Programming

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<CLK GAIN> – Clock buffer gain programmability, Gain decreases monotonically from Gain 4 to Gain 0																
0	1	1	0	1	0	1	1	0	0	**1**	**1**	**0**	**0**	**1**	**0**	Gain 4
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**1**	**0**	**1**	**0**	Gain 3
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**1**	**1**	**0**	Gain 2
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**0**	**0**	Gain 1 Default gain
0	1	1	0	1	0	1	1	0	0	**1**	**0**	**0**	**0**	**1**	**1**	Gain 0 Minimum gain

Programmable Gain

ADS5525 has programmable gain from 0 dB to 6 dB in steps of 1 dB. The corresponding full-scale input range varies from 2 V_{PP} down to 1 V_{PP}, with 0 dB being the default gain. At high IF, this is especially useful as the SFDR improvement is significant with marginal degradation in SNR.

The gain can be programmed using the serial interface (bits D3-D0 in register 0x68).

Table 9. Programmable Gain

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<GAIN> Gain programming - Channel gain can be programmed from 0 to 6 dB for SFDR/SNR trade-off. For each gain setting, the input full-scale range has to be proportionally scaled. For 6 dB gain, the full-scale range will be 1 V_{PP} compared to 2 V_{PP} at 0 dB gain.																
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**0**	**0**	0 dB Default after reset
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**0**	**1**	1 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**1**	**0**	2 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**0**	**1**	**1**	3 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**1**	**0**	**0**	4 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**1**	**0**	**1**	5 dB
0	1	1	0	1	0	0	0	0	0	0	0	**1**	**1**	**1**	**0**	6 dB

Power Down

ADS5525 has three power-down modes – global STANDBY, output buffer disabled, and input clock stopped.

Global STANDBY

This mode can be initiated by controlling SDATA (pin 28) or by setting the register bit **<STBY>** through the serial interface. In this mode, the A/D converter, reference block and the output buffers are powered down and the total power dissipation reduces to about 100 mW. The output buffers are in high impedance state. The wake-up time from the global power down to data becoming valid normal mode is maximum 100 µs.

Output Buffer Disable

The output buffers can be disabled using OE pin 7 in both the LVDS and CMOS modes, reducing the total power by about 100 mW. With the buffers disabled, the outputs are in high impedance state. The wake-up time from this mode to data becoming valid in normal mode is maximum 1 µs in LVDS mode and 50 ns in CMOS mode.

Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 100 mW and the wake-up time from this mode to data becoming valid in normal mode is maximum 100 µs.

Power Scaling Modes

ADS5525 has a power scaling mode in which the device can be operated at reduced power levels at lower sampling frequencies with no difference in performance. (See Figure 30)(1) There are four power scaling modes for different sampling clock frequency ranges, using the serial interface register bits **<POWER SCALING>**. Only the AVDD power is scaled, leaving the DRVDD power unchanged.

Table 10. Power Scaling vs Sampling Speed

Sampling Frequency MSPS	Power Scaling Mode	Analog Power (Typical)	Analog Power in Default Mode
> 150	Default	960 mW at 170 MSPS	960 mW at 170 MSPS
105 to 150	Power Mode 1	841 mW at 150 MSPS	917 mW at 150 MSPS
50 to 105	Power Mode 2	670 mW at 105 MSPS	830 mW at 105 MSPS
< 50	Power Mode 3	525 mW at 50 MSPS	760 mW at 50 MSPS

(1) The performance in the power scaling modes is from characterization and not tested in production.

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
<POWER SCALING> Power scaling vs sampling frequency. The ADC can be operated at reduced power at lower sampling rates with no loss in performance.																
0	1	1	0	1	1	0	1	**0**	**0**	**1**	0	0	0	0	0	Default Fs > 150 MSPS Default after reset
0	1	1	0	1	1	0	1	**1**	**0**	**1**	0	0	0	0	0	Power Mode1 105 < Fs ≤ 150 MSPS
0	1	1	0	1	1	0	1	**0**	**1**	**1**	0	0	0	0	0	Power Mode2 50 < Fs ≤ 105 MSPS
0	1	1	0	1	1	0	1	**1**	**1**	**1**	0	0	0	0	0	Power Mode3 Fs ≤ 50 MSPS

Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

Digital Output Information

ADS5525 provides 12-bit data, an output clock synchronized with the data and an out-of-range indicator that goes high when the output reaches the full-scale limits. In addition, output enable control (OE pin 7) is provided to power down the output buffers and put the outputs in high-impedance state.

Output Interface

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the DFS (see Table 5) or the serial interface register bit **<ODI>**.

DDR LVDS Outputs

In this mode, the 12 data bits and the output clock are available as LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair as shown in Figure 47. So, there are 6LVDS output pairs for the 12 data bits and 1 LVDS output pair for the output clock.

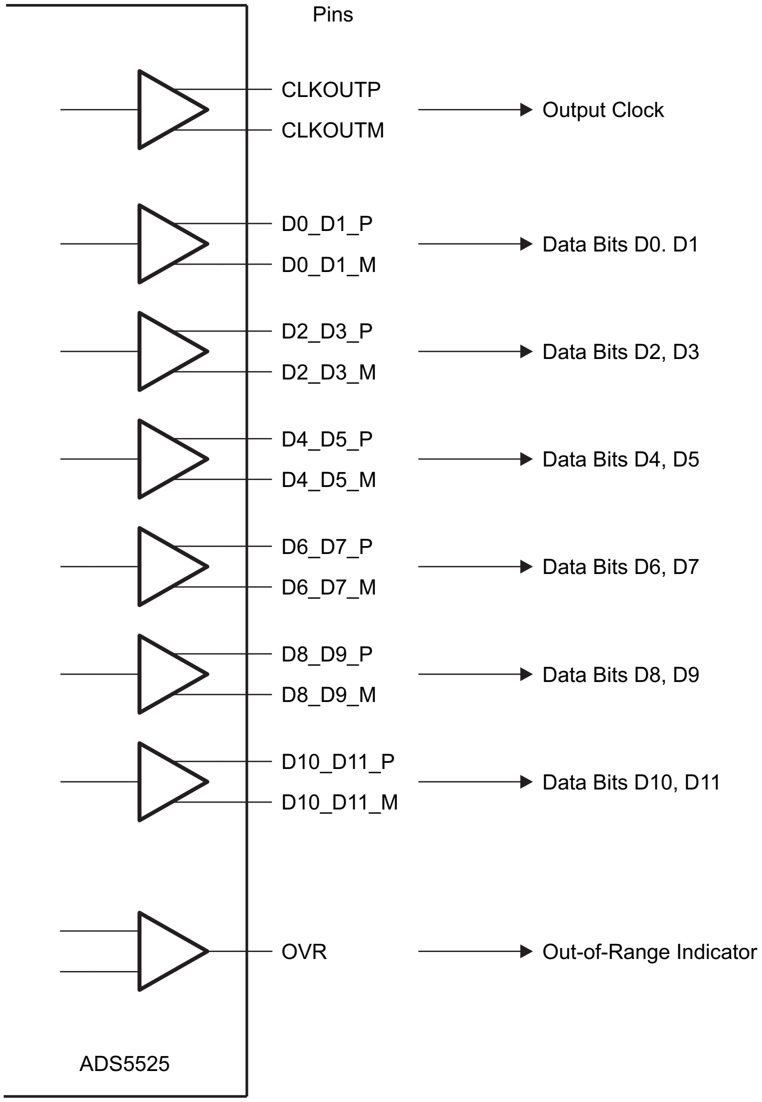


Figure 47. DDR LVDS Outputs

Even data bits D0, D2, D4, D6, D8 and D10 are output at the falling edge of CLKOUTP and the odd data bits D1, D3, D5, D7, D9 and D11 are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the 12 data bits (see Figure 48).

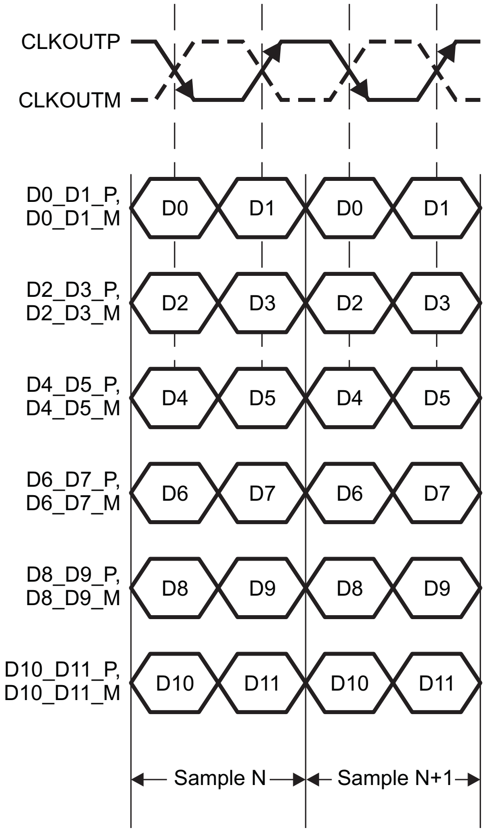


Figure 48. DDR LVDS Interface

LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in a 350-mV single-ended voltage swing (700-mV$_{PP}$ differential swing). The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.75 mA using the serial interface. In addition, there exists a current double mode, where this current is doubled for the data and output clock buffers.

Table 11. LVDS Buffer Currents Programming

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<LVDS CURRENT> – Output data and clock buffers current programmability																
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**0**	3.5 mA Default after reset
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**0**	**1**	2.5 mA
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**0**	4.5 mA
0	1	1	1	1	1	1	0	0	0	0	0	0	0	**1**	**1**	1.75 mA
<CURRENT DOUBLE> – The output data and clock buffer currents are doubled from the value selected by the <LVDS CURRENT> register.																
0	1	1	1	1	1	1	1	**0**	**0**	0	0	0	0	0	0	Value specified by **<LVDS CURRENT>** Default after reset
0	1	1	1	1	1	1	1	**0**	**1**	0	0	0	0	0	0	2x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**0**	0	0	0	0	0	0	1x data, 2x clock currents
0	1	1	1	1	1	1	1	**1**	**1**	0	0	0	0	0	0	2x data, 4x clock currents

LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. The termination resistances available are – 325, 200, and 170 Ω (nominal with ±20% variation). Any combination of these three terminations can be programmed; the effective termination is the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 75 Ω.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100-Ω internal and 100-Ω external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode (see Table 11).

Table 12. Programming Internal Termination for LVDS Data and Clock

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<DATA TERM> Internal termination - Option to terminate the LVDS DATA buffers inside the ADC to improve signal integrity. By default, internal termination is disabled.																
0	1	1	1	1	1	1	0	**0**	**0**	**0**	0	0	0	0	0	No termination Default after reset
0	1	1	1	1	1	1	0	**0**	**0**	**1**	0	0	0	0	0	325 Ω
0	1	1	1	1	1	1	0	**0**	**1**	**0**	0	0	0	0	0	200 Ω
0	1	1	1	1	1	1	0	**0**	**1**	**1**	0	0	0	0	0	125 Ω
0	1	1	1	1	1	1	0	**1**	**0**	**0**	0	0	0	0	0	170 Ω
0	1	1	1	1	1	1	0	**1**	**0**	**1**	0	0	0	0	0	120 Ω
0	1	1	1	1	1	1	0	**1**	**1**	**0**	0	0	0	0	0	100 Ω
0	1	1	1	1	1	1	0	**1**	**1**	**1**	0	0	0	0	0	75 Ω
<CLK TERM> Internal termination – Option to terminate the LVDS CLK buffers inside the ADC to improve signal integrity. By default, internal termination is disabled.																
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**0**	0	0	No termination Default after reset
0	1	1	1	1	1	1	0	0	0	0	**0**	**0**	**1**	0	0	325 Ω
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**0**	0	0	200 Ω
0	1	1	1	1	1	1	0	0	0	0	**0**	**1**	**1**	0	0	125 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**0**	0	0	170 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**0**	**1**	0	0	120 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**0**	0	0	100 Ω
0	1	1	1	1	1	1	0	0	0	0	**1**	**1**	**1**	0	0	75 Ω

Parallel CMOS

In this mode, the 12 data outputs and the output clock are available as 3.3-V CMOS voltage levels. Each data bit and the output clock is available on a separate pin in parallel. By default, the data outputs are valid during the rising edge of the output clock. The output clock is CLKOUT (pin 5).

Output Clock Position Programmability

In both the LVDS and CMOS modes, the output clock can be moved around its default position. This can be done using SEN pin 27 (as described in Table 4) or using the serial interface register bits **<CLKOUT POSN>**. Using this allows to trade-off the setup and hold times leading to reliable data capture. There also exists an option to align the output clock edge with the data transition.

Note that programming the output clock position also affects the clock propagation delay times.

Table 13. CLKOUT Position Programing

REGISTER ADDRESS								REGISTER DATA								DESCRIPTION
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
<CLKOUT POSN CMOS> – Output clock rising edge programmability in CMOS mode																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	Output clock rising edge later by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**0**	**1**	Output clock rising edge later by (3/12)Ts
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**1**	**1**	Output clock rising edge later by (2/12)Ts
<CLKOUT POSN CMOS> – Output clock falling edge programmability in CMOS mode																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	**1**	Output clock falling edge later by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	**1**	**0**	0	0	**1**	Output clock falling edge later by (3/12)Ts
0	1	1	0	0	0	1	0	0	0	0	**1**	**1**	0	0	**1**	Output clock falling edge later by (2/12)Ts
<CLKOUT POSN LVDS> – Output clock rising edge programmability in LVDS mode																
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**0**	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	0	0	**0**	**1**	**1**	Output clock rising edge earlier by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**0**	**1**	Output clock rising edge aligned with data transition
0	1	1	0	0	0	1	0	0	0	0	0	0	**1**	**1**	**1**	Output clock rising edge aligned with data transition
<CLKOUT POSN LVDS> – Output clock falling edge programmability in LVDS mode																
0	1	1	0	0	0	1	0	0	0	0	**0**	**0**	0	0	**1**	Default position
0	1	1	0	0	0	1	0	0	0	0	**0**	**1**	0	0	**1**	Output clock falling edge earlier by (1/12)Ts
0	1	1	0	0	0	1	0	0	0	0	**1**	**0**	0	0	**1**	Output clock falling edge aligned with data transition
0	1	1	0	0	0	1	0	0	0	0	**1**	**1**	0	0	**1**	Output clock falling edge aligned with data transition

Output Data Format

Two output data formats are supported – 2's complement and offset binary. They can be selected using the DFS (pin 6) or the serial interface register bit **<DFS>** . In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0xFFF in offset binary output format, and 0x7FF in 2's complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x800 in 2's complement output format.

Output Timing

For the best performance at high sampling frequencies, ADS5525 uses a clock generator circuit to derive internal timing for ADC. This results in optimal setup and hold times of the output data and 50% output clock duty cycle for sampling frequencies from 80 MSPS to 170 MSPS. See Table 14 for timing information above 80 MSPS.

Table 14. Timing Characteristics (80 MSPS to 170 MSPS) (1)

Fs, MSPS	t_{su} DATA SETUP TIME, ns			t_h DATA HOLD TIME, ns			t_{PDI} CLOCK PROPAGATION DELAY, ns		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
DDR LVDS									
150	1.6	2.1		0.6	1.1		4.3	5	5.7
130	2.0	2.5		0.8	1.3		4.5	5.2	5.9
80	3.6	4.1		1.6	2.1		4.7	5.7	6.7
PARALLEL CMOS									
150	2.8	3.6		1.2	1.6		1.7	2.5	3.3
130	3.3	4.1		1.7	2.1		1.1	1.9	2.7
80	6	7		3.7	4.1		10.8	12	13.2

(1) Timing parameters are specified by design and characterization and not tested in production.

Below 80 MSPS, the setup and hold times do not scale with the sampling frequency. The output clock duty cycle also progressively moves away from 50% as the sampling frequency is reduced from 80 MSPS.

See Table 15 for detailed timings at sampling frequencies below 80 MSPS. Figure 49 shows the clock duty cycle across sampling frequencies in the DDR LVDS and CMOS modes.

Table 15. Timing Characteristics (1 MSPS to 80 MSPS) (1)

Fs, MSPS	t_{su} DATA SETUP TIME, ns			t_h DATA HOLD TIME, ns			t_{PDI} CLOCK PROPAGATION DELAY, ns		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
DDR LVDS									
1 to 80	3.6			1.6				5.7	
PARALLEL CMOS									
1 to 80	6			3.7				12	

(1) Timing parameters are specified by design and characterization and not tested in production.

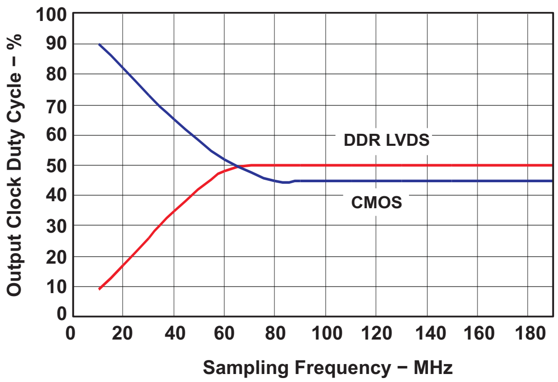


Figure 49. Output Clock Duty Cycle (typical) vs Sampling Frequency

The latency of ADS5525 is 14 clock cycles from the sampling instant (input clock rising edge). In the LVDS mode, the latency remains constant across sampling frequencies. In the CMOS mode, the latency is 14 clock cycles above 80 MSPS and 13 clock cycles below 80 MSPS.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs

Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

DEFINITION OF SPECIFICATIONS (continued)

Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \tag{3}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \tag{4}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

PRODUCT PREVIEW

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{5}$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10} \frac{P_S}{P_N} \tag{6}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

DEFINITION OF SPECIFICATIONS (continued)

AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is the measure of rejection of variations in the supply voltage of the ADC. If ΔV_{SUP} is the change in the supply voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$\text{PSRR} = 20\text{Log}^{10}\frac{\Delta V_{OUT}}{\Delta V_{SUP}} \quad \text{(Expressed in dBc)} \tag{7}$$

Common Mode Rejection Ratio (CMRR)

CMRR is the measure of rejection of variations in the input common-mode voltage of the ADC. If ΔVcm is the change in the input common-mode voltage and ΔV_{OUT} is the resultant change in the ADC output code (referred to the input), then

$$\text{CMRR} = 20\text{Log}^{10}\frac{\Delta V_{OUT}}{\Delta V_{CM}} \quad \text{(Expressed in dBc)} \tag{8}$$

Voltage Overload Recovery

The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs. A 6-dBFS sine wave at Nyquist frequency is used as the test stimulus.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS5525IRGZR	PREVIEW	QFN	RGZ	48	2500	TBD	Call TI	Call TI
ADS5525IRGZT	PREVIEW	QFN	RGZ	48	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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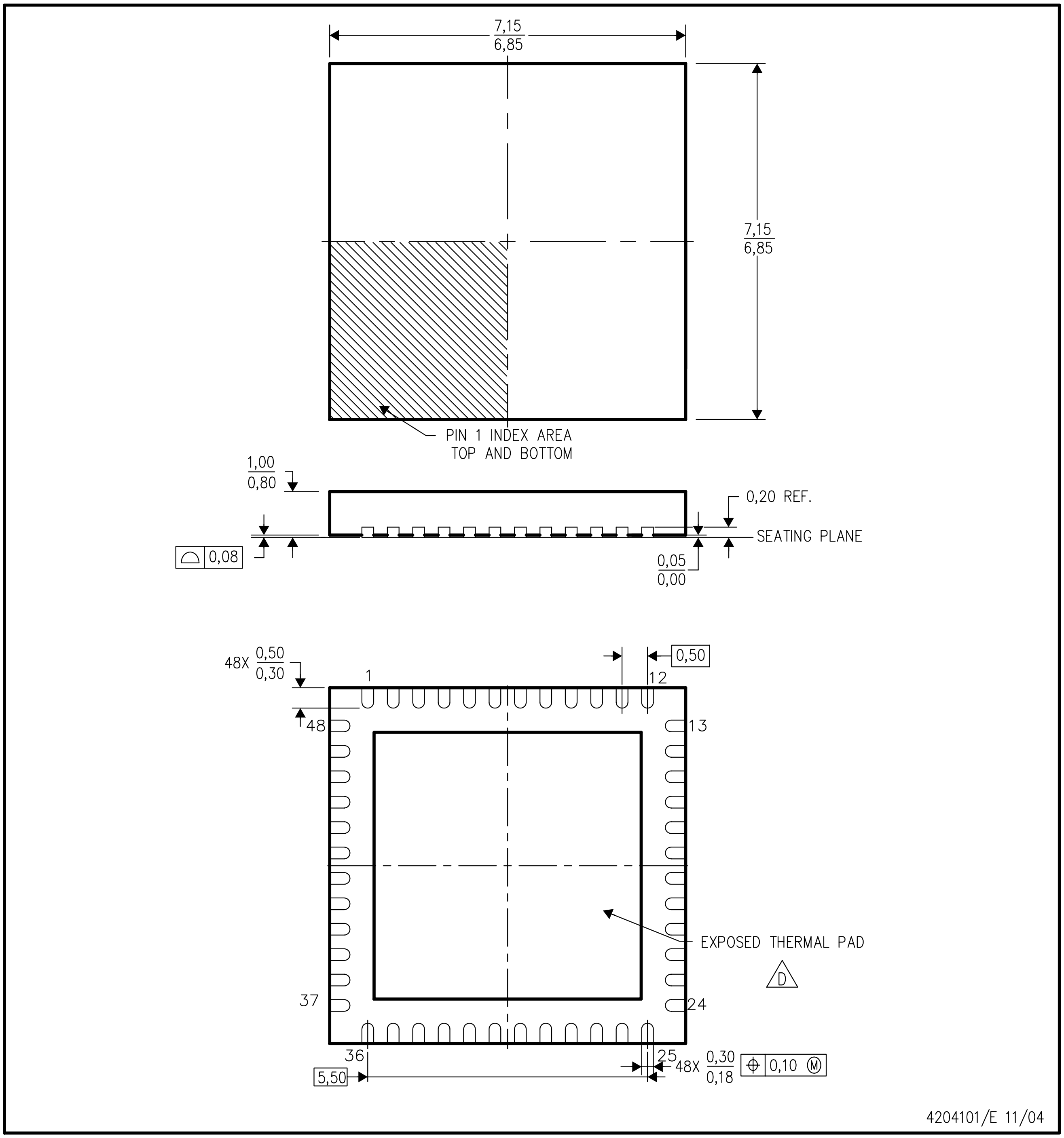
RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

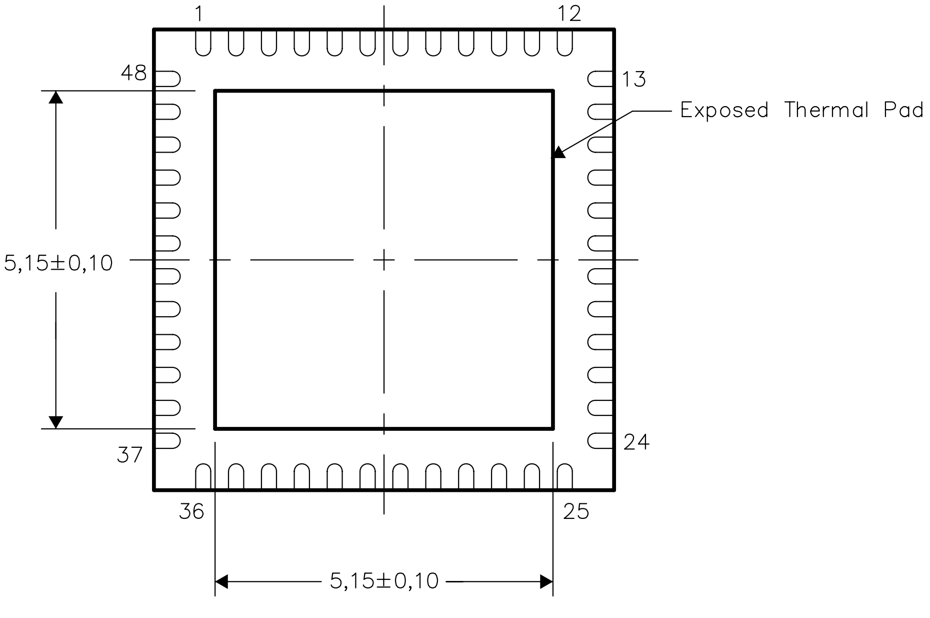
RGZ (S–PQFP–N48)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

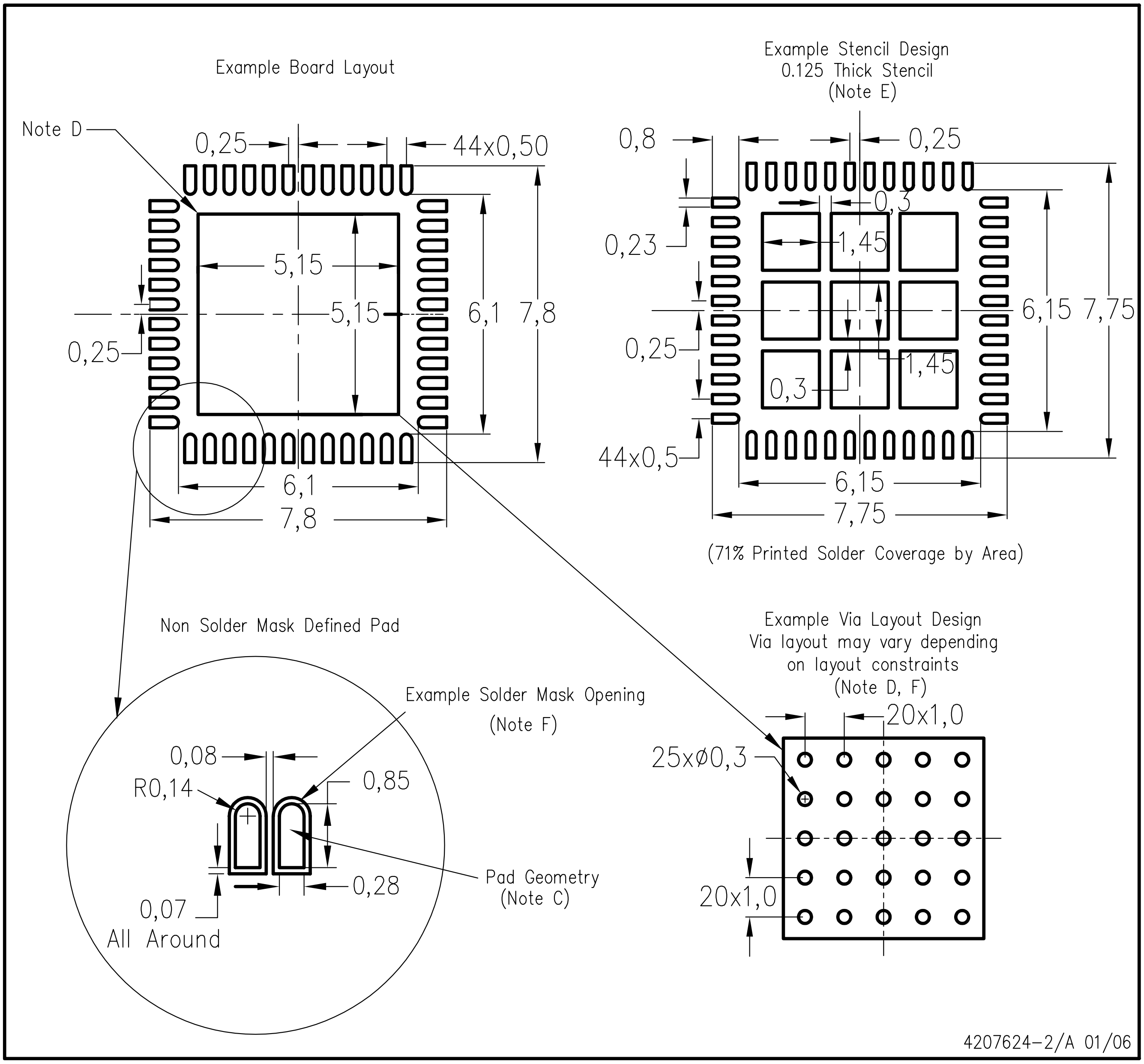


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGZ (S-PQFP-N48)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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