ALPHA & OMEGA SEMICONDUCTOR

AOZ1015

EZBuck™ 1.5A Synchronous Buck Regulator

General Description

The AOZ1015 is a high efficiency, simple to use, 1.5A buck regulator. The AOZ1015 works from a 4.5V to 16V input voltage range, and provides up to 1.5A of continuous output current with an output voltage adjustable down to 0.8V.

The AOZ1015 comes in an SO-8 package and is rated over a -40°C to +85°C ambient temperature range.

Features

- 4.5V to 16V operating input voltage range
- 130mΩ internal PFET switch for high efficiency: up to 95%
- Internal Schottky diode
- Internal soft start
- Output voltage adjustable to 0.8V
- 1.5A continuous output current
- Fixed 500kHz PWM operation
- Cycle-by-cycle current limit
- Short-circuit protection
- Under voltage lockout
- Output over voltage protection
- Thermal shutdown
- Small size SO-8 package

Applications

- Point of load DC/DC conversion
- PCIe graphics cards
- Set top boxes
- DVD drives and HDD
- LCD panels
- Cable modems
- Telecom/networking/datacom equipment

Typical Application

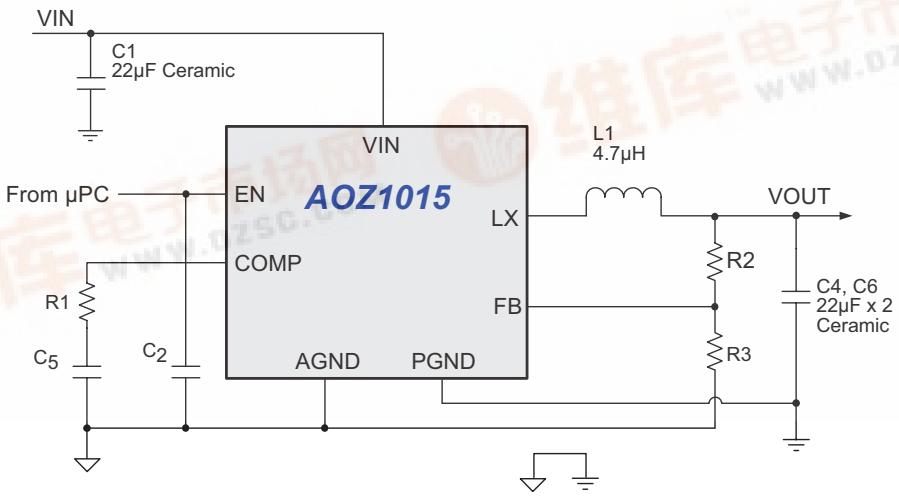


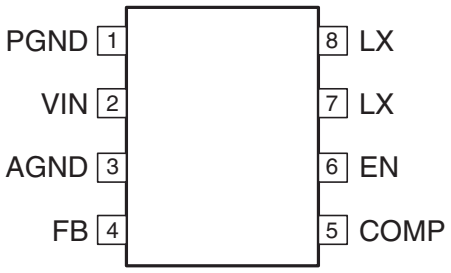
Figure 1. 3.3V/1.5A Buck Regulator

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1015AI	-40°C to +85°C	SO-8	RoHS

All AOS Products are offering in packaging with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

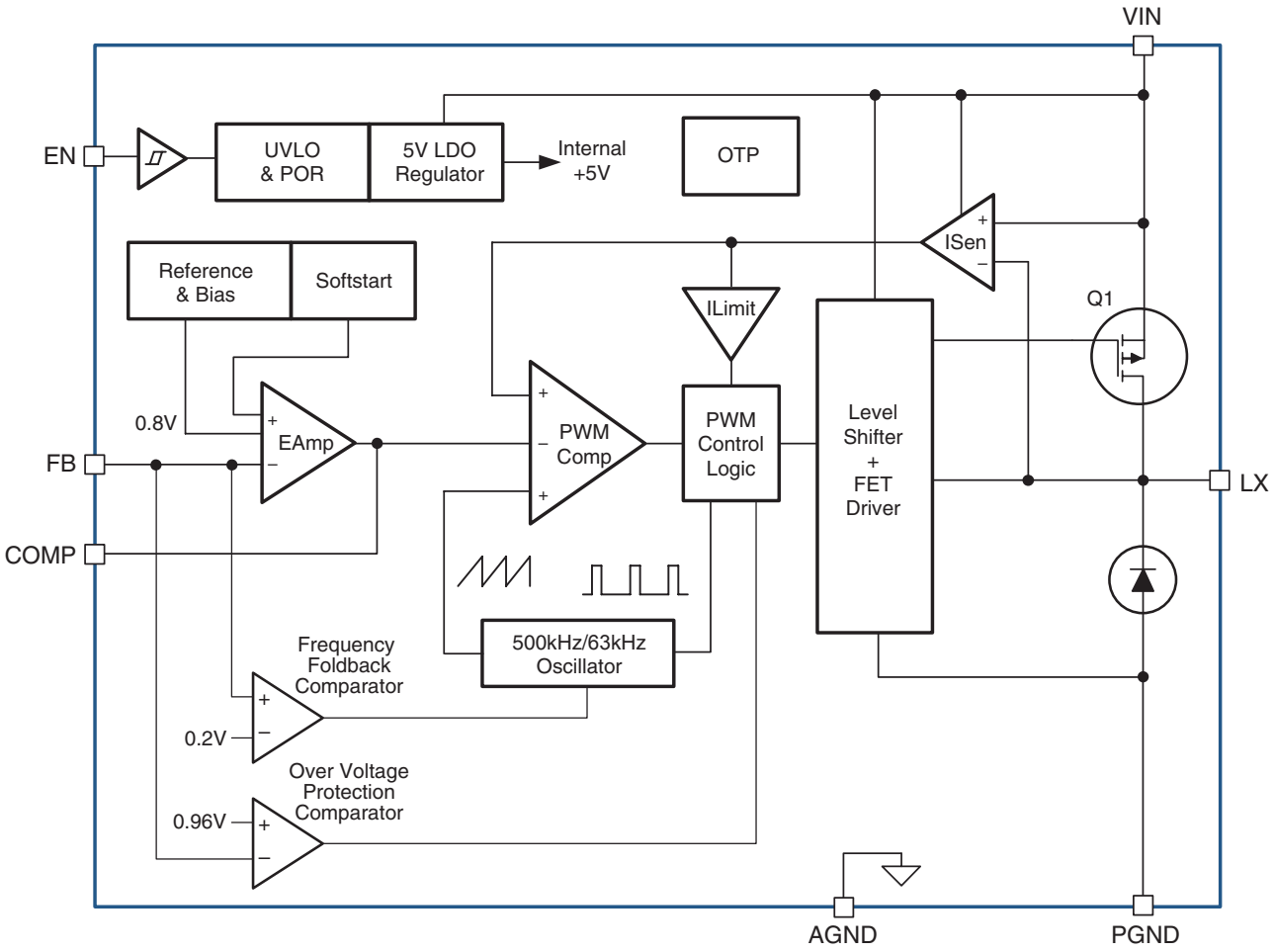


SO-8
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGND	Power ground. Electrically needs to be connected to AGND.
2	V_{IN}	Supply voltage input. When V_{IN} rises above the UVLO threshold the device starts up.
3	AGND	Reference connection for controller section. Also used as thermal connection for controller section. Electrically needs to be connected to PGND.
4	FB	The FB pin is used to determine the output voltage via a resistor divider between the output and GND.
5	COMP	External loop compensation pin.
6	EN	The enable pin is active HIGH. Connect EN pin to V_{IN} if not used. Do not leave the EN pin floating.
7, 8	LX	PWM output connection to inductor. Thermal connection for output stage.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	18V
LX to AGND	-0.7V to V_{IN}+0.3V
EN to AGND	-0.3V to V_{IN}+0.3V
FB to AGND	-0.3V to 6V
COMP to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(1) Human Body Model Machine Model	 2kV 200V

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF. The machine model is a 200pF capacitor discharged directly into each pin.

Recommend Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 16V
Output Voltage Range	0.8V to V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance SO-8 (Θ_{JA})(2)	87°C/W

Note:

2. The value of Θ_{JA} is measured with the device mounted on 1-in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.(3)

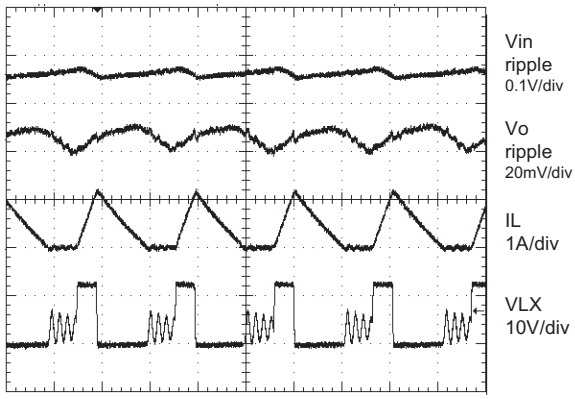
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**4.5**		**16**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		**4.00** **3.70**		V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0, V_{FB} = 1.2V, V_{EN} > 1.2V		**2**	**3**	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		**1**	**10**	µA
V_{FB}	Feedback Voltage		0.782	0.8	0.818	V
	Load Regulation			0.5		%
	Line Regulation			0.5		%
I_{FB}	Feedback Voltage Input Current				200	nA
ENABLE						
V_{EN}	EN Input Threshold	Off Threshold On Threshold	 **2.0**		**0.6**	V
V_{HYS}	EN Input Hysteresis			**100**		mV
I_{EN}	EN Input Current				1	µA
MODULATOR						
f_O	Frequency		400	500	600	kHz
D_{MAX}	Maximum Duty Cycle		100			%
D_{MIN}	Minimum Duty Cycle				6	%
	Error Amplifier Voltage Gain			500		V / V
	Error Amplifier Transconductance			200		µA / V
PROTECTION						
I_{LIM}	Current Limit		2		3.6	A
V_{PR}	Output Over-Voltage Protection Threshold	Off threshold On threshold	920 820	960 860	1000 900	mV
T_J	Over-Temperature Shutdown Limit			150		°C
t_{SS}	Soft Start Interval			2.2		ms
OUTPUT STAGE						
	High-Side Switch On-Resistance	V_{IN} = 12V V_{IN} = 5V		97 166	130 200	mΩ

Note:
3. Specification in **BOLD** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

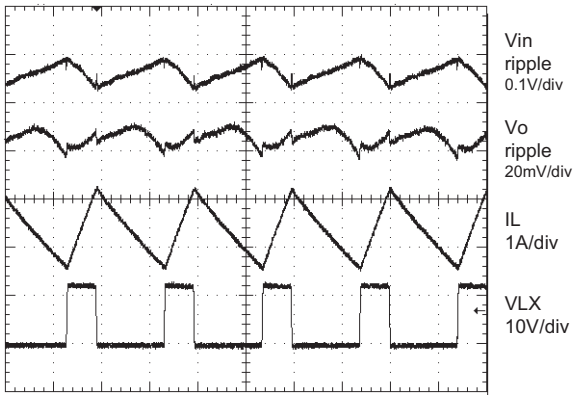
Typical Performance Characteristics

Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.

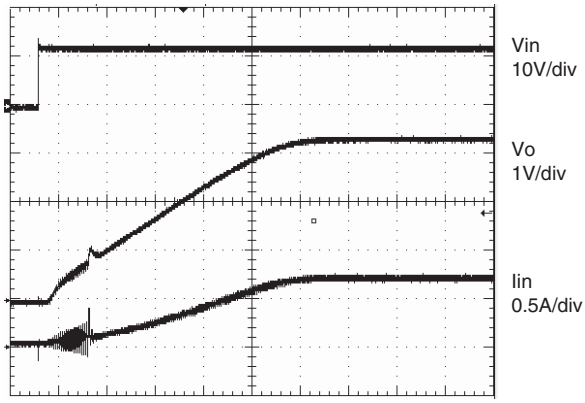
Light Load (DCM) Operation



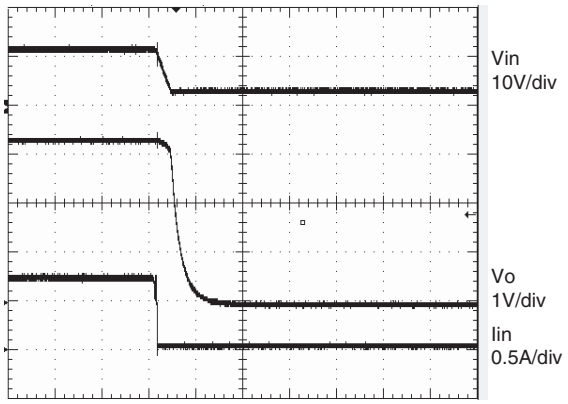
Full Load (CCM) Operation



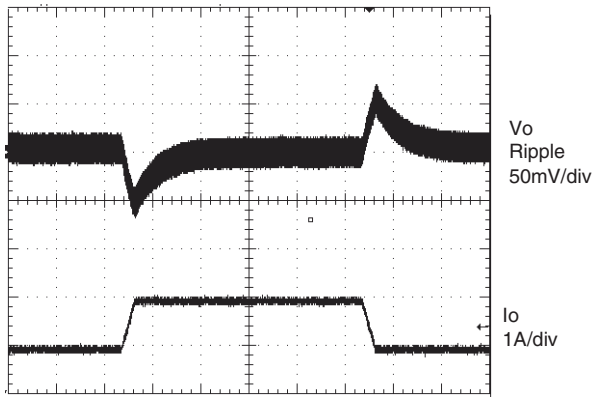
Startup to Full Load



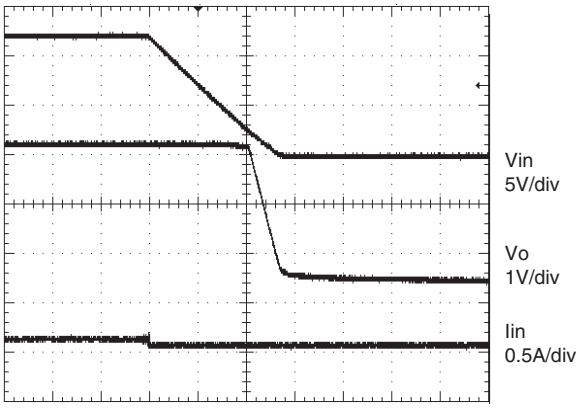
Full Load to Turnoff



50% to 100% Load Transient



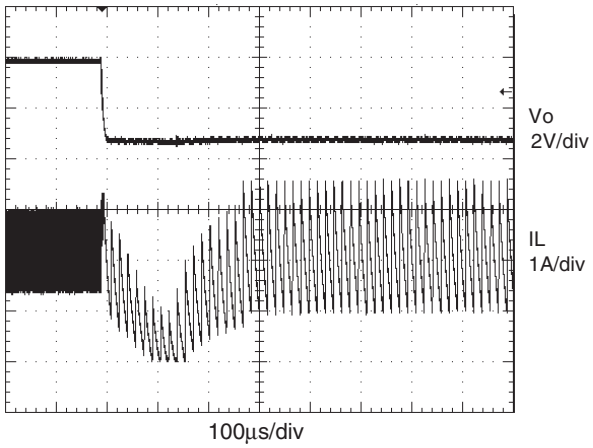
Light Load to Turnoff



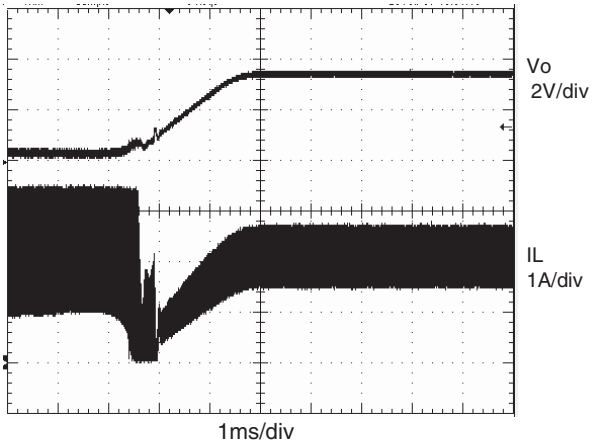
Typical Performance Characteristics *(Continued)*

Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.

Short Circuit Protection

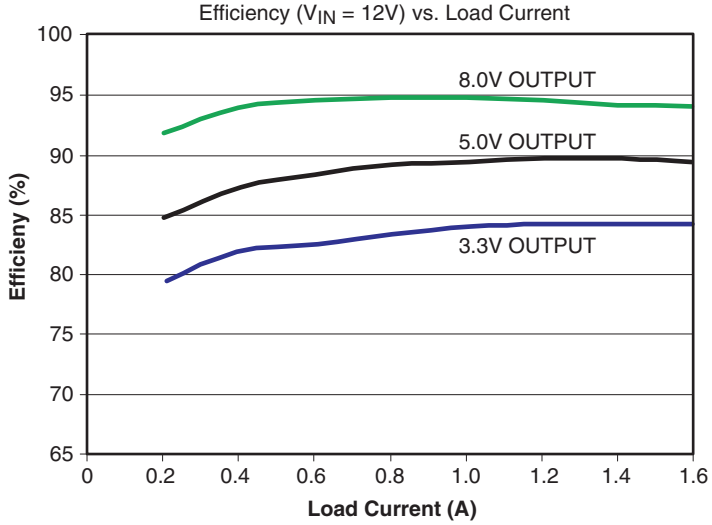


Short Circuit Recovery



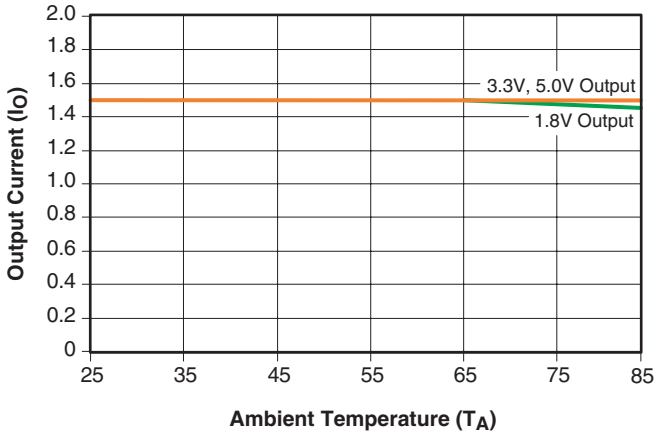
AOZ1015AI Efficiency

Efficiency (V_{IN} = 12V) vs. Load Current

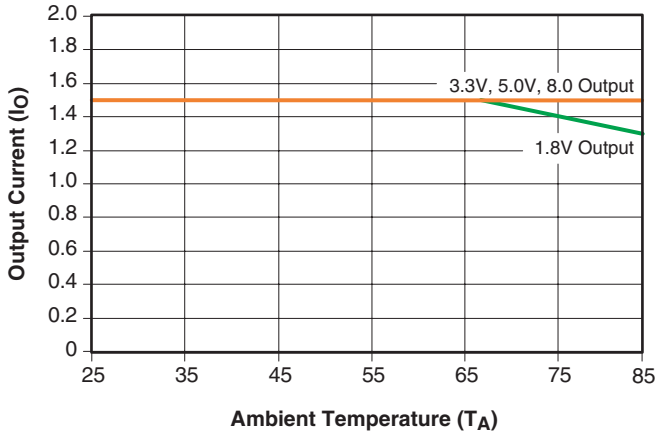


Thermal de-rating curves for SO-8 package part under typical input and output condition based on the evaluation board. 25°C ambient temperature and natural convection (air speed < 50LFM) unless otherwise specified.

Derating Curves at 5V Input



Derating Curves at 12V Input



Detailed Description

The AOZ1015 is a current-mode step down regulator with integrated high side PMOS switch and a low side free-wheeling Schottky diode. It operates from a 4.5V to 16V input voltage range and supplies up to 1.5A of load current. The duty cycle can be adjusted from 6% to 100% allowing a wide range of output voltages. Features include; enable control, Power-On Reset, input under voltage lockout, fixed internal soft-start and thermal shut down.

The AOZ1015 is available in an SO-8 package.

Enable and Soft Start

The AOZ1015 has an internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.0V and voltage on EN pin is HIGH. In the soft start process, the output voltage is typically ramped to regulation voltage in 2.2ms. The 2.2ms soft start time is set internally.

The EN pin of the AOZ1015 is active HIGH. Connect the EN pin to V_{IN} if the enable function is not used. Pulling EN to ground will disable the AOZ1015. Do not leave it open. The voltage on the EN pin must be above 2.0V to enable the AOZ1015. When voltage on EN falls below 0.6V, the AOZ1015 is disabled. If an application circuit requires the AOZ1015 to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1015 integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is the sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal Schottky diode to output.

The AOZ1015 uses a P-Channel MOSFET as the high side switch. It saves the bootstrap capacitor normally seen in a circuit which is using an NMOS switch. It allows 100% turn-on of the upper switch to achieve linear regulation mode of operation. The minimum voltage drop from V_{IN} to V_O is the load current X DC resistance of MOSFET + DC resistance of the buck inductor. It can be calculated by equation below:

$$V_{O\_MAX} = V_{IN} - I_O \times (R_{DS(ON)} + R_{inductor})$$

where;

V_{O_MAX} is the maximum output voltage,

V_{IN} is the input voltage from 4.5V to 16V,

I_O is the output current from 0A to 1.5A,

$R_{DS(ON)}$ is the on resistance of the internal MOSFET, the value is between 97mΩ and 200mΩ depending on input voltage and junction temperature, and

$R_{inductor}$ is the inductor DC resistance.

Switching Frequency

The AOZ1015 switching frequency is fixed and set by an internal oscillator. The actual switching frequency could range from 400kHz to 600kHz due to device variation.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_2 and R_3. Usually, a design is started by picking a fixed R_3 value and calculating the required R_2 with equation below.

$$V_O = 0.8 \times \left(1 + \frac{R_2}{R_3}\right)$$

Some standard values of R_2, R_3 for most commonly used output voltage values are listed in Table 1.

Table 1.

V_O (V)	R_2 (kΩ)	R_3 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

The combination of R_2 and R_3 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Since the switch duty cycle can be as high as 100%, the maximum output voltage can be set as high as the input voltage minus the voltage drop on upper PMOS and inductor.

Protection Features

The AOZ1015 has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1015 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

The cycle by cycle current limit threshold is set between 2.0A and 3.6A. When the load current reaches the current limit threshold, the cycle by cycle current limit circuit turns off the high side switch immediately to terminate the current duty cycle. The inductor current stop rising. The cycle by cycle current limit protection directly limits inductor peak current. The average inductor current is also limited due to the limitation on peak inductor current. When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreases.

The AOZ1015 has internal short circuit protection to protect itself from catastrophic failure under output short circuit conditions. The FB pin voltage is proportional to the output voltage. Whenever FB pin voltage is below 0.2V, the short circuit protection circuit is triggered. As a result, the converter is shut down and hiccups at a frequency equal to 1/8 of normal switching frequency. The converter will start up via a soft start once the short circuit condition is resolved. In short circuit protection mode, the inductor average current is greatly reduced because of the low hiccup frequency.

Output Over Voltage Protection (OVP)

The AOZ1015 monitors the feedback voltage. When the feedback voltage is higher than 960mV, it immediately turns-off the PMOS to protect the output voltage overshoot at fault condition. When feedback voltage is lower than 860mV, the PMOS is allowed to turn on in the next cycle.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4V, the converter starts operation. When input voltage falls below 3.7V, the converter will stop switching.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side PMOS if the junction temperature exceeds 150°C.

Application Information

The basic AOZ1015 application circuit is shown in Figure 1. Component selection is explained below.

Input Capacitor

The input capacitor (C_1 in Figure 1) must be connected to the V_{IN} pin and PGND pin of the AOZ1015 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor (C_d in Figure 1), usually 1µF, should be connected to the V_{IN} pin and AGND pin for stable operation of the AOZ1015. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

If let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

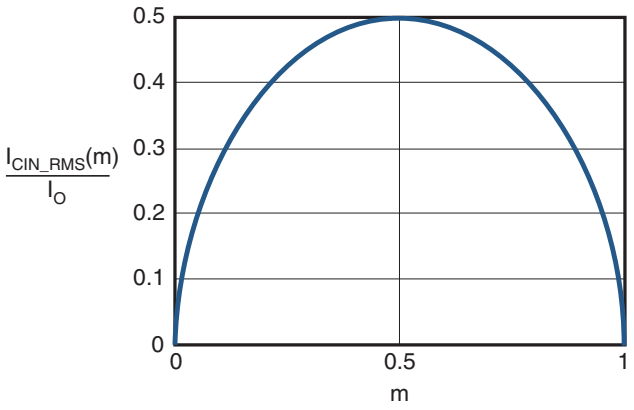


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at the worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitors or aluminum electrolytic capacitors may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufacturers is based on a certain device life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For a given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires a larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through the inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. They cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where,

C_O is output capacitor value, and

ESR_{CO} is the equivalent series resistance of the output capacitor.

When a low ESR ceramic capacitor is used as an output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is primarily caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is primarily decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of the output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, the output capacitor could be overstressed.

Loop Compensation

The AOZ1015 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is the dominant pole and can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value, and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter close loop transfer function to get the desired gain and phase. Several different types of compensation networks can be used for the AOZ1015. In most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

The FB pin and the COMP pin are the inverting input and the output of the internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V,

G_{VEA} is the error amplifier voltage gain, which is 500 V/V, and

C_C is compensation capacitor.

The zero given by the external compensation network, capacitor C_C (C_5 in Figure 1) and resistor R_C (R_1 in Figure 1), is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where the control loop has unity gain. The crossover frequency is also called the converter bandwidth. Generally, a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high due to system stability concern. When designing the compensation loop, converter stability under all line and load conditions must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of the switching frequency. The AOZ1015 operates at a fixed switching frequency range from 40 0kHz to 600kHz. It is recommended to choose a crossover frequency less than 50kHz.

$$f_C = 50kHz$$

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where;

f_C is the desired crossover frequency,

V_{FB} is 0.8V,

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V, and

G_{CS} is the current sense circuit transconductance, which is 5.64 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

The previous equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Consideration

In the AOZ1015 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the V_{IN} pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then returns to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the PGND pin of the AOZ1015, to the LX pins of the AOZ1015. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ1015.

In the AOZ1015 buck regulator circuit, the two major power dissipating components are the AOZ1015 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of the inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual AOZ1015 junction temperature can be calculated with power dissipation in the AOZ1015 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta + T_{ambient}$$

The maximum junction temperature of the AOZ1015 is 150°C, which limits the maximum load current capability. Please see the thermal de-rating curves for the maximum load current of the AOZ1015 under different ambient temperatures.

The thermal performance of the AOZ1015 is strongly affected by the PCB layout. Extra care should be taken by users during the design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electronic and thermal performance. Figure 3 illustrates a single layer PCB layout example as reference.

1. Do not use thermal relief connection to the V_{IN} and the PGND pins. Pour a maximized copper area to the PGND pin and the V_{IN} pin to help thermal dissipation.
2. The input capacitors should be connected as close as possible to the V_{IN} and PGND pins.
3. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin. In this case, a decoupling capacitor should be connected between V_{IN} and AGND.
4. Make the current trace from LX pins to L to C_O to the PGND as short as possible.
5. Pour copper plane on all unused board area and connect it to stable DC nodes, like V_{IN}, GND or V_{OUT}.
6. The two LX pins are connected to the internal PFET drain. They are low resistance thermal conduction path and a noisy switching node. Connecting a copper plane to the LX pin to help thermal dissipation. This copper plane should not be too large otherwise switching noise may be coupled to other parts of the circuit.
7. Keep sensitive signal traces such as trace connecting FB and COMP away from the LX pins.

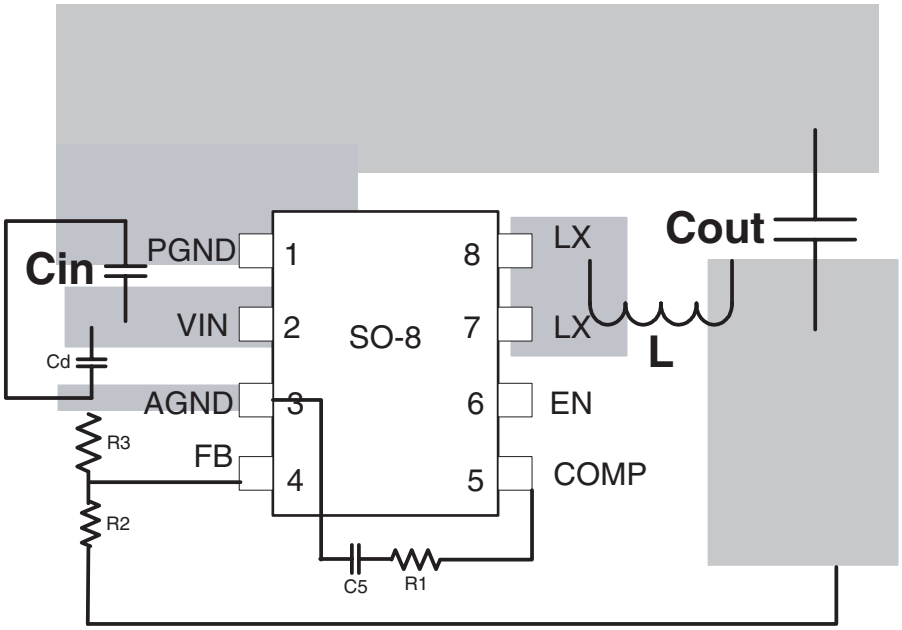
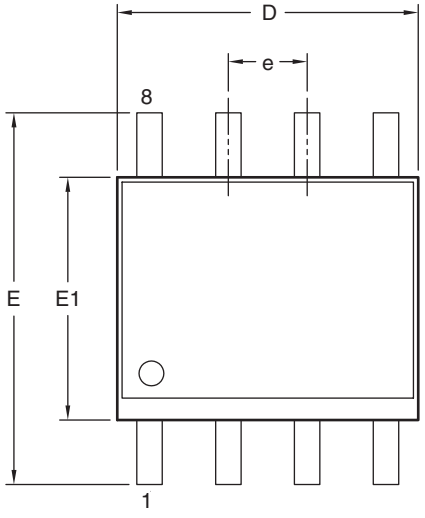
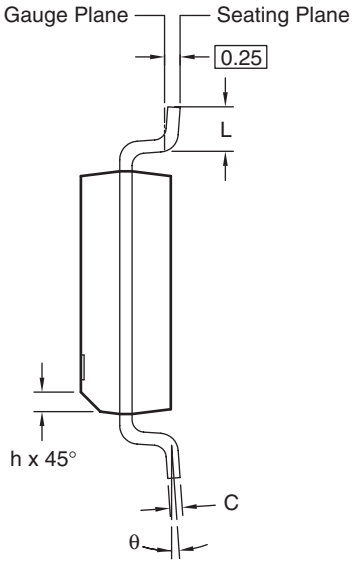
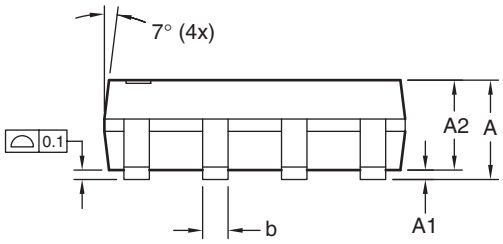


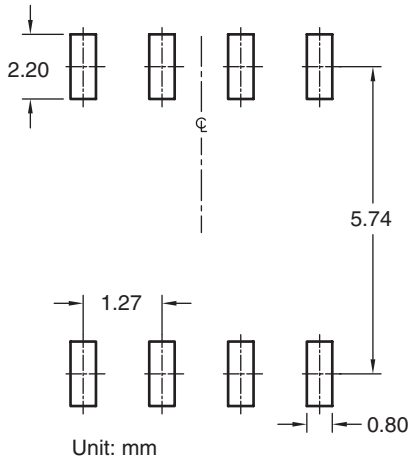
Figure 3. AOZ1015 PCB Layout

Package Dimensions, SO-8L









Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

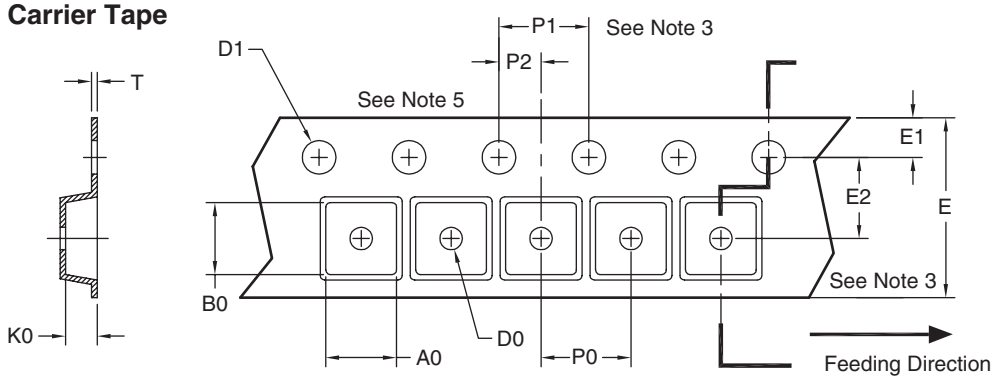
Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions

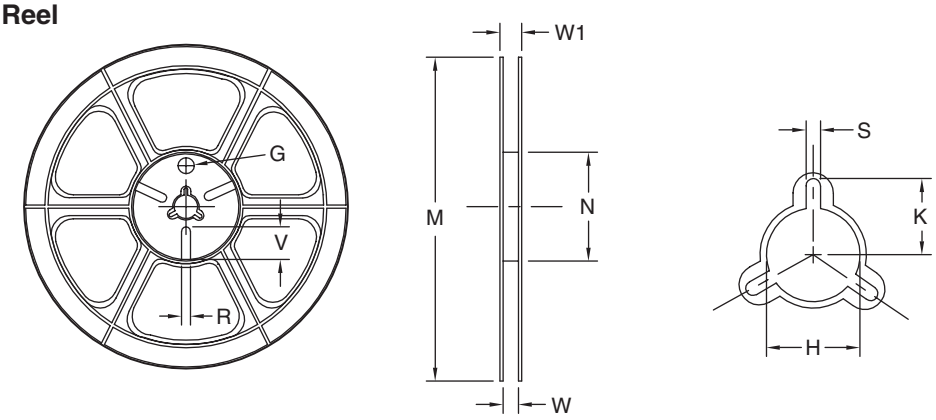
SO-8 Carrier Tape



Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

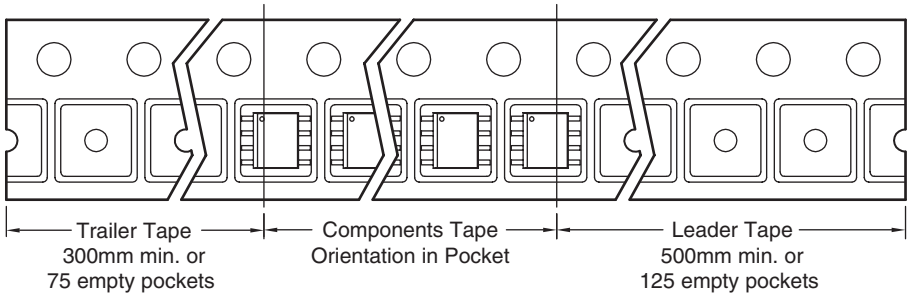
SO-8 Reel



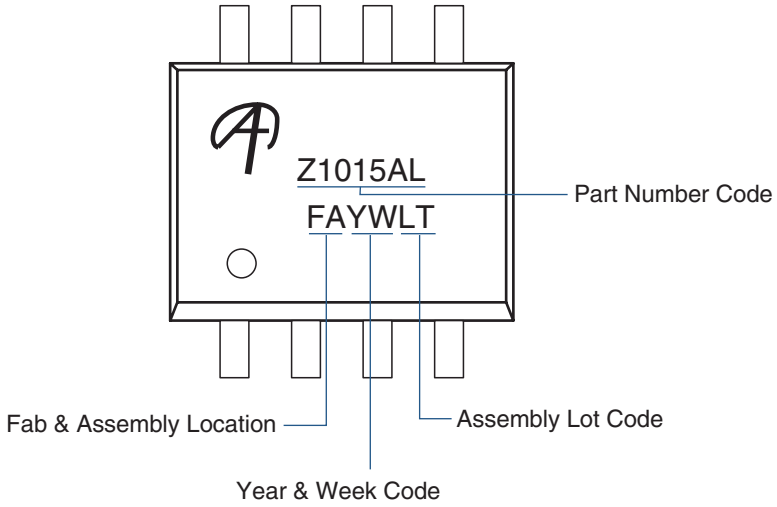
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

SO-8 Tape

Leader/Trailer & Orientation



AOZ1015 Package Marking



This datasheet contains preliminary data; supplementary data may be published at a later date.
Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.