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## Features

- Hardware
  - ATSTK94 Onboard Features
    - Programmable Switches, LEDs and Alphanumeric Displays
    - Two RS232 Compatible Serial Ports
    - Multiple Clocks (4 MHz, 18.432 MHz, 32.768 kHz and Manual)
    - 2-wire Serial Interface for Communication
    - Easy Access to all FPSLIC Pins via Headers
    - Push Button AVR and FPSLIC Reset
  - Supports both Drop-In and In-System Programming (ISP)
  - Runs Off Portable 9V DC Power Supply
  - Designed to Work with Atmel System Designer™ 1.0 or Above
- Software
  - Atmel's System Designer
    - Atmel's AVR Studio®
    - Atmel's Configurator Programming System (CPS)
    - Co-verification, Powered by Mentor Graphics
    - Exemplar's LeonardoSpectrum™
    - Model Technology™'s ModelSim®
    - Several C Compiler Evaluation Copies
  - Atmel's Integrated Development System (IDS) – FPGA Place & Route Tool
  - Supports Windows® 95/98/2000/Me and WindowsNT®
  - Online Help
- Contents
  - ATSTK94 Starter Kit Board with 1 Configurator
  - ATDH2225 Programming Dongle with 10-pin Ribbon Cable
  - 9V DC, 200 mA, 2.1 mm Center Positive Power Supply
  - Atmel System Designer CD with Evaluation License (4 Months)
  - Detailed User Guide including Complete Board Schematics
  - Software Tutorial and Sample Designs on Floppy Disk

## Description

Atmel's AT94K Starter Kit (ATSTK94) allows designers to, quickly and economically, evaluate Atmel's family of AT94K Field Programmable System Level Integrated Circuit (FPSLIC) devices and AT17 FPSLIC Configuration Memory devices. The ATSTK94, see Figure 1, board connects to any x86 PC via the parallel port through a 10-pin header cable to program the AT17 FPSLIC Configuration EEPROM, which in turn programs the AT94K FPSLIC device. A truly portable solution, which allows engineers to prototype and develop designs from their lab bench or office.

# Starter Kit

FPSLIC™

# Programmable SLI ATSTK94

Rev. 2309B–FPSLI–01/02

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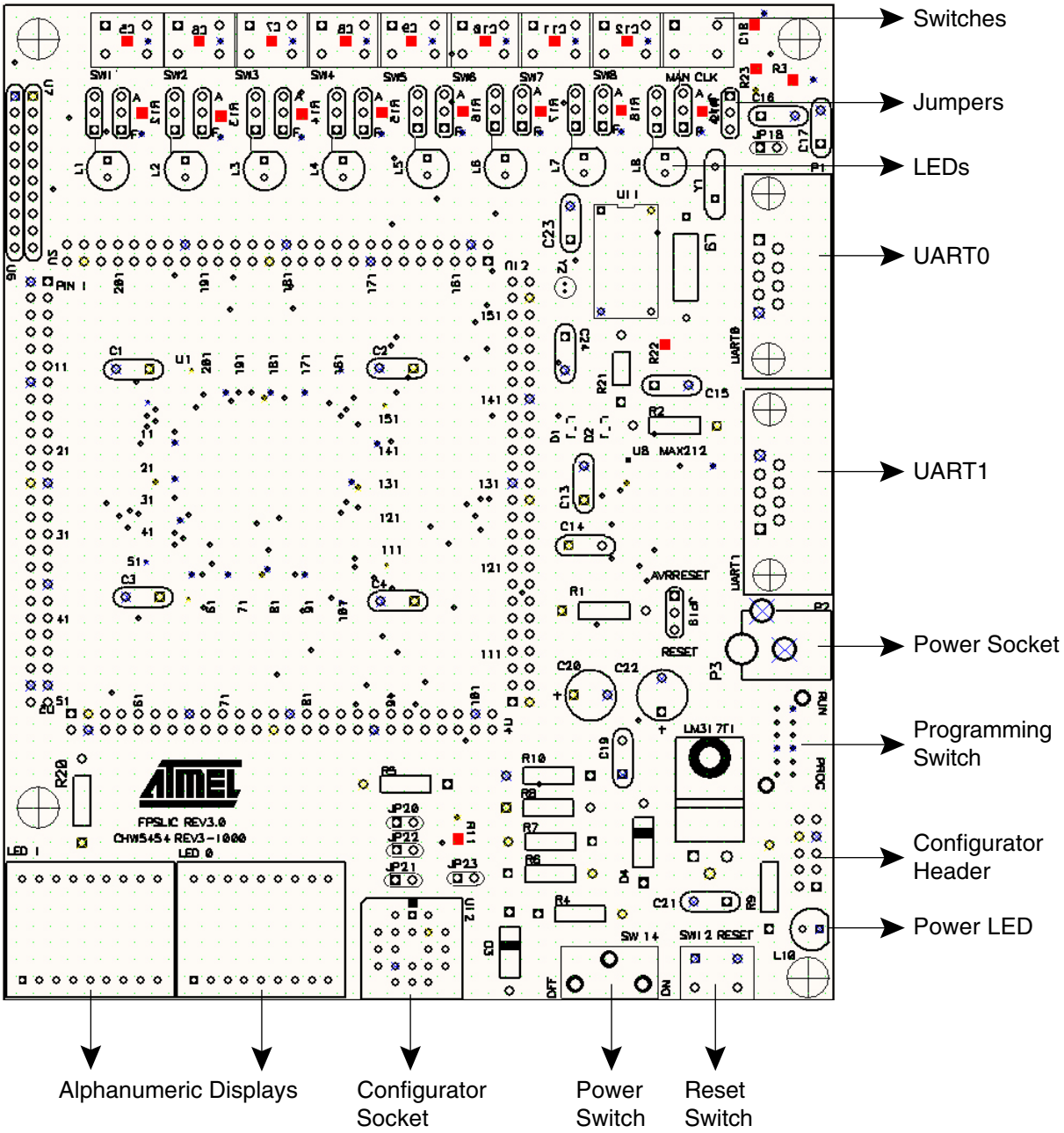
**Figure 1.** ATSTK94 FPSLIC Starter Kit Board



## Switches, LEDs, and Alphanumeric Displays

The user configures each Programmable Switch or LED for use, with either the FPGA or AVR portion of the FPSLIC device. Furthermore, some switches may be configured for use as AVR External Interrupts allowing simulation of external events. The board features four Alphanumeric Displays which are connected to I/O pins of the embedded AT40KAL FPGA core.

### Program and Run Switch

The Program and Run Switch controls the connection from the download cable to the Configurator and the Configurator to the FPSLIC.

In the PROG position you can use the download cable and CPS to program the configuration memory with your FPSLIC Bitstream file generated by System Designer.

In the Run position the FPSLIC device will load the Bitstream file and run your design. If the design does not start, you can use the RESET button with JP19 in the RESET position to force a reconfiguration of the device. In the Run position, the configurator will boot the FPSLIC device with the current program.

### ISP and Reset Connections

There are 2 device reset connections in the FPSLIC device.

The AVR RESET will reset the AVR and start from the reset vector in the interrupt table.

RESET will cause the whole device to reset and reboot from the Configurator.

SW12 is used to perform the reset. Jumper 19 is used to determine whether it will be an AVR reset or a full device reset, see Table 1.

If you have logic RESET signal in your design, you cannot use SW12 to perform this reset; you should use one of the switches SW 1 – 8 to perform your design reset. Your design reset can be connected to any User IO on the FPGA side of FPSLIC. If you are using SW1 – 8, then you should use Pin locks to assign the correct user IO for the correct Switch.

**Table 1.** Reset Connections

| RESET | Source | Pin | Hardware Settings |
|---|---|---|---|
| RESET | SW12 | 108 | JP19 Set to RESET (Default) |
| AVR RESET | SW12 | 48 | JP19 Set to AVR RESET |

### Button/Switch Connections

The jumpers, located next to the buttons/switches control the button/switch connections, see Table 2.

The left side of the jumpers are connected to LEDs, the right side of the jumpers are connected to Switches.

The A and F markings indicate a connection to the AVR or the FPGA.

When you press the switch it generates a “1”.

**Table 2.** Switch Connections

| Switch | Destination | Pin | Hardware Settings |
|---|---|---|---|
| SW1 | FPGA User IO | 202 | Jumper Set to F |
| SW2 | FPGA User IO | 198 | Jumper Set to F |
| SW3 | FPGA User IO | 192 | Jumper Set to F |
| SW4 | FPGA User IO | 188 | Jumper Set to F |
| SW5 | FPGA User IO | 180 | Jumper Set to F |
| SW6 | FPGA User IO | 176 | Jumper Set to F |
| SW7 | FPGA User IO | 172 | Jumper Set to F |
| SW8 | FPGA User IO | 168 | Jumper Set to F |
| SW1 | AVR Interrupt INTP0 | 135 | Jumper Set to A |
| SW2 | AVR Interrupt INTP1 | 145 | Jumper Set to A |
| SW3 | AVR Interrupt INTP2 | 146 | Jumper Set to A |
| SW4 | AVR Interrupt INTP3 | 152 | Jumper Set to A |
| SW5 | AVR PortE PE0 | 109 | Jumper Set to A |
| SW6 | AVR PortE PE1 | 110 | Jumper Set to A |
| SW7 | AVR PortE PE2 | 113 | Jumper Set to A |
| SW8 | AVR PortE PE3 | 122 | Jumper Set to A |

## LED Connections

The jumpers, located next to the LEDs, control the LED connections.

Alternate jumpers connect to the switches, see Table 3, and to the LEDs. A white line on the silk screen indicates whether the jumper is for LED or the Switch.

With the A F text the right way up the left most Jumper is for the LED 1. The A and F markings indicate a connection to the AVR or the FPGA.

When you drive a “1” to the LED it will light.

**Table 3.** LED Connections

| LED | Source | Pin | Hardware Settings |
|---|---|---|---|
| L1 | FPGA User IO | 200 | Jumper Set to F |
| L2 | FPGA User IO | 196 | Jumper Set to F |
| L3 | FPGA User IO | 190 | Jumper Set to F |
| L4 | FPGA User IO | 186 | Jumper Set to F |
| L5 | FPGA User IO | 178 | Jumper Set to F |
| L6 | FPGA User IO | 174 | Jumper Set to F |
| L7 | FPGA User IO | 170 | Jumper Set to F |
| L8 | FPGA User IO | 166 | Jumper Set to F |
| L1 | AVR PortD PD0 | 111 | Jumper Set to A |
| L2 | AVR PortD PD1 | 112 | Jumper Set to A |
| L3 | AVR PortD PD2 | 114 | Jumper Set to A |

**Table 3.** LED Connections

| LED | Source | Pin | Hardware Settings |
|---|---|---|---|
| L4 | AVR PortD PD3 | 120 | Jumper Set to A |
| L5 | AVR PortD PD4 | 121 | Jumper Set to A |
| L6 | AVR PortD PD5 | 126 | Jumper Set to A |
| L7 | AVR PortD PD6 | 127 | Jumper Set to A |
| L8 | AVR PortD PD7 | 134 | Jumper Set to A |

## Alphanumeric Connections

There are 4 digits of Alphanumeric on the board. The connections to the Alphanumeric are shared between both bits on the same device, see Table 4. This means that Bit 0 and Bit 1 share connections, and Bit 2 and Bit 3 share connections for all the segments, see Figure 2. The difference in connection is in the cathode connection that selects between the 2 digits. The cathodes should be driven with a 1/10 Duty Cycle and a 0.1 ms Pulse Width, see Table 5.

**Table 4.** Alphanumeric Connections

| LED 0 | Source | Pin | LED 1 | Source | Pin |
|---|---|---|---|---|---|
| Anode A | FPGA User IO | 94 | Anode A | FPGA User IO | 73 |
| Anode B | FPGA User IO | 98 | Anode B | FPGA User IO | 80 |
| Anode C | FPGA User IO | 97 | Anode C | FPGA User IO | 76 |
| Anode D | FPGA User IO | 93 | Anode D | FPGA User IO | 72 |
| Anode E | FPGA User IO | 81 | Anode E | FPGA User IO | 59 |
| Anode F | FPGA User IO | 82 | Anode F | FPGA User IO | 60 |
| Anode G | FPGA User IO | 87 | Anode G | FPGA User IO | 66 |
| Anode H | FPGA User IO | 89 | Anode H | FPGA User IO | 69 |
| Anode J | FPGA User IO | 91 | Anode J | FPGA User IO | 70 |
| Anode K | FPGA User IO | 88 | Anode K | FPGA User IO | 68 |
| Anode L | FPGA User IO | 86 | Anode L | FPGA User IO | 65 |
| Anode M | FPGA User IO | 83 | Anode M | FPGA User IO | 61 |
| Anode N | FPGA User IO | 92 | Anode N | FPGA User IO | 71 |
| Anode P | FPGA User IO | 84 | Anode P | FPGA User IO | 63 |
| Anode D.P. | FPGA User IO | 95 | Anode D.P. | FPGA User IO | 74 |
| Cathode Bit 1 | FPGA User IO | 85 | Cathode Bit 1 | FPGA User IO | 64 |
| Cathode Bit 2 | FPGA User IO | 96 | Cathode Bit 2 | FPGA User IO | 75 |

**Figure 2.** LEDs

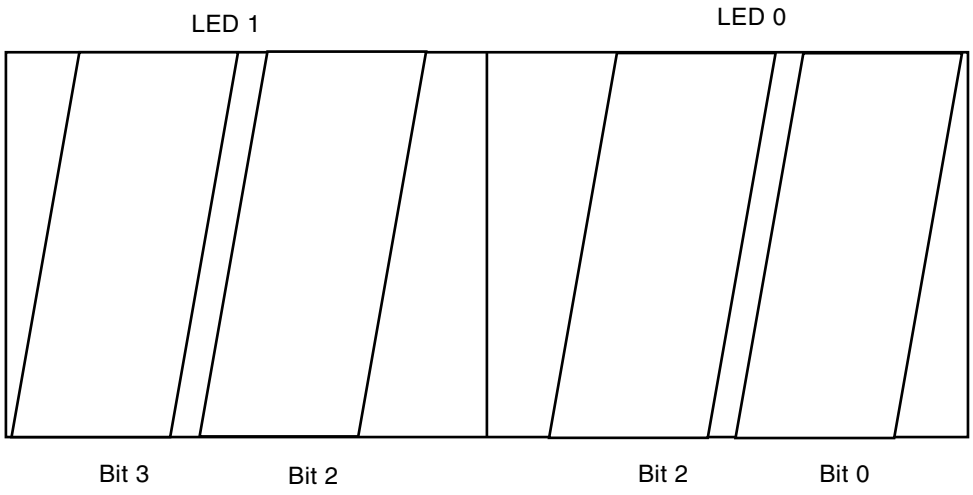



**Table 5.** ASCII Code Table

| Value | DP | P | N | M | L | K | J | H | G | F | E | D | C | B | A |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 3 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 5 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| a | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| b | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| c | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| d | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| e | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| f | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| . | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

## RS232-compatible UARTs

The RS232-compatible UARTs allow for communication between the two on-board UARTs through the null-modem cable. It is also possible for communication between the UARTs and other devices, such as your PC, by using a simple terminal program.

### UART Connections

The 2 UART connections, see Table 6, are made to DB9 connectors. Printf commands are sent out on UART 0.

**Table 6.** UART Connections

| UART | Source /Destination | Pin | Hardware Settings |
|---|---|---|---|
| UART 0 | RX0 | 140 | Connect Cable to UART0 |
| UART 0 | TX0 | 141 | Connect Cable to UART 0 |
| UART1 | RX1 | 149 | Connect Cable to UART 1 |
| UART1 | TX1 | 150 | Connect Cable to UART 1 |

## Multiple Clocks

There are multiple clock circuits on the Starter Kit. A Manual Clock or the 4 MHz Oscillator are connected to 2 of the FPGA Global Clock pins. The 32,768 KHz (for the implementation of the Real Time Clock calculations), 4 MHz, or 18.432 MHz can be used to drive the AVR. The FPGA has 8 Global Clocks, 2 of these (GCLK5 and GCLK6) can also be driven from the AVR system Clock. GCLK6 can alternatively be driven from the Watchdog timer or one of the timer counters. For full details on the Clock circuits in the FPSLIC device please refer to the AT94K datasheet available on the Atmel web site, at http://www.atmel.com/atmel/acrobat/doc1138.pdf.

**Table 7.** Clock Connections

| Frequency | Destination | Pin | Hardware Settings |
|---|---|---|---|
| Manual Clock | FPGA GCLK7 | 162 | Use MAN CLK Switch (SW9) to Pulse Clock |
| Available Global Clocks | FPGA GCLK1<br>FPGA GCLK2<br>FPGA GCLK3<br>FPGA GCLK4<br>FPGA GCLK7<br>FPGA GCLK8 | 4<br>47<br>57<br>100<br>162<br>204 | |
| 32,768 KHz Crystal | AVR TOSC 1 | 147 | None |
| 4 MHz Oscillator | AVR System Clock | 138 | For Rev2 – JP17 towards side of board, JP18 is unconnected.<br>For Rev3 and beyond –Position of JP17 is changed, it is aligned with FPGA and AVR jumpers. JP17 is connected towards the inner side of the board, JP18 is unconnected. |
| 18.432 MHz Crystal | AVR System Clock | 138 | For Rev2 – JP17 towards middle of board, JP18 connected.<br>For Rev3 and beyond – Position of JP17 is changed, it is aligned with FPGA and AVR jumpers. JP17 is connected towards the edge of the board, JP18 is connected. |

## 2-wire Serial Interface

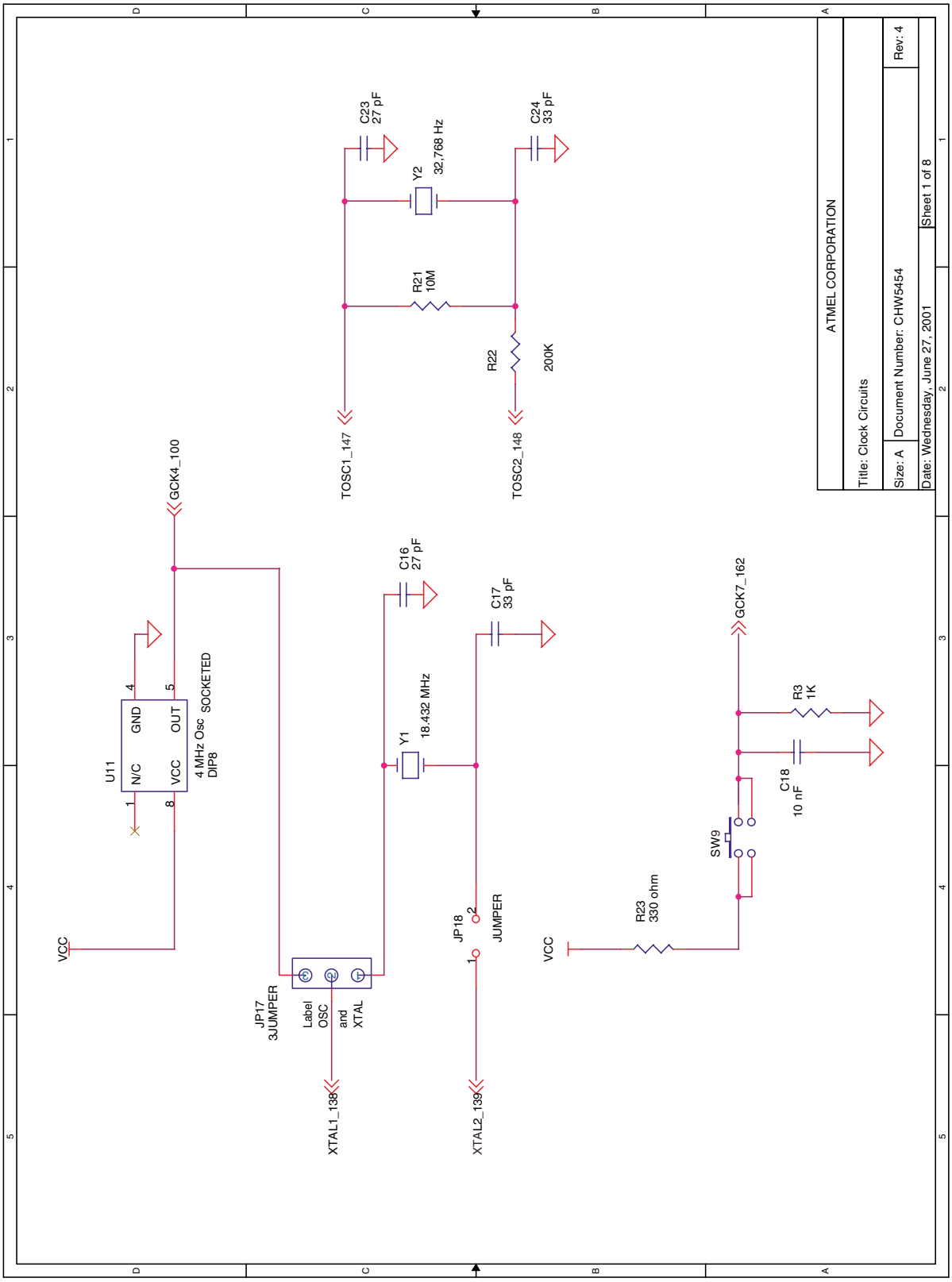
The 2-wire Serial Interface is the protocol from which the FPSLIC device receives configuration data from the AT17LV010 Configuration Memory. The maximum size of an AT94K40 design is approximately 800 kbits, thus leaving approximately 200 kbits of unused space. By using the 2-wire Serial Interface, it is possible to use the unused 200 kbits as external data storage memory.

## Related Documents

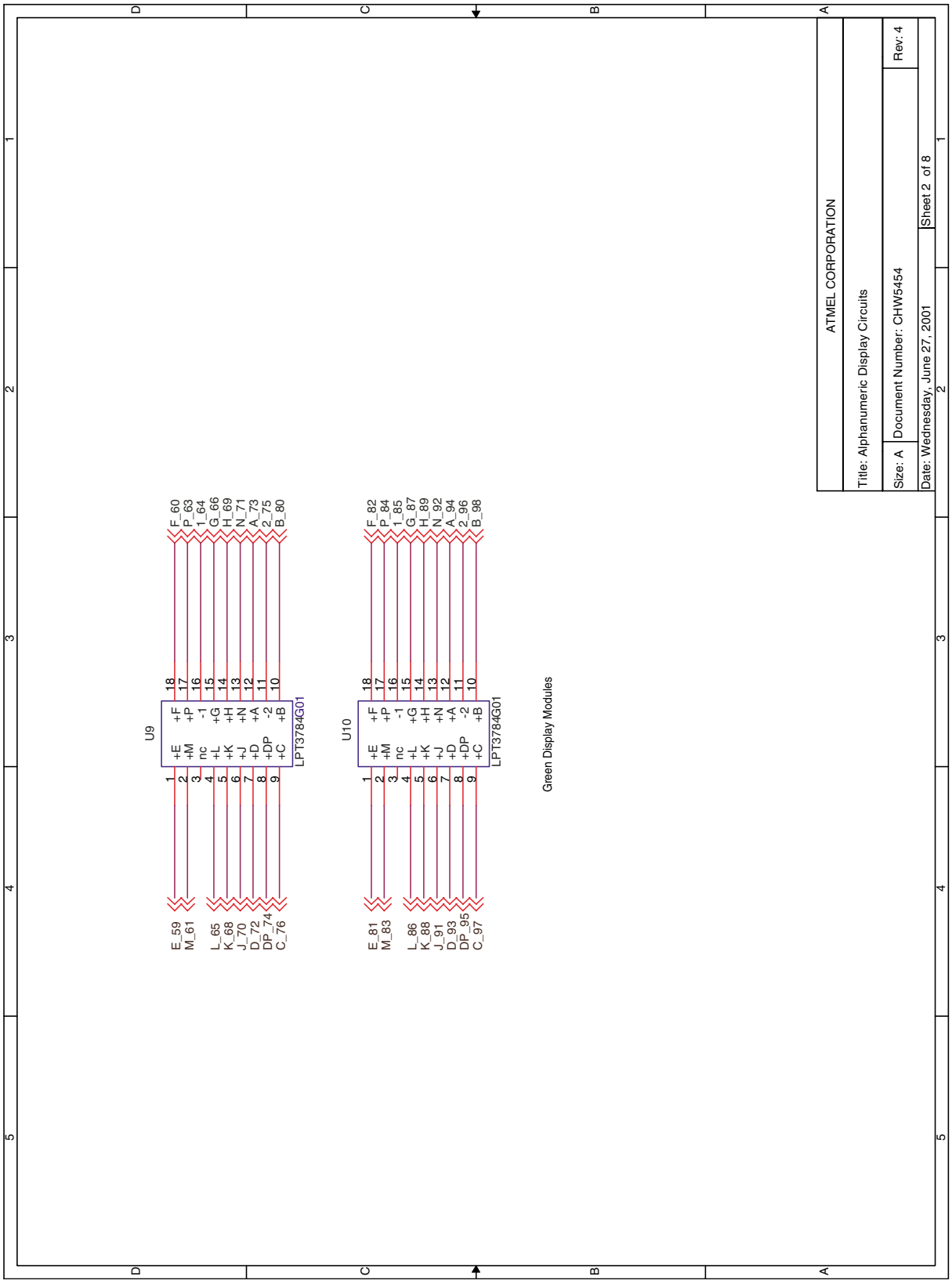
- ATSTK94 Starter Kit User Guide (Supplied with ATSTK94)
- AT94K Series datasheet, available at http://www.atmel.com/atmel/acrobat/doc1138.pdf.
- AT94K Series Configuration application note, available at http://www.atmel.com/atmel/acrobat/doc2313.pdf.
- AT17LV010 datasheet, available at http://www.atmel.com/atmel/acrobat/doc0944.pdf.
- Programming Specification for Atmel's Configuration EEPROMs, available at http://www.atmel.com/atmel/acrobat/doc0437.pdf.
- Additional application notes found on the Atmel web site, at http://www.atmel.com/atmel/products/prod183.htm.

## Board Schematics

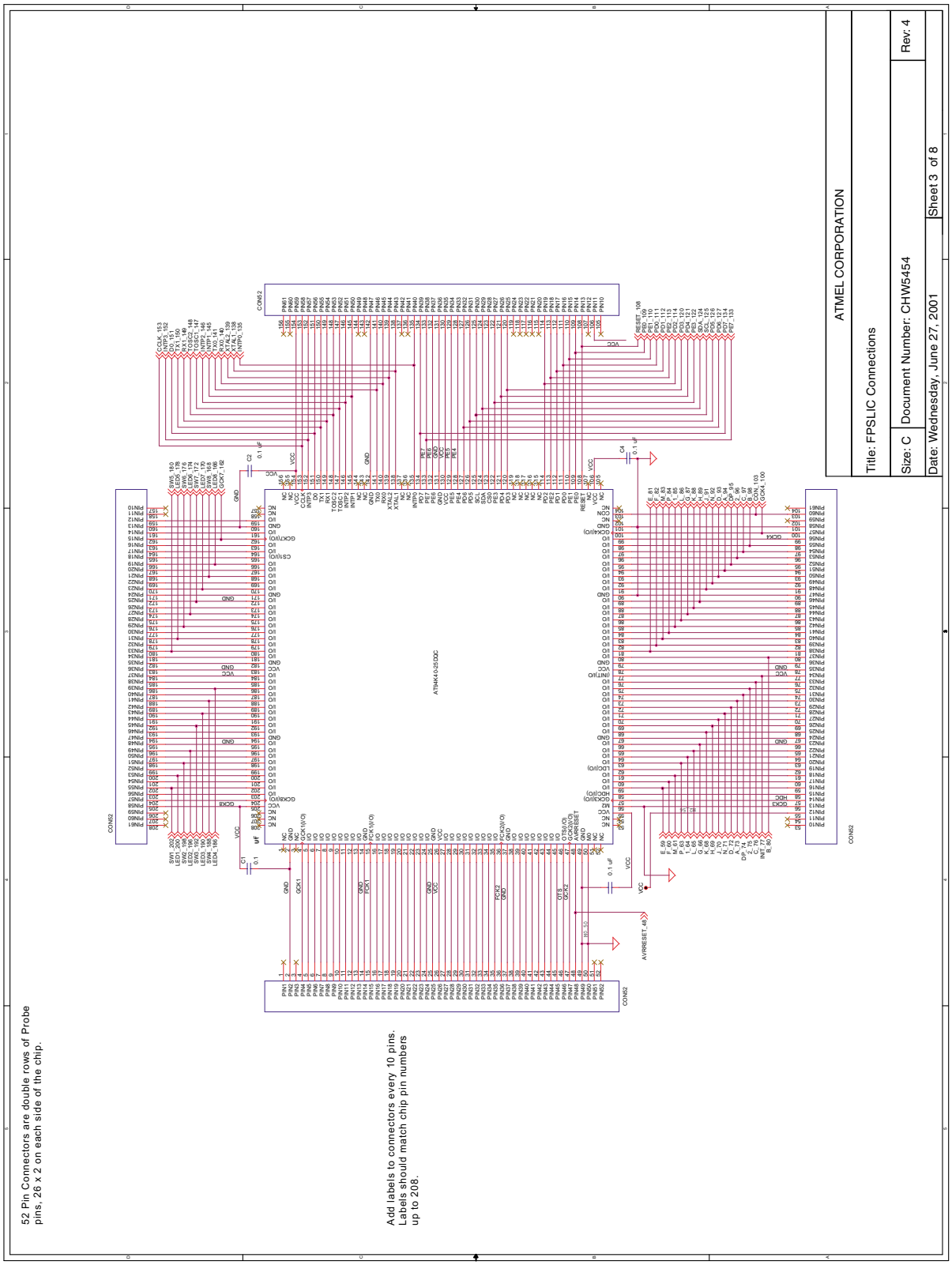
### Clock Circuits



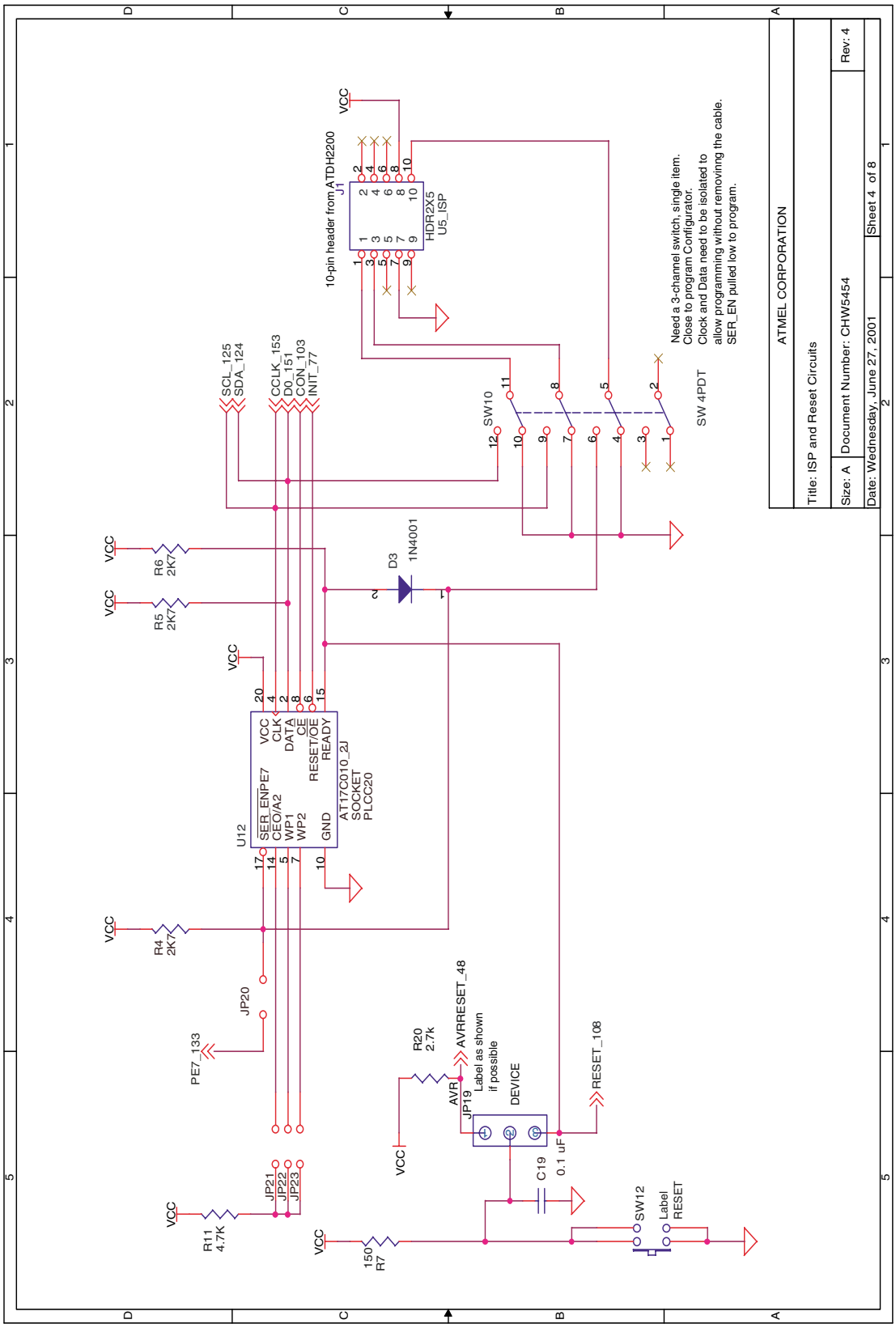
## Alphanumeric Display Circuits



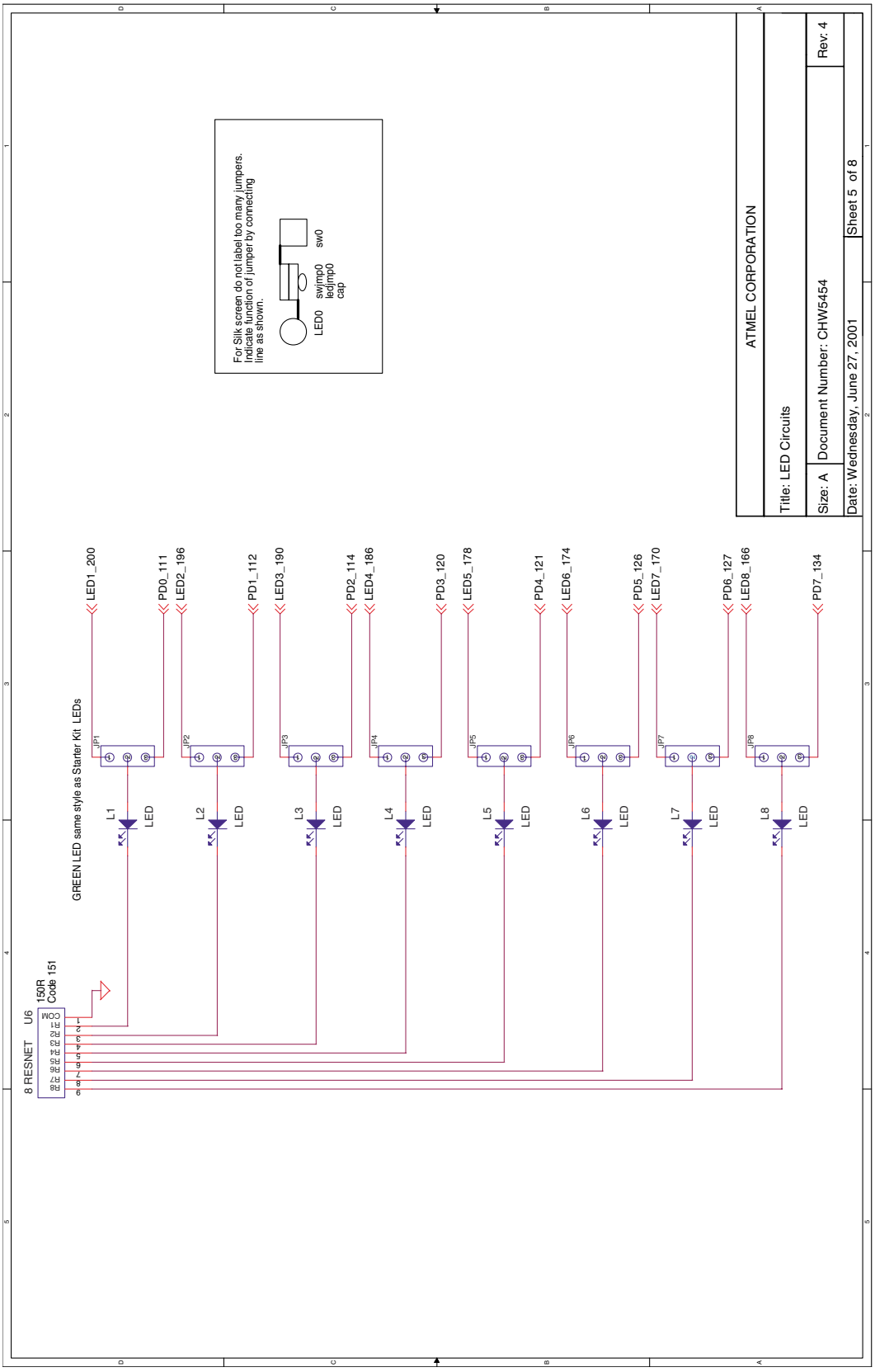
## FPSLIC Connections



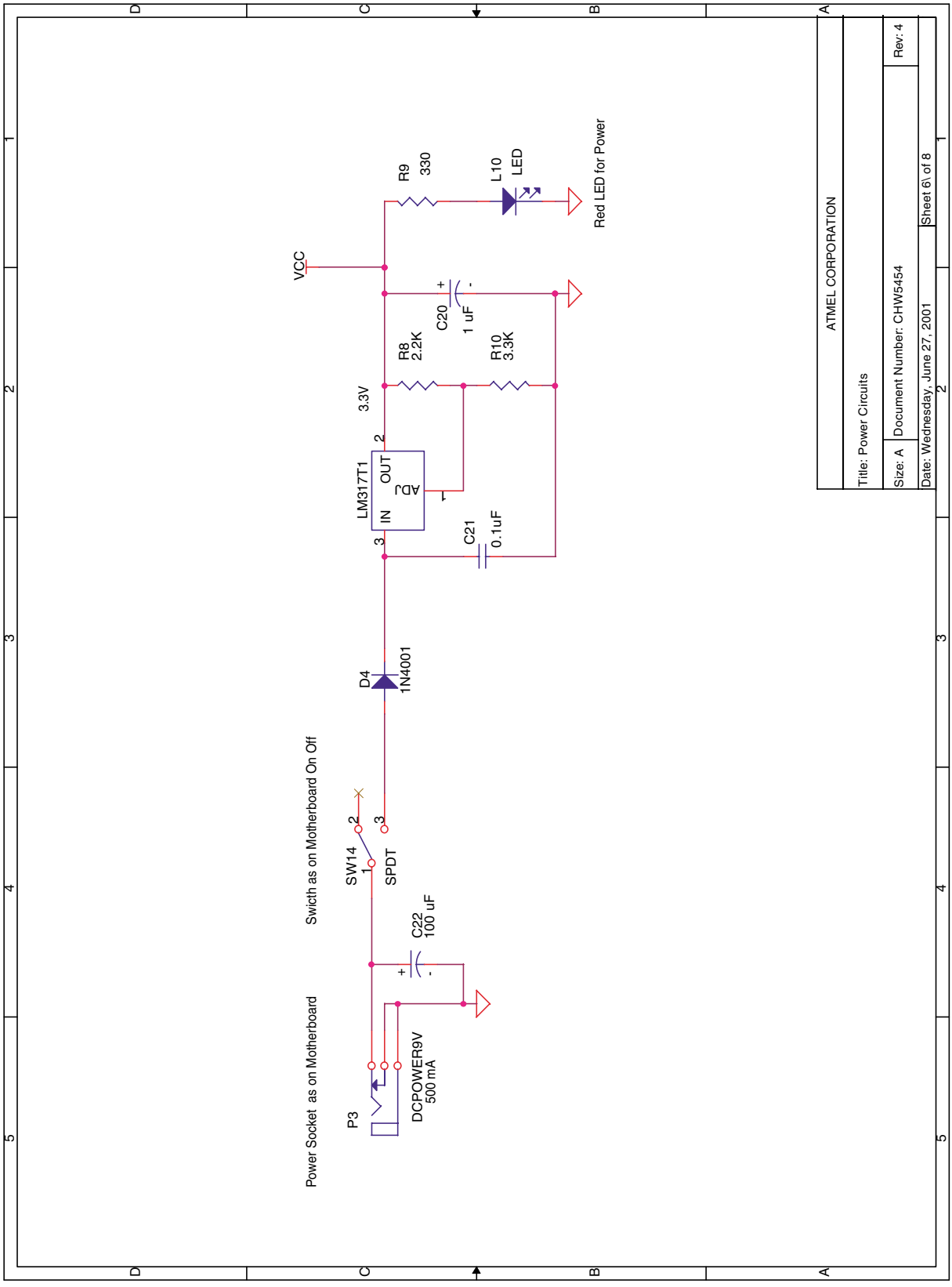
## ISP and Reset Circuits



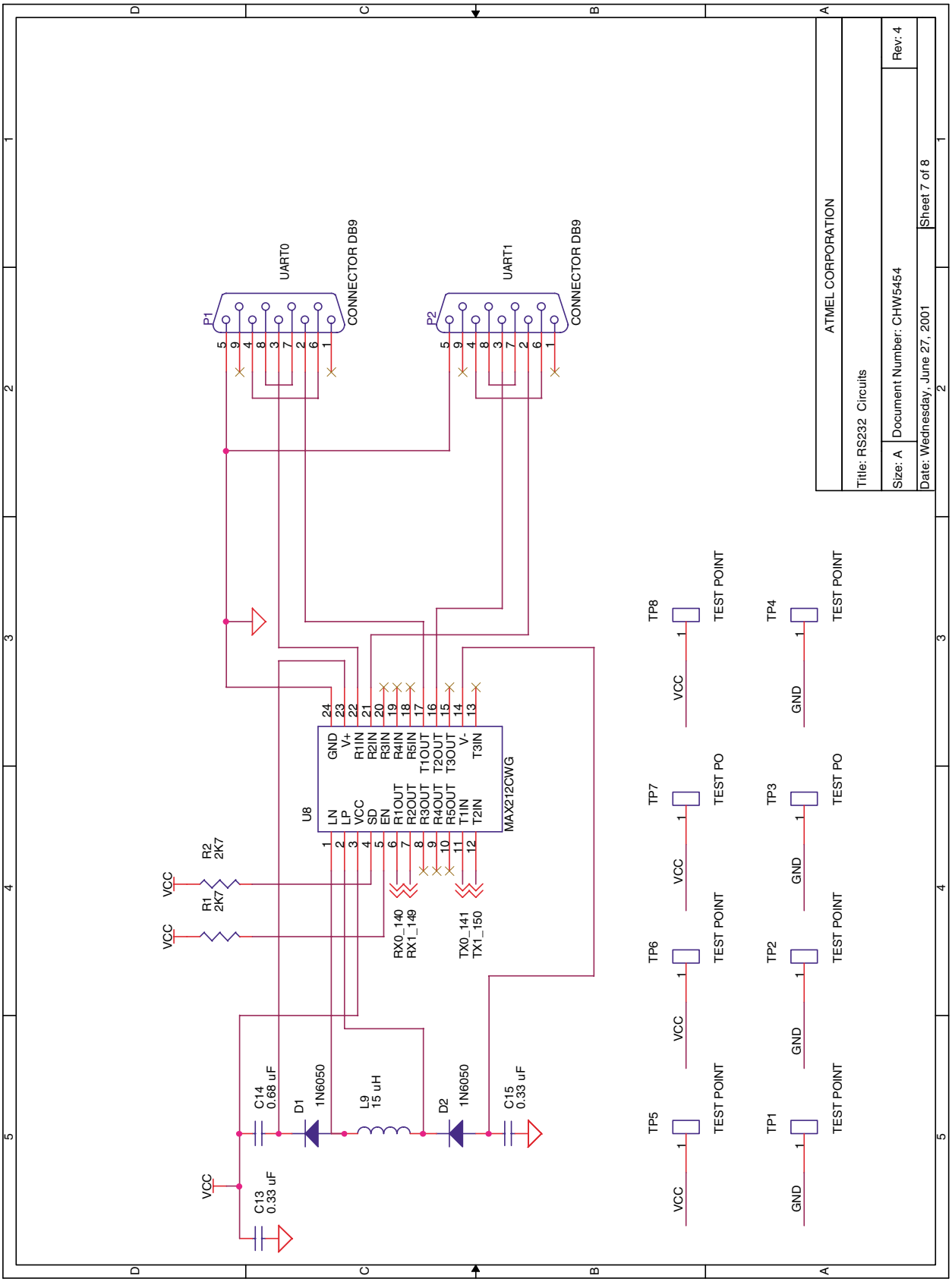
## LED Circuits



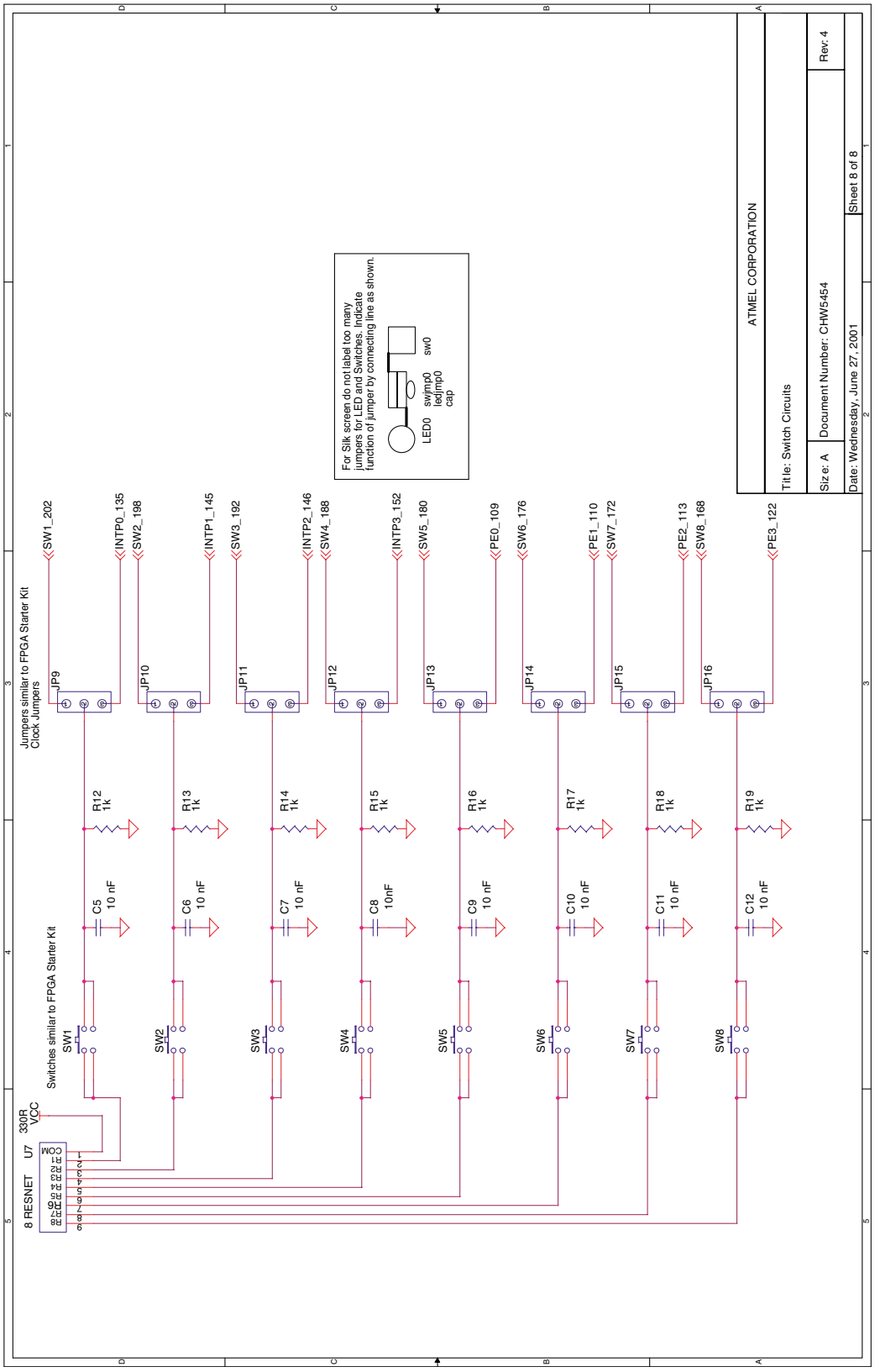
## Power Circuits



## RS232 Circuits



## Switch Circuits



## Device Pinout and Board Connection Summary

Table 8 shows the pin number for the FPSLIC device, the corresponding function of the FPSLIC pin and then the function as it is laid out on the Starter Kit. Any pin that does not have a board Function assigned may be used as a wire wrap or probe connection into the FPSLIC device.

All probe pins on the board are connected to the corresponding IO of the chip.

Pins that connect to the Switches or LEDs may also be used as user-specific inputs or outputs simply by leaving the corresponding Jumper disconnected.

**Table 8.** Pinout and Board Connection

| Pin | FPSLIC IO Type | Board Function | Hardware |
|---|---|---|---|
| 1 | No Connect | | |
| 2 | GND | GND | |
| 3 | No Connect | | |
| 4 | GCK1(IO) | | |
| 5 | IO | | |
| 6 | IO | | |
| 7 | IO | | |
| 8 | IO | | |
| 9 | IO | | |
| 10 | IO | | |
| 11 | IO | | |
| 12 | IO | | |
| 13 | IO | | |
| 14 | GND | GND | |
| 15 | FCK1(IO) | | |
| 16 | IO | | |
| 17 | IO | | |
| 18 | IO | | |
| 19 | IO | | |
| 20 | IO | | |
| 21 | IO | | |
| 22 | IO | | |
| 23 | IO | | |
| 24 | IO | | |
| 25 | GND | GND | |
| 26 | $V_{CC}$ | $V_{CC}$ | |
| 27 | IO | | |
| 28 | IO | | |
| 29 | IO | | |

**Table 8.** Pinout and Board Connection

| Pin | FPSLIC IO Type | Board Function | Hardware |
|---|---|---|---|
| 30 | IO | | |
| 31 | IO | | |
| 32 | IO | | |
| 33 | IO | | |
| 34 | IO | | |
| 35 | IO | | |
| 36 | FCK2(IO) | | |
| 37 | GND | GND | |
| 38 | IO | | |
| 39 | IO | | |
| 40 | IO | | |
| 41 | IO | | |
| 42 | IO | | |
| 43 | IO | | |
| 44 | IO | | |
| 45 | IO | | |
| 46 | OTS(IO) | | |
| 47 | GCK2(IO) | | |
| 48 | AVRRESET | AVR RESET | JP19, SW12 |
| 49 | GND | GND | |
| 50 | M0 | GND | |
| 51 | No Connect | | |
| 52 | No Connect | | |
| 53 | No Connect | | |
| 54 | No Connect | | |
| 55 | $V_{CC}$ | | |
| 56 | M2 | GND | |
| 57 | GCK3(IO) | | |
| 58 | HDC(IO) | | |
| 59 | IO | ALPHANUMERIC 1 E | LED1 E |
| 60 | IO | ALPHANUMERIC 1 F | LED1 F |
| 61 | IO | ALPHANUMERIC 1 M | LED1 M |
| 62 | LDC(IO) | | |
| 63 | IO | ALPHANUMERIC 1 P | LED1 P |
| 64 | IO | ALPHANUMERIC 1 Cathode 1 | LED1 Cathode 1 |

**Table 8.** Pinout and Board Connection

| Pin | FPSLIC IO Type | Board Function | Hardware |
|---|---|---|---|
| 65 | IO | ALPHANUMERIC 1 L | LED1 L |
| 66 | IO | ALPHANUMERIC 1 G | LED1 G |
| 67 | GND | GND | |
| 68 | IO | ALPHANUMERIC 1 K | LED1 K |
| 69 | IO | ALPHANUMERIC 1 H | LED1 H |
| 70 | IO | ALPHANUMERIC 1 J | LED1 J |
| 71 | IO | ALPHANUMERIC 1 N | LED1 N |
| 72 | IO | ALPHANUMERIC 1 D | LED1 D |
| 73 | IO | ALPHANUMERIC 1 A | LED1 A |
| 74 | IO | ALPHANUMERIC 1 DP | LED1 DP |
| 75 | IO | ALPHANUMERIC 1 Cathode 2 | LED1 Cathode 2 |
| 76 | IO | ALPHANUMERIC 1 C | LED1 C |
| 77 | INIT(IO) | INIT | AT17 RESET/OE |
| 78 | $V_{CC}$ | $V_{CC}$ | |
| 79 | GND | GND | |
| 80 | IO | ALPHANUMERIC 1 B | LED1 B |
| 81 | IO | ALPHANUMERIC 0 E | LED0 E |
| 82 | IO | ALPHANUMERIC 0 F | LED0 F |
| 83 | IO | ALPHANUMERIC 0 M | LED0 M |
| 84 | IO | ALPHANUMERIC 0 P | LED0 P |
| 85 | IO | ALPHANUMERIC 0 Cathode 1 | LED0 Cathode 1 |
| 86 | IO | ALPHANUMERIC 0 L | LED0 L |
| 87 | IO | ALPHANUMERIC 0 G | LED0 G |
| 88 | IO | ALPHANUMERIC 0 K | LED0 K |
| 89 | IO | ALPHANUMERIC 0 H | LED0 H |
| 90 | GND | GND | |
| 91 | IO | ALPHANUMERIC 0 J | LED0 J |
| 92 | IO | ALPHANUMERIC 0 N | LED0 N |
| 93 | IO | ALPHANUMERIC 0 D | LED0 D |
| 94 | IO | ALPHANUMERIC 0 A | LED0 A |
| 95 | IO | ALPHANUMERIC 0 DP | LED0 DP |
| 96 | IO | ALPHANUMERIC 0 Cathode 2 | LED0 Cathode 2 |
| 97 | IO | ALPHANUMERIC 0 C | LED0 C |
| 98 | IO | ALPHANUMERIC 0 B | LED0 B |

**Table 8.** Pinout and Board Connection

| Pin | FPSLIC IO Type | Board Function | Hardware |
|---|---|---|---|
| 99 | IO | | |
| 100 | GCK4 (IO) | GCK4 – 4 MHz Clock | 4 MHz Oscillator |
| 101 | GND | GND | |
| 102 | No Connect | | |
| 103 | CON | Configuration Control | AT17 /CE |
| 104 | No Connect | | |
| 105 | No Connect | | |
| 106 | $V_{CC}$ | $V_{CC}$ | |
| 107 | No Connect | | |
| 108 | RESET | FPSLIC Device RESET | JP19, SW12 |
| 109 | PE0 | PortE 0 | JP13 A |
| 110 | PE1 | PortE 1 | JP14 A |
| 111 | PD0 | PortD 0 | JP1 A |
| 112 | PD1 | PortD 1 | JP2 A |
| 113 | PE2 | PortE 2 | JP15 A |
| 114 | PD2 | PortD 2 | JP3 A |
| 115 | No Connect | | |
| 116 | No Connect | | |
| 117 | No Connect | | |
| 118 | No Connect | | |
| 119 | No Connect | | |
| 120 | PD3 | PortD 3 | JP4 A |
| 121 | PD4 | PortD 4 | JP5 A |
| 122 | PE3 | PortE 3 | JP16 A |
| 123 | CS0 | | |
| 124 | SDA | 2 Wire Serial Data | AT17 Data |
| 125 | SCL | 2 Wire Serial Clock | AT17 Clock |
| 126 | PD5 | PortD 5 | JP6 A |
| 127 | PD6 | PortD 6 | JP7 A |
| 128 | PE4 | PortE 4 | |
| 129 | PE5 | PortE 5 | |
| 130 | $V_{CC}$ | $V_{CC}$ | |
| 131 | GND | GND | |
| 132 | PE6 | PortE 6 | |
| 133 | PE7 | PortE 7 | |
| 134 | PD7 | PortD 7 | JP8 A |

**Table 8.** Pinout and Board Connection

| Pin | FPSLIC IO Type | Board Function | Hardware |
|---|---|---|---|
| 135 | INTP0 | External Interrupt 0 | JP9 A |
| 136 | No Connect | | |
| 137 | No Connect | | |
| 138 | XTAL1 | AVR System Clock Input | JP17, Y1 |
| 139 | XTAL2 | AVR System Clock Pair | JP18, Y1 |
| 140 | RX0 | UART 0 Receive | UART 0 pin3 |
| 141 | TX0 | UART 0 Transmit | UART 0 pin 2 |
| 142 | GND | GND | |
| 143 | No Connect | | |
| 144 | No Connect | | |
| 145 | INTP1 | External Interrupt 1 | JP10 A |
| 146 | INTP2 | External Interrupt 2 | JP11 A |
| 147 | TOSC1 | Oscillator Input | Y2 |
| 148 | TOSC2 | Oscillator Pair | Y2 |
| 149 | RX1 | UART 1 Receive | UART 1 pin 2 |
| 150 | TX1 | UART 1 Transmit | UART 1 pin 3 |
| 151 | D0 | Configuration Data Input | AT17 Data |
| 152 | INTP3 | External Interrupt 3 | JP12 A |
| 153 | CCLK | Configuration Clock | AT17 Clock |
| 154 | $V_{CC}$ | | |
| 155 | No Connect | | |
| 156 | No Connect | | |
| 157 | No Connect | | |
| 158 | No Connect | | |
| 159 | IO | | |
| 160 | GND | | |
| 161 | IO0 | | |
| 162 | GCK7(IO) | GCK7 Manual Clock | MAN CLK (SW) |
| 163 | IO | | |
| 164 | IO | | |
| 165 | IO | | |
| 166 | IO | LED 8 | JP8 F |
| 167 | IO | | |
| 168 | IO | Switch 8 | JP16 F |
| 169 | IO | | |

**Table 8.** Pinout and Board Connection

| Pin | FPSLIC IO Type | Board Function | Hardware |
|---|---|---|---|
| 170 | IO | LED 7 | JP7 F |
| 171 | GND | | |
| 172 | IO | Switch 7 | JP15 F |
| 173 | IO | | |
| 174 | IO | LED 6 | JP6 F |
| 175 | IO | | |
| 176 | IO | Switch 6 | JP14 F |
| 177 | IO | | |
| 178 | IO | LED 5 | JP5 F |
| 179 | IO | | |
| 180 | IO | Switch 5 | JP13 F |
| 181 | IO | | |
| 182 | GND | | |
| 183 | $V_{CC}$ | | |
| 184 | IO | | |
| 185 | IO | | |
| 186 | IO | LED 4 | JP4 F |
| 187 | IO | | |
| 188 | IO | Switch 4 | JP12 F |
| 189 | IO | | |
| 190 | IO | LED 3 | JP3 F |
| 191 | IO | | |
| 192 | IO | Switch 3 | JP11 F |
| 193 | IO | | |
| 194 | GND | | |
| 195 | IO | | |
| 196 | IO | LED 2 | JP2 F |
| 197 | IO | | |
| 198 | IO | Switch 2 | JP10 F |
| 199 | IO | | |
| 200 | IO | LED 1 | JP1 F |
| 201 | IO | | |
| 202 | IO | Switch 1 | JP9 F |
| 203 | IO | | |
| 204 | GCK8(IO) | | |
| 205 | $V_{CC}$ | | |

**Table 8.** Pinout and Board Connection

| Pin | FPSLIC IO Type | Board Function | Hardware |
|---|---|---|---|
| 206 | No Connect | | |
| 207 | No Connect | | |
| 208 | No Connect | | |

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