16-BIT, ULTRA-LOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Relative Accuracy: 8 LSB (Max)**
- **Glitch Energy: 0.1 nV-s**
- **Settling Time: 10 μs to ±0.003% FSR**
- **Power Supply: +2.7 V to +5.5 V**
- **16-Bit Monotonic Over Temperature**
- ***Micro*Power Operation: 200 μA at 5 V**
- **Rail-to-Rail Output Amplifier**
- **Power-On Reset to Midscale**
- **Power-Down Capability**
- **Schmitt-Triggered Digital Inputs**
- **$\overline{\text{SYNC}}$ Interrupt Facility**
- **2's Complement Input and Reset to Midscale**
- **Operating Temperature Range: -40°C to 105°C**
- **Available Packages:**
  - **3 mm × 5 mm MSOP-8**

APPLICATIONS

- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo-Control**
- **PC Peripherals**
- **Portable Instrumentation**
- **Programmable Attenuation**

DESCRIPTION

The DAC8550 is a small, low-power, voltage output, 16-bit digital-to-analog converter (DAC). It is monotonic, provides good linearity, and minimizes undesired code to code transient voltages. The DAC8550 uses a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

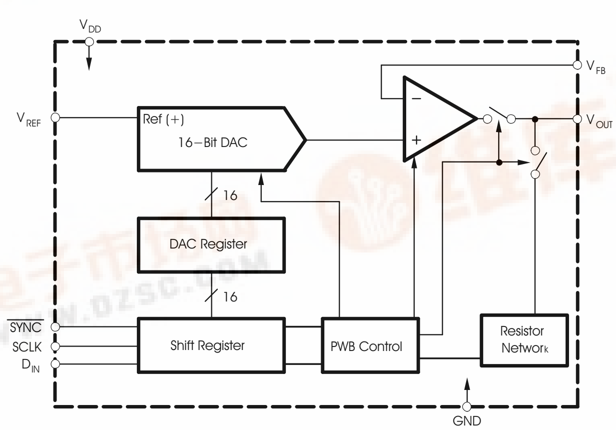
The DAC8550 requires an external reference voltage to set its output range. The DAC8550 incorporates a power-on reset circuit that ensures that the DAC output powers up at midscale and remain there until a valid write takes place to the device. The DAC8550 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 200 nA at 5 V.

The low-power consumption of this device in normal operation makes it ideal for portable battery-operated equipment. Power consumption is 1 mW at 5 V, reducing to 1 μW in power-down mode.

The DAC8550 is available in a MSOP-8 package.

Also see the DAC8551 binary coded counterpart of the DAC8550.

FUNCTIONAL BLOCK DIAGRAM



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SPI, QSPI are trademarks of Motorola.
Microwire is a trademark of National Semiconductor.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE LEAD	PACKAGE DESIGNATOR(1)	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8550	±12	±1	MSOP-8	DGK	–40°C TO 105°C	D80	DAC8550IDGKT	Tape and Reel, 250
							DAC8550IDGKR	Tape and Reel, 2500
DAC8550B	±8	±1	MSOP-8	DGK	–40°C TO 105°C	D80	DAC8550IBDGKT	Tape and Reel, 250
							DAC8550IBDGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	UNIT
Supply voltage, V_{DD} to GND	–0.3 V to 6 V
Digital input voltage range, V_I to GND	–0.3 V to $+V_{DD}$ + 0.3 V
Output voltage, V_{OUT} to GND	–0.3 V to $+V_{DD}$ + 0.3 V
Operating free-air temperature range, T_A	–40°C to 105°C
Storage temperature range, T_{STG}	–65°C to 150°C
Junction temperature range, $T_{J(max)}$	150°C
Power dissipation (DGK package)	$(T_J max – T_A)/\theta_{JA}$
Thermal impedance, θ_{JA}	206°C/W
Thermal impedance, θ_{JC}	44°C/W

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V,– 40°C to 105°C range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)							
	Resolution			16			Bits
E_L	Relative accuracy	Measured by line passing through codes -32283 and 32063	DAC8550		±5	±12	LSB
			DAC8550B		±3	±8	LSB
E_D	Differential nonlinearity	16-bit Monotonic			±0.25	±1	LSB
E_O	Zero-code error	Measured by line passing through codes -32283 and 32063.			±2	±12	mV
E_{FS}	Full-scale error				±0.05	±0.5	% of FSR
E_G	Gain error				±0.02	±0.2	% of FSR
	Zero-code error drift				±5		µV/°C
	Gain temperature coefficient				±1		ppm of FSR/°C
PSRR	Power supply rejection ratio	R_L = 2 kΩ, C_L = 200 pF			0.75		mV/V
OUTPUT CHARACTERISTICS(2)							
V_O	Output voltage range			0		V_{REF}	V

(1) Linearity calculated using a reduced code range of -32283 to 32063; output unloaded.
(2) Specified by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

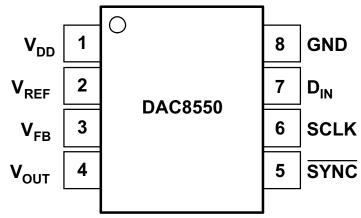
V_{DD} = 2.7 V to 5.5 V,– 40°C to 105°C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{sd}	Output voltage settling time	To ±0.003% FSR, 1200_H to $8D00_H$, R_L = 2 kΩ, 0 pF < C_L < 200 pF		8	10	µs
		R_L = 2 kΩ, C_L = 500 pF		12		µs
SR	Slew rate			1.8		V/µs
	Capacitive load stability	R_L = ∞		470		pF
		R_L = 2 kΩ		1000		pF
	Code change glitch impulse	1 LSB change around major carry		0.1		nV-s
	Digital feedthrough	SCLK toggling, FSYNC high		0.1		nV-s
z_o	DC output impedance	At mid-code input		1		Ω
I_{OS}	Short-circuit current	V_{DD} = 5 V		50		mA
		V_{DD} = 3 V		20		mA
t_{on}	Power-up time	Coming out of power-down mode V_{DD} = 5 V		2.5		µs
		Coming out of power-down mode V_{DD} = 3 V		5		µs
AC PERFORMANCE						
SNR	Signal-to-noise ratio (1st 19 harmonics removed)	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		95		dB
THD	Total harmonic distortion	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		85		dB
SFDR	Spurious-free dynamic range	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		87		dB
SINAD	Signal-to-noise and distortion	BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz		84		dB
REFERENCE INPUT						
V_{ref}	Reference voltage		0		V_{DD}	V
$I_{I(ref)}$	Reference current input range	V_{REF} = V_{DD} = 5 V		50	75	µA
		V_{REF} = V_{DD} = 3.6 V		30	45	µA
$z_{I(ref)}$	Reference input impedance			125		kΩ
LOGIC INPUTS (3)						
Input current				±1		µA
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.6	V
V_{IH}	High-level input voltage	V_{DD} = 5 V	2.4			V
		V_{DD} = 3 V	2.1			V
	Pin capacitance				3	pF
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
I_{DD} (normal mode)		Input code equals mid-scale, reference current included, no load				
	V_{DD} = 3.6 V to 5.5 V	V_{IH} = V_{DD} and V_{IL} = GND		200	250	µA
	V_{DD} = 2.7 V to 3.6 V	V_{IH} = V_{DD} and V_{IL} = GND		180	240	µA
I_{DD} (all power-down modes)		V_{IH} = V_{DD} and V_{IL} = GND				
	V_{DD} = 3.6 V to 5.5 V	V_{IH} = V_{DD} and V_{IL} = GND		0.2	2	µA
	V_{DD} = 2.7 V to 3.6 V	V_{IH} = V_{DD} and V_{IL} = GND		0.05	2	µA
POWER EFFICIENCY						
I_{OUT}/I_{DD}		I_{LOAD} = 2 mA, V_{DD} = 5 V		89%		
TEMPERATURE RANGE						
Specified performance			–40		105	°C

(3) Specified by design and characterization, not production tested.

PIN CONFIGURATION

MSOP-8
(Top View)



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Power supply input, 2.7 V to 5.5 V.
2	V_{REF}	Reference voltage input.
3	V_{FB}	Feedback connection for the output amplifier.
4	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{SYNC}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock (unless $\overline{SYNC}$ is taken HIGH before this edge in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC8550).
6	SCLK	Serial clock input. Data can be transferred at rates up to 30 MHz.
7	D_{IN}	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input.
8	GND	Ground reference point for all circuitry on the part.

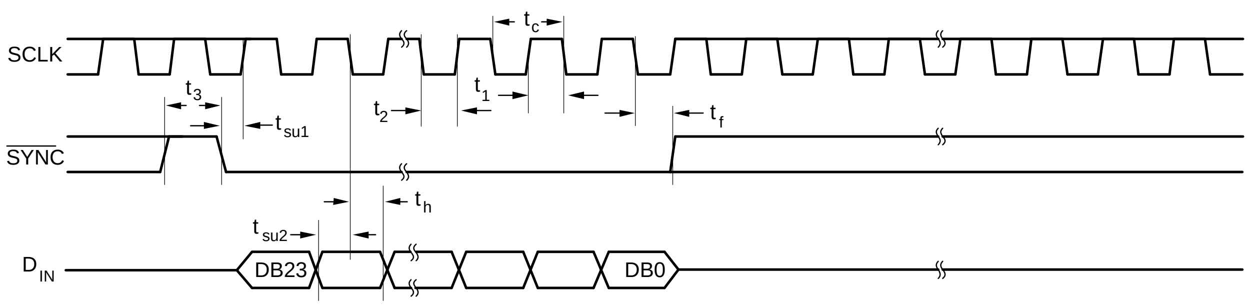
TIMING REQUIREMENTS(1)(2)

V_{DD} = 2.7 V to 5.5 V, all specifications –40°C to 105°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c(3)	SCLK cycle time	V_{DD} = 2.7 V to 3.6 V	20			ns
		V_{DD} = 3.6 V to 5.5 V	20			
t_1	SCLK HIGH time	V_{DD} = 2.7 V to 3.6 V	13			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_2	SCLK LOW time	V_{DD} = 2.7 V to 3.6 V	22.5			ns
		V_{DD} = 3.6 V to 5.5 V	13			
t_{su1}	$\overline{SYNC}$ to SCLK rising edge setup time	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_{su2}	Data setup time	V_{DD} = 2.7 V to 3.6 V	5			ns
		V_{DD} = 3.6 V to 5.5 V	5			
t_h	Data hold time	V_{DD} = 2.7 V to 3.6 V	4.5			ns
		V_{DD} = 3.6 V to 5.5 V	4.5			
t_f	SCLK falling edge to $\overline{SYNC}$ rising edge	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_3	Minimum $\overline{SYNC}$ HIGH time	V_{DD} = 2.7 V to 3.6 V	50			ns
		V_{DD} = 3.6 V to 5.5 V	33			

(1) All input signals are specified with $t_R = t_F$ = 3 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See *Serial Write Operation* timing diagram.
(3) Maximum SCLK frequency is 30 MHz at V_{DD} = 3.6 V to 5.5 V and 20 MHz at V_{DD} = 2.7 V to 3.6 V.

SERIAL WRITE OPERATION



TYPICAL CHARACTERISTICS: V_{DD} = 5 V

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (-40°C)

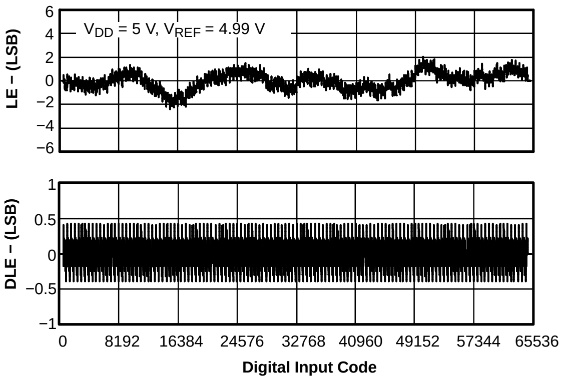


Figure 1.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (25°C)

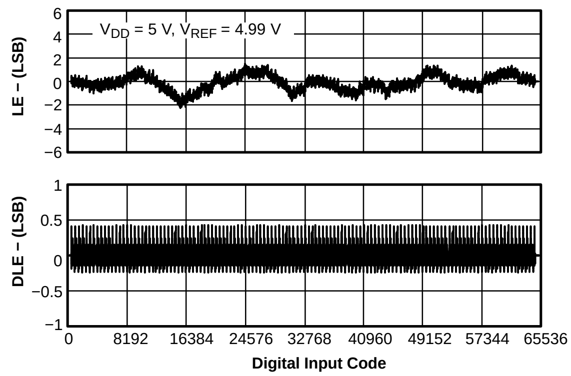


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (105°C)

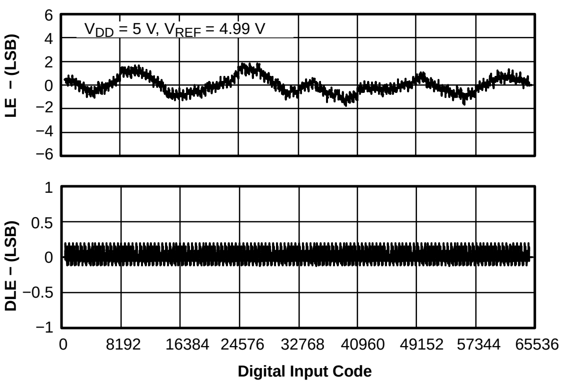


Figure 3.

ZERO-SCALE ERROR vs TEMPERATURE

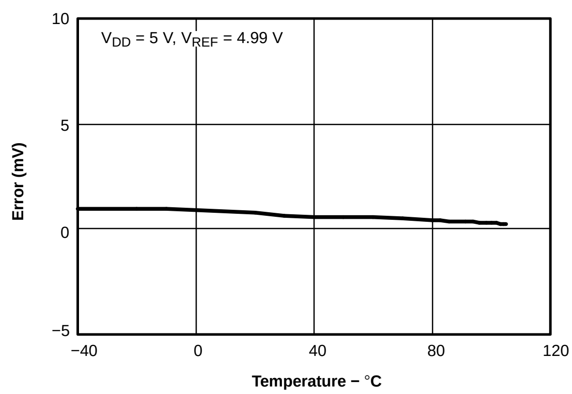


Figure 4.

FULL-SCALE ERROR vs TEMPERATURE

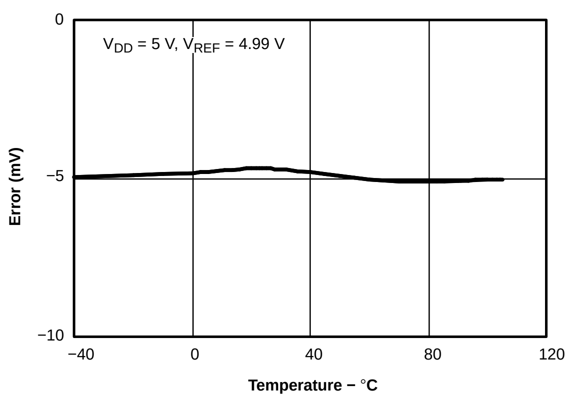


Figure 5.

I_{DD} HISTOGRAM

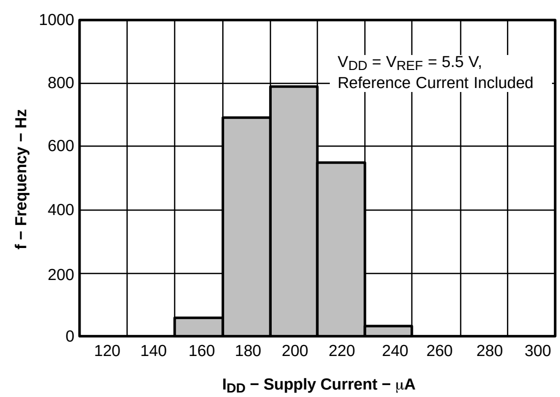


Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

SOURCE AND SINK CURRENT CAPABILITY

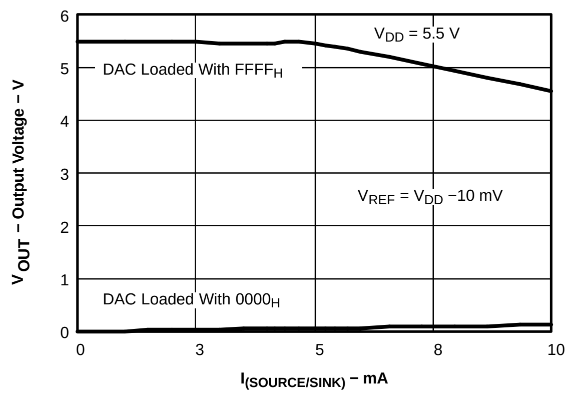


Figure 7.

SUPPLY CURRENT vs DIGITAL INPUT CODE

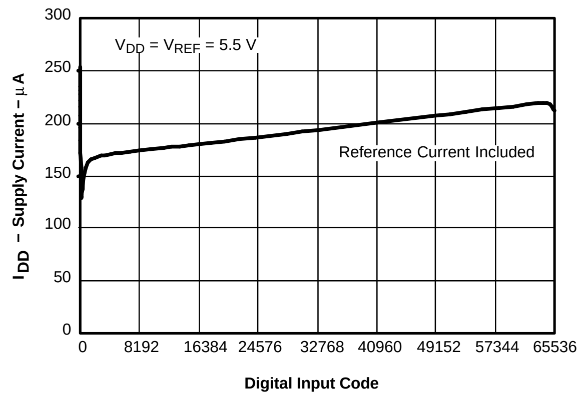


Figure 8.

POWER-SUPPLY CURRENT vs TEMPERATURE

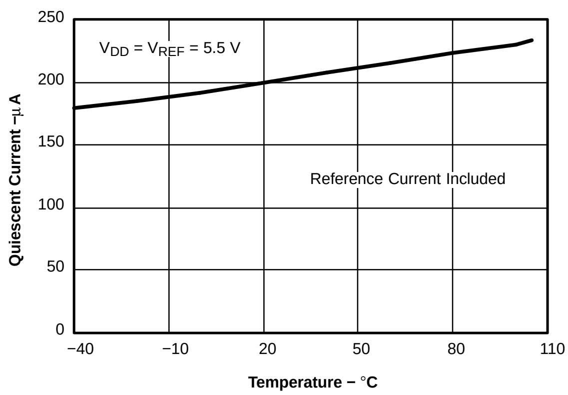


Figure 9.

SUPPLY CURRENT vs SUPPLY VOLTAGE

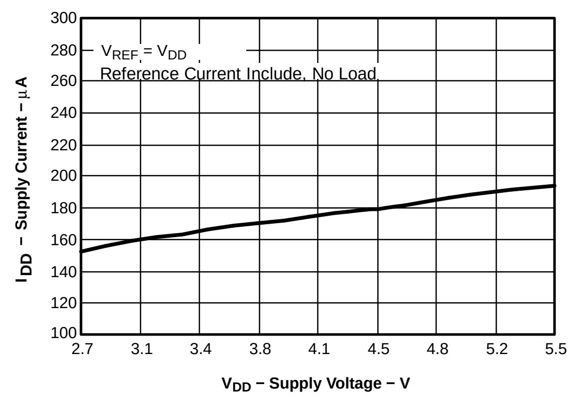


Figure 10.

POWER-DOWN CURRENT vs SUPPLY VOLTAGE

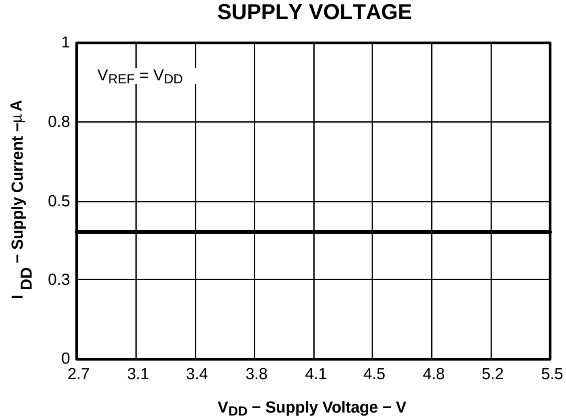


Figure 11.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

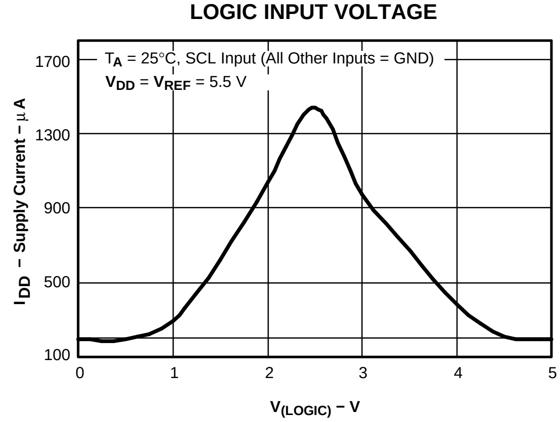


Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

FULL-SCALE SETTLING TIME: 5-V RISING EDGE

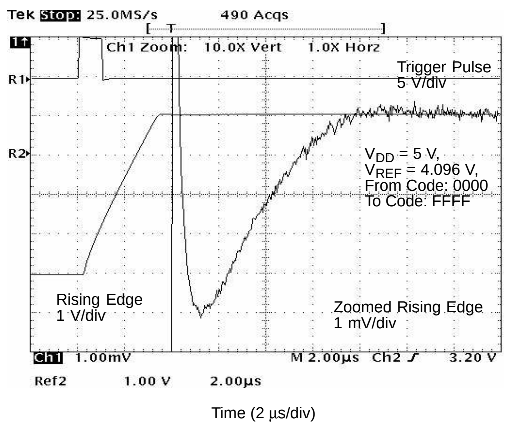


Figure 13.

FULL-SCALE SETTLING TIME: 5-V FALLING EDGE

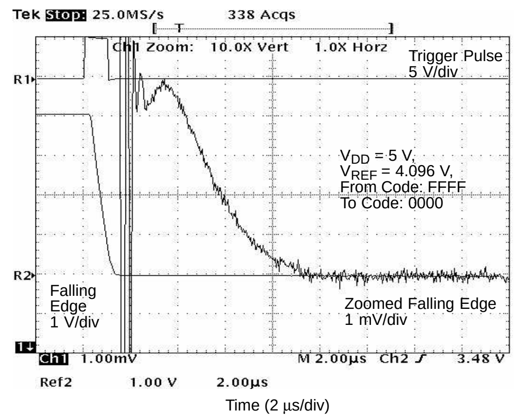


Figure 14.

HALF-SCALE SETTLING TIME: 5-V RISING EDGE

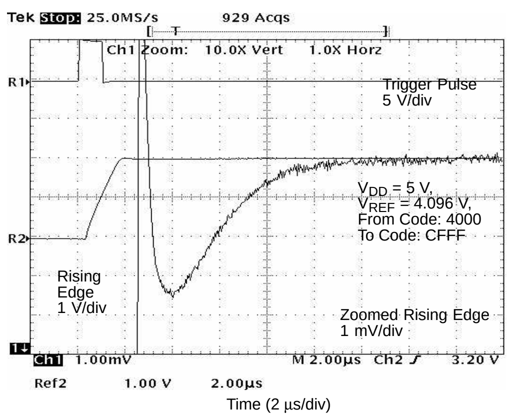


Figure 15.

HALF-SCALE SETTLING TIME: 5-V FALLING EDGE

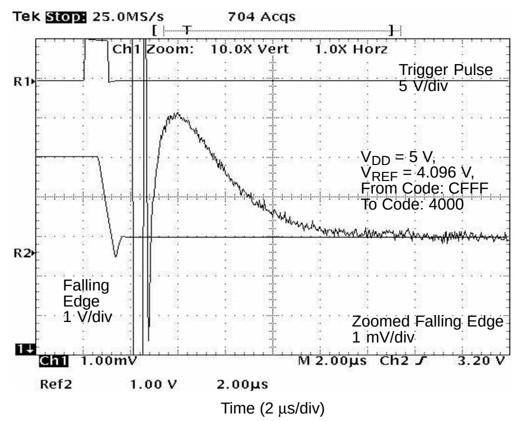


Figure 16.

GLITCH ENERGY: 5-V, 1-LSB STEP, RISING EDGE

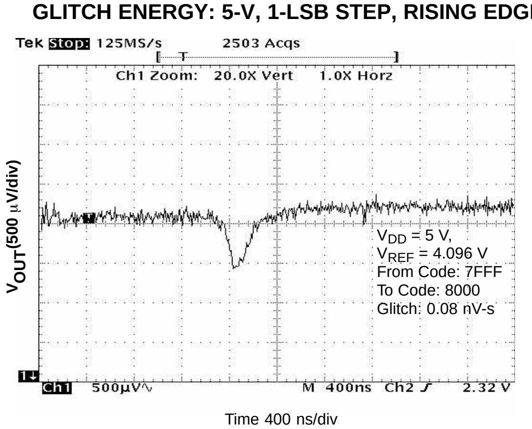


Figure 17.

GLITCH ENERGY: 5-V, 1-LSB STEP, FALLING EDGE

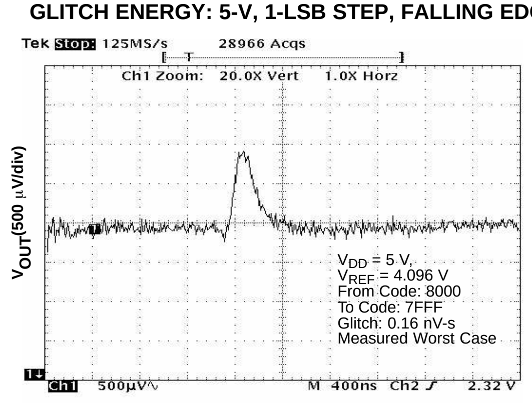


Figure 18.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

GLITCH ENERGY: 5-V, 16-LSB STEP, RISING EDGE

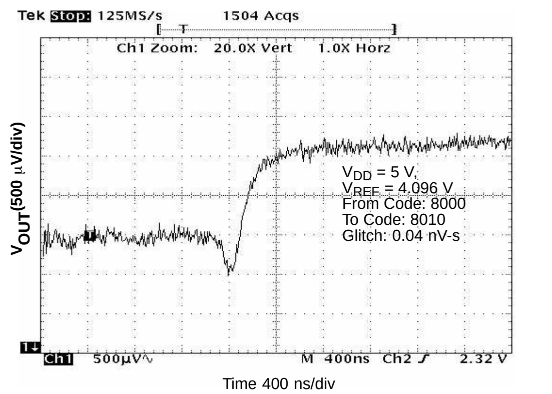


Figure 19.

GLITCH ENERGY: 5-V, 16-LSB STEP, FALLING EDGE

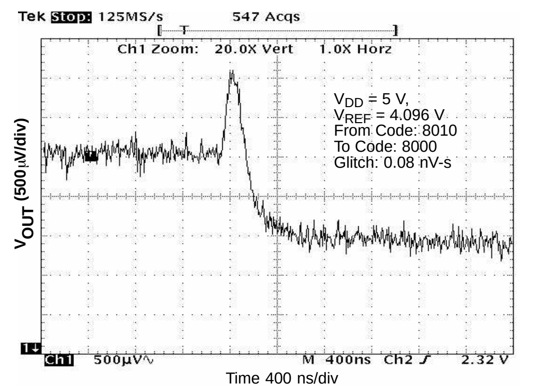


Figure 20.

GLITCH ENERGY: 5-V, 256-LSB STEP, RISING EDGE

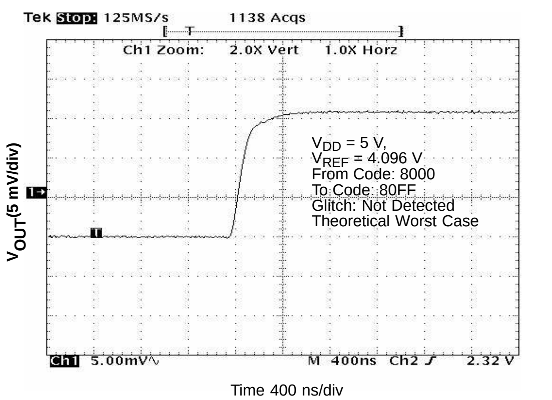


Figure 21.

GLITCH ENERGY: 5-V, 256-LSB STEP, FALLING EDGE

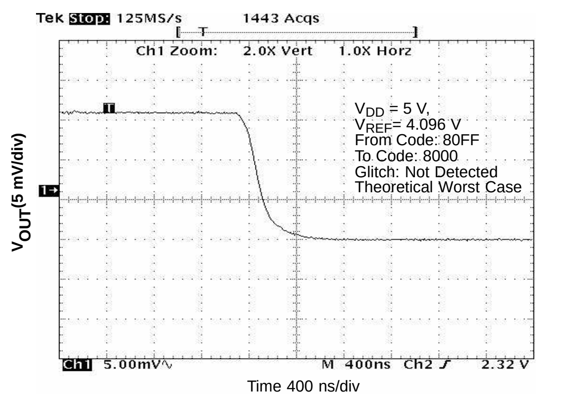


Figure 22.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

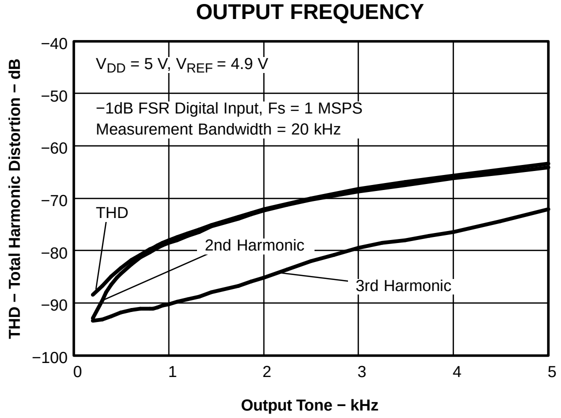


Figure 23.

SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

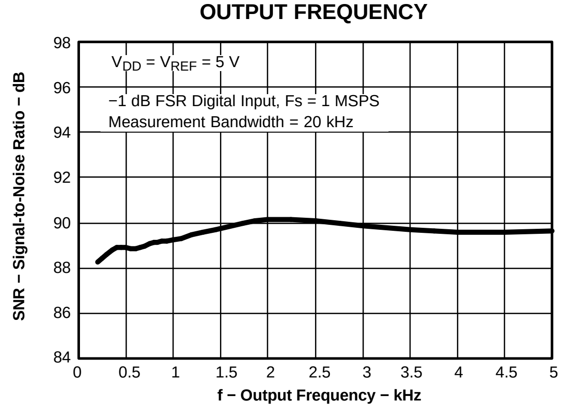


Figure 24.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

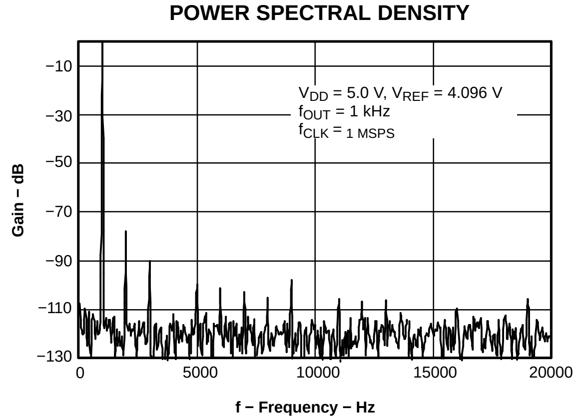


Figure 25.

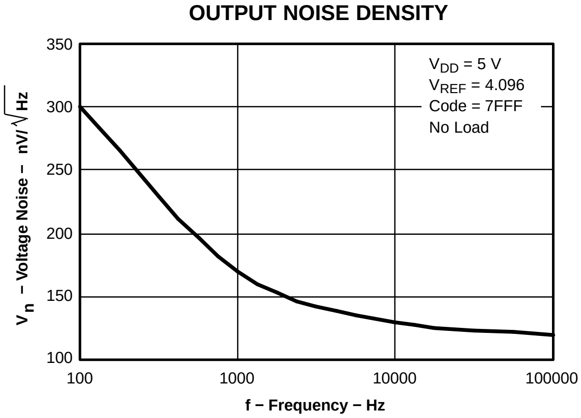


Figure 26.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (-40°C)

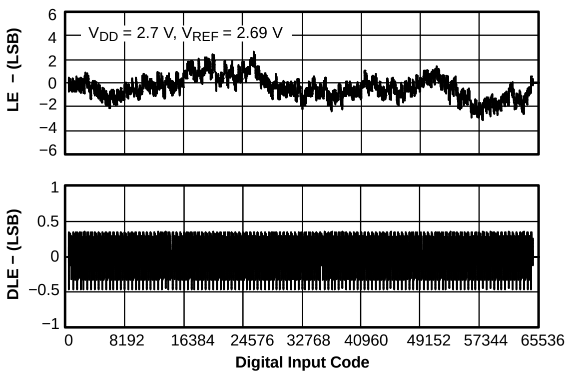


Figure 27.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (25°C)

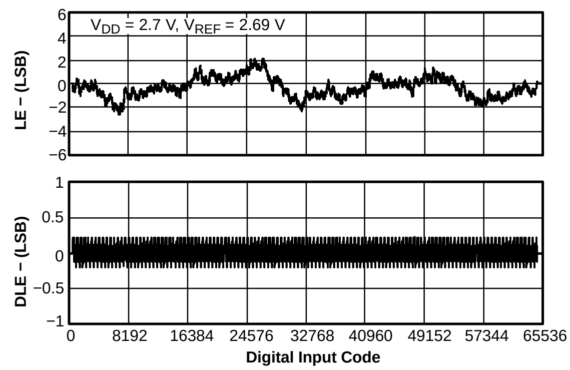


Figure 28.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (105°C)

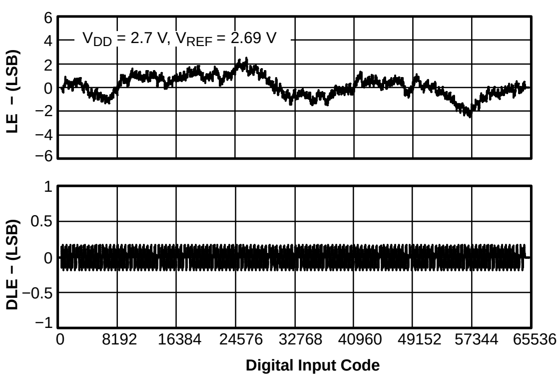


Figure 29.

ZERO-SCALE ERROR vs TEMPERATURE

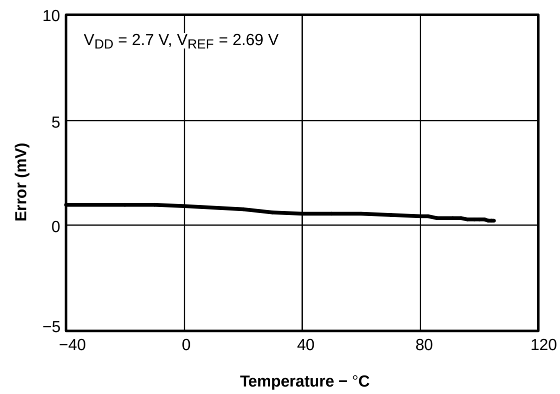


Figure 30.

FULL-SCALE ERROR vs TEMPERATURE

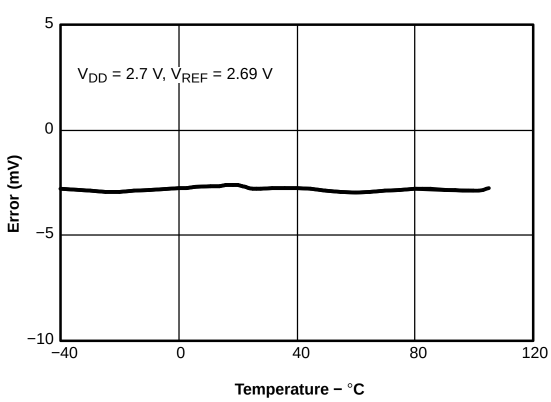


Figure 31.

I_{DD} HISTOGRAM

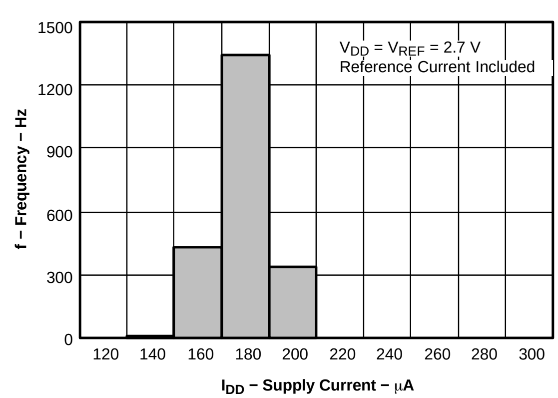


Figure 32.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V (continued)

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

SOURCE AND SINK CURRENT CAPABILITY

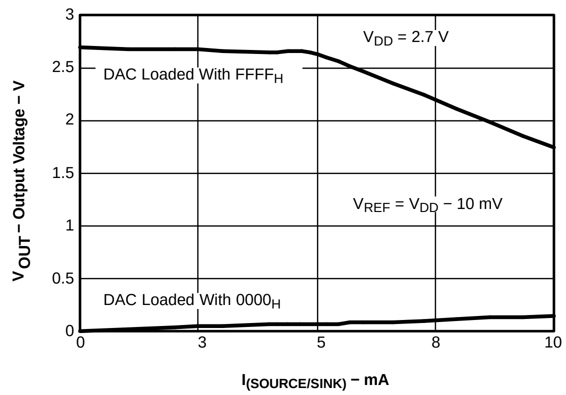


Figure 33.

SUPPLY CURRENT vs DIGITAL INPUT CODE

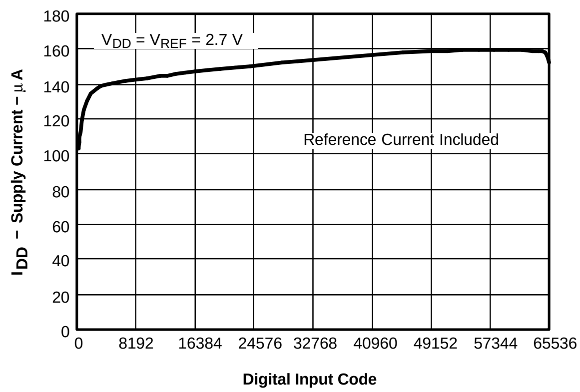


Figure 34.

POWER-SUPPLY CURRENT vs TEMPERATURE

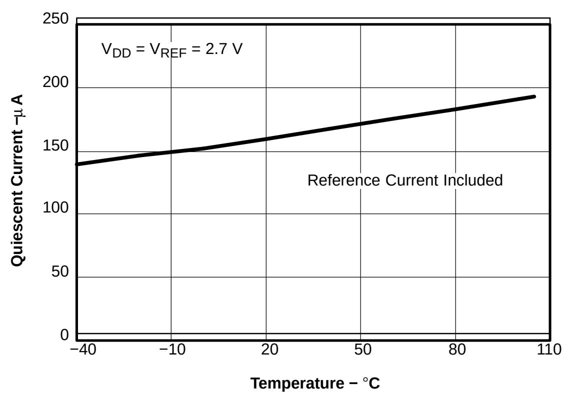


Figure 35.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

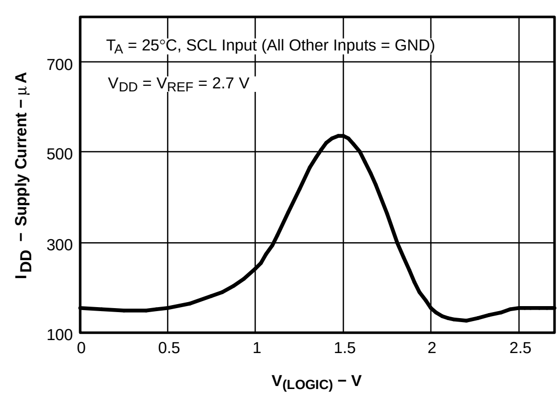


Figure 36.

FULL-SCALE SETTLING TIME: 2.7-V RISING EDGE

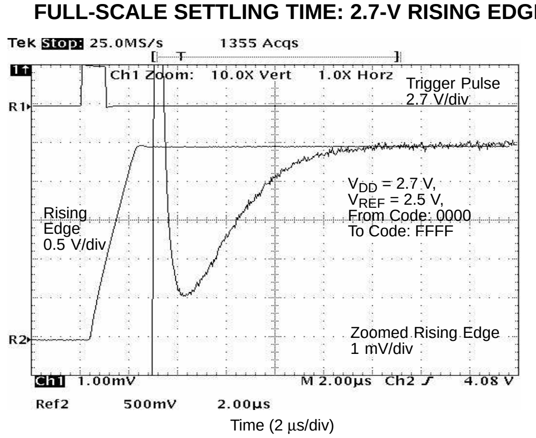


Figure 37.

FULL-SCALE SETTLING TIME: 2.7-V FALLING EDGE

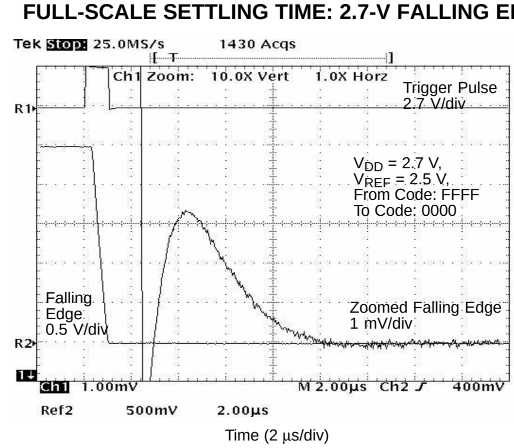


Figure 38.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V (continued)

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

HALF-SCALE SETTLING TIME: 2.7-V RISING EDGE

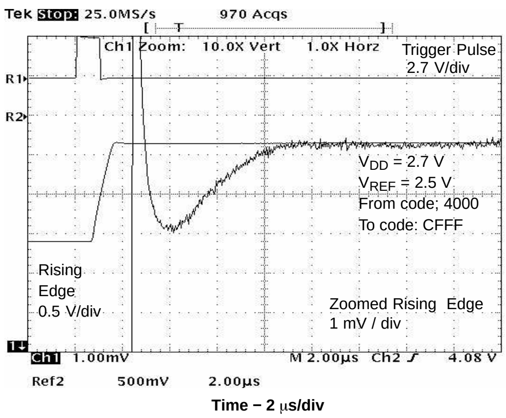


Figure 39.

HALF-SCALE SETTLING TIME: 2.7-V FALLING EDGE

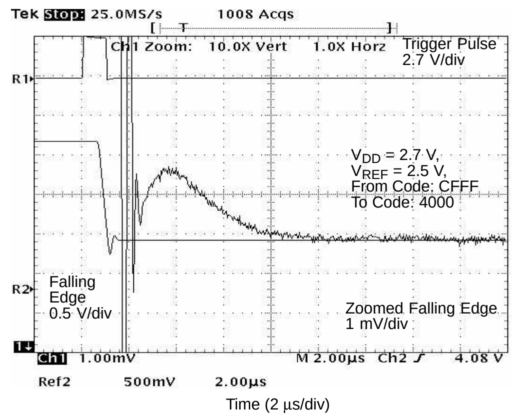


Figure 40.

GLITCH ENERGY: 2.7-V, 1-LSB STEP, RISING EDGE

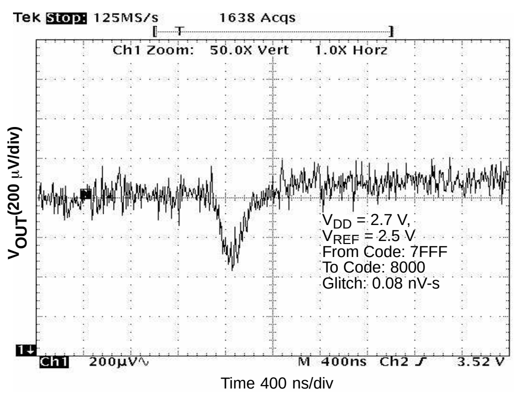


Figure 41.

GLITCH ENERGY: 2.7-V, 1-LSB STEP, FALLING EDGE

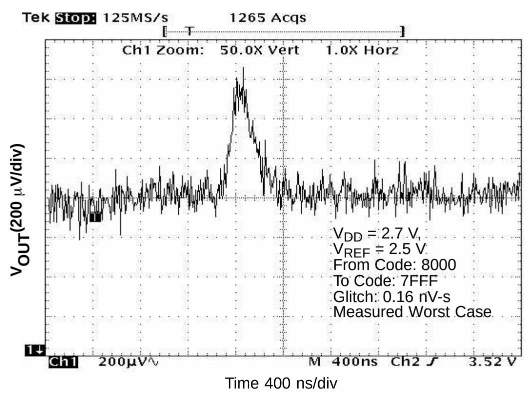


Figure 42.

GLITCH ENERGY: 2.7-V, 16-LSB STEP, RISING EDGE

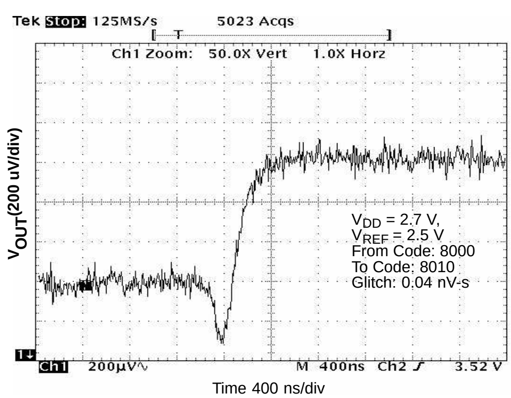


Figure 43.

GLITCH ENERGY: 2.7-V, 16-LSB STEP, FALLING EDGE

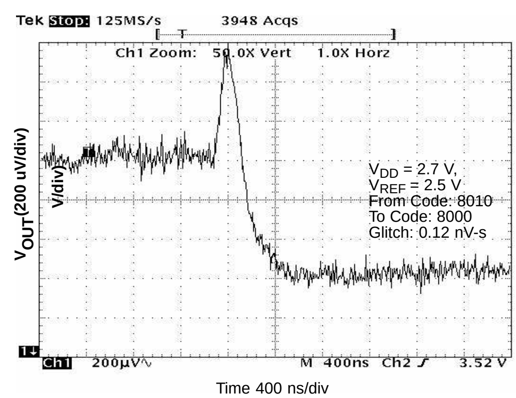


Figure 44.

TYPICAL CHARACTERISTICS: V_{DD} = 2.7 V (continued)

At T_A = 25°C, unless otherwise noted. Unsigned binary equivalent inputs are shown in all figures.

GLITCH ENERGY: 2.7-V, 256-LSB STEP, RISING EDGE

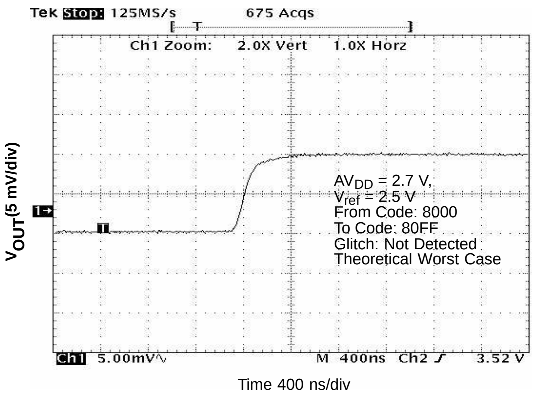


Figure 45.

GLITCH ENERGY: 2.7-V, 256-LSB STEP, FALLING EDGE

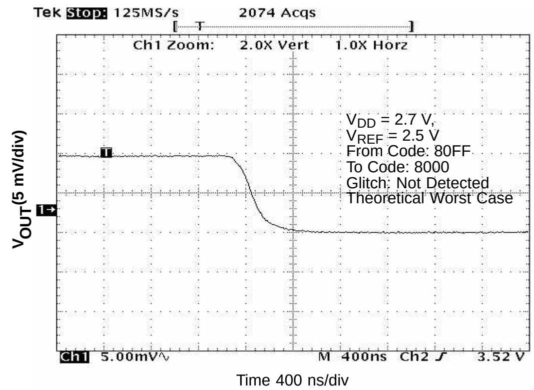


Figure 46.

THEORY OF OPERATION

DAC SECTION

The architecture consists of a string DAC followed by an output buffer amplifier. Figure 47 shows the block diagram of the DAC architecture.

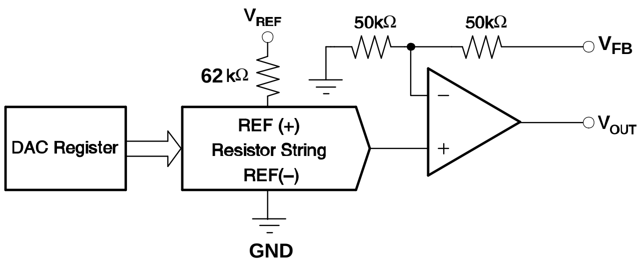


Figure 47. DAC8550 Architecture

The input coding to the DAC8550 is 2's complement, so the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{REF}}{2} + \frac{V_{REF} \times D}{65536} \quad (1)$$

where D = decimal equivalent of the 2's complement code that is loaded to the DAC register; D ranges from -32768 to +32767 where D = 0 is centered at $V_{REF}/2$.

RESISTOR STRING

The resistor string section is shown in Figure 48. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Monotonicity is ensured due to the string resistor architecture.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail output voltages with a range of 0 V to V_{DD}. It is capable of driving a load of 2 Ωk in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slewrate is 1.8 V/µs with a full-scale setting time of 8 µs with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin. This allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

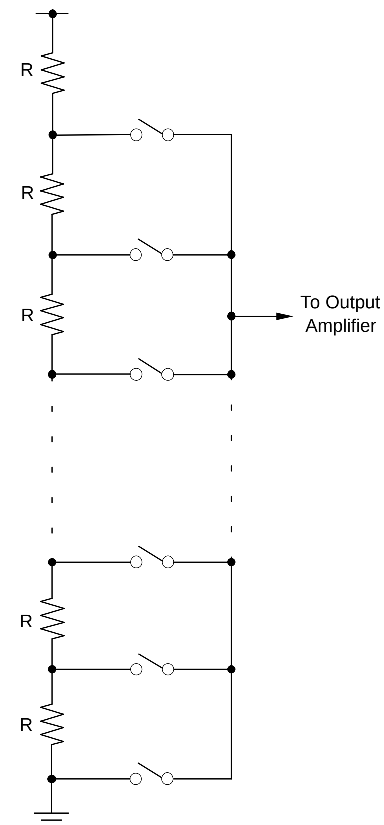


Figure 48. Resistor String

SERIAL INTERFACE

The DAC8550 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI™, QSPI™, and Microwire™ interface standards, as well as most DSP interfaces. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the DAC8550 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is excuted (i.e., a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Since the $\overline{SYNC}$ buffer draws more current when the $\overline{SYNC}$ signal is HIGH than it does when it is LOW, $\overline{\text{SYNC}}$ should be idled LOW between write sequences for lowest power operation of the part. As mentioned above, it must be brought HIGH again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide, as shown in Figure 49. The first six bits are *don't care* bits. The next two bits (PD1 andPD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). For a more complete description of the various modes see the *Power-Down Modes* section. The next 16 bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if $\overline{\text{SYNC}}$ is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 50.

POWER-ON RESET

The DAC8550 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the output voltages are set to midscale; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

DB23 ... DB0

X	X	X	X	X	X	PD1	PD0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 49. DAC8550 Data Input Register Format

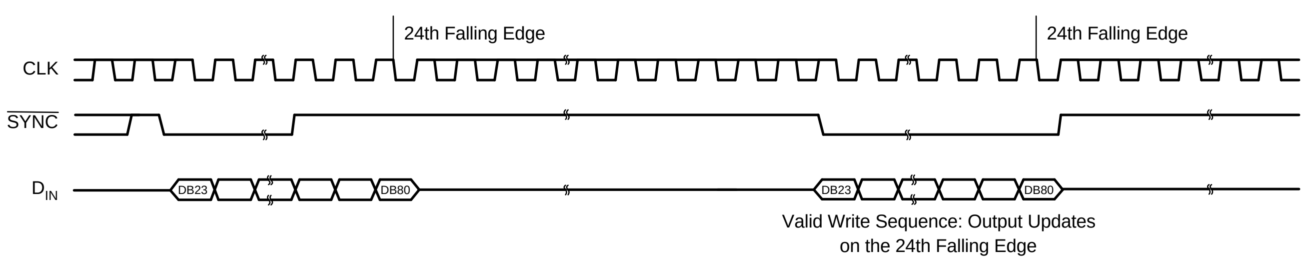


Figure 50. $\overline{\text{SYNC}}$ Interrupt Facility

POWER-DOWN MODES

The DAC8550 supports four seperate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in control register. Table 1 shows how the state of the bits corresponds to the mode of operation of the device.

Table 1. Modes of Operation for the DAC8550

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal operation
--	--	Power-down modes
0	1	Output typically 1 kΩ to GND
1	0	Output typically 100 kΩ to GND
1	1	High-Z

When both bits are set to 0, the device works normally with a typical current consumption of 200 µA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. The advantage with this is that the output impedance of the device is known while in power-down mode. There are three different options. The output is connected internally to GND through a 1-kΩ resistor, a 100-kΩ resistor, or it is left open-circuited (High-Z). The output stage is illustrated in Figure 51.

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V, and 5 µs for V_{DD} = 3 V. See the *Typical Characteristics* for more information.

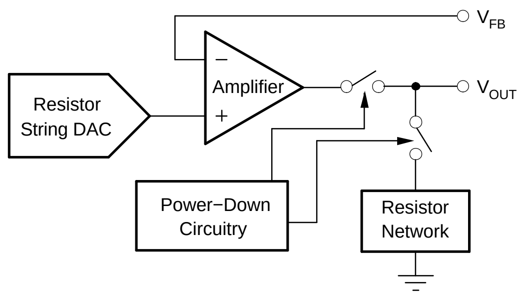
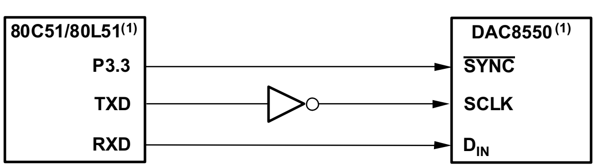


Figure 51. Output Stage During Power-Down

MICROPROCESSOR INTERFACING

DAC8550 TO 8051 Interface

See Figure 52 for a serial interface between the DAC8550 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8550, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8550, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which has the LSB first. The DAC8550 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.

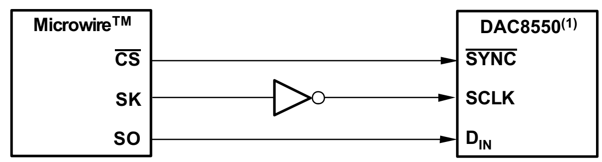


NOTE: (1) Additional pins omitted for clarity.

Figure 52. DAC8550 to 80C51/80L51 Interface

DAC8550 to Microwire Interface

Figure 53 shows an interface between the DAC8550 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8550 on the rising edge of the SK signal.

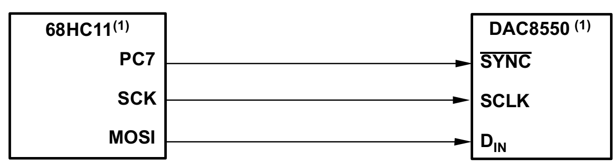


NOTE: (1) Additional pins omitted for clarity.

Figure 53. DAC8550 to Microwire Interface

DAC8550 to 68HC11 Interface

Figure 54 shows a serial interface between the DAC8550 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8550, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7), similar to the 8051 diagram.



NOTE: (1) Additional pins omitted for clarity.

Figure 54. DAC8550 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is 0 and its CPHA bit is 1. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data is being transmitted to the DAC, the SYNC line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8550, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.

APPLICATION INFORMATION

USING THE REF02 AS A POWER SUPPLY FOR THE DAC8550

Due to the extremely low supply current required by the DAC8550, an alternative option is to use a REF02 +5 V precision voltage reference to supply the required voltage to the device, as shown in Figure 55.

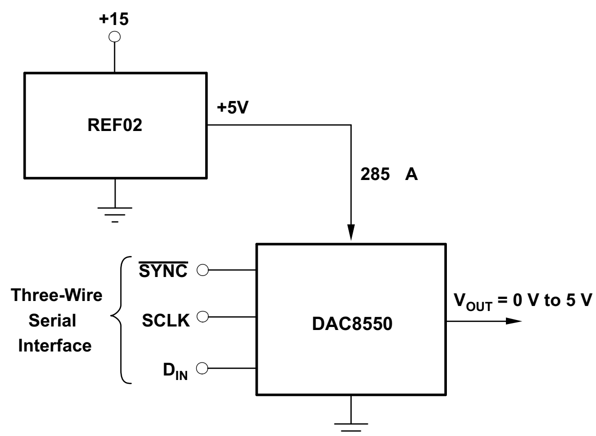


Figure 55. REF02 as a Power Supply to the DAC8550

This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 outputs a steady supply voltage for the DAC8550. If the REF02 is used, the current it needs to supply to the DAC8550 is 250 μA. This is with no load on the output of the DAC. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5 kΩ load on the DAC output) is:

$$200\ \mu A \times \frac{5\ V}{5\ k\Omega} + 1.2\ mA \tag{2}$$

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 299 μV for the 1.2 mA current drawn from it. This corresponds to a 8.9 LSB error.

BIPOLAR OPERATION USING THE DAC8550

The DAC8550 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 56. The circuit shown gives an output voltage range of $\pm V_{REF}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O \left[\left(\frac{V_{REF}}{2} + V_{REF} \times \frac{D}{65536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{REF} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in 2's complement (-32768 to +32767).

With V_{REF} = 5 V, R1 = R2 = 10 kΩ.

$$V_O + 10 \times \frac{D}{65536} \tag{4}$$

This is an output voltage range of ±5 V with 8000_H corresponding to a –5 V output and $8FFF_H$ corresponding to a 5 V output. Similarly, using V_{REF} = 2.5 V a ±2.5 V output voltage range can be achieved.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8550 offers single-supply operation and is used often in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed the more difficult it is to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8550 all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to V_{DD} should be well regulated and have low noise. Switching power supplies and DC/DC converters often has high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a 5 V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1 μF to 10 μF capacitor and 0.1 μF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100 μF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors, all designed to essentially low-pass filter the 5 V supply, removing the high-frequency noise.

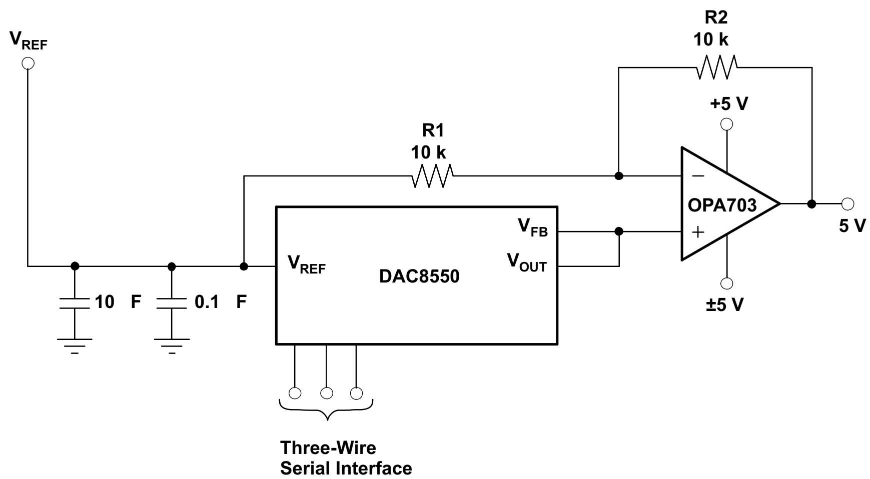


Figure 56. Bipolar Output Range

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8550IBDGKR	ACTIVE	MSOP	DGK	8	2500	TBD	Call TI	Call TI
DAC8550IBDGKT	ACTIVE	MSOP	DGK	8	250	TBD	Call TI	Call TI
DAC8550IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
DAC8550IDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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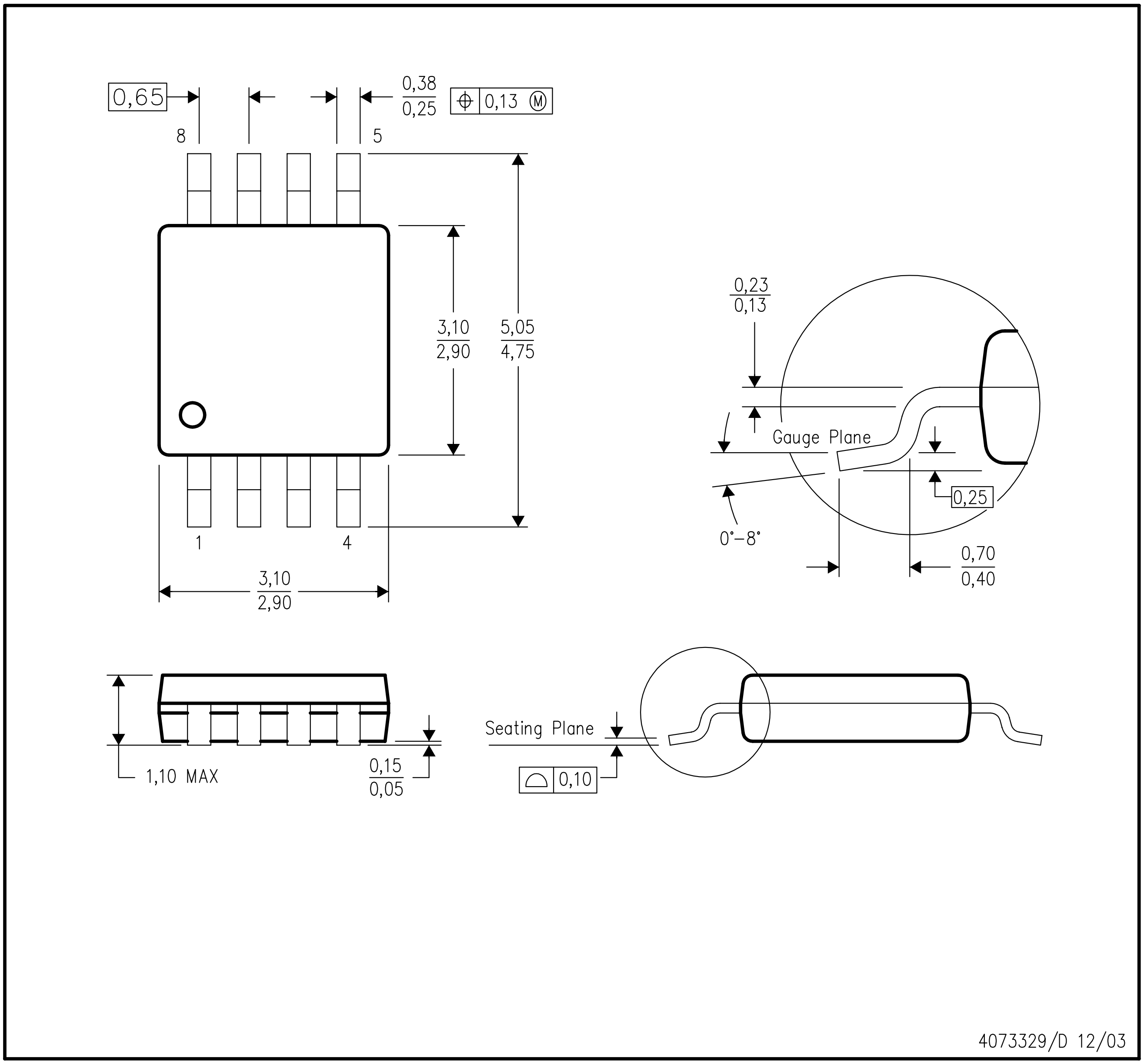
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation AA.