Rev 0; 9/07

Dual-Channel, I²C Adjustable Sink/Source Current DAC

DS4412

General Description

The DS4412 contains two I²C adjustable-current DACs that are each capable of sinking or sourcing current. Each output has 15 sink and 15 source settings that are programmed by I²C interface. The full-scale range and step size of each output is determined by an external resistor that can adjust the output current over a 4:1 range.

The output pins, OUT0 and OUT1, power-up in a high-impedance state.

Applications

Power-Supply Adjustment

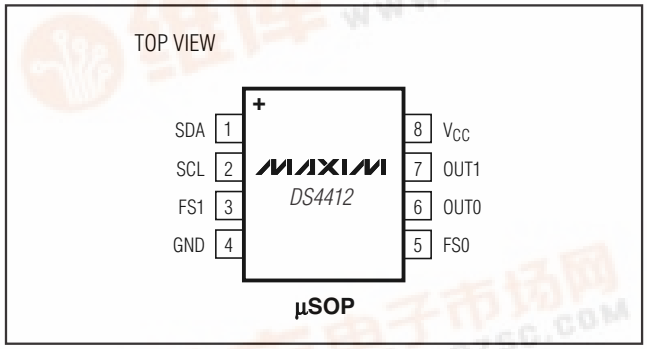
Power-Supply Margining

Adjustable Current Sink or Source

Features

- Two Current DACs
- Full-Scale Current 500µA to 2mA
- Full-Scale Range for Each DAC Determined by External Resistors
- 15 Settings Each for Sink and Source Modes
- I²C-Compatible Serial Interface
- Low Cost
- Small Package (8-Pin µSOP)
- -40°C to +85°C Temperature Range
- 2.7V to 5.5V Operation

Pin Configuration

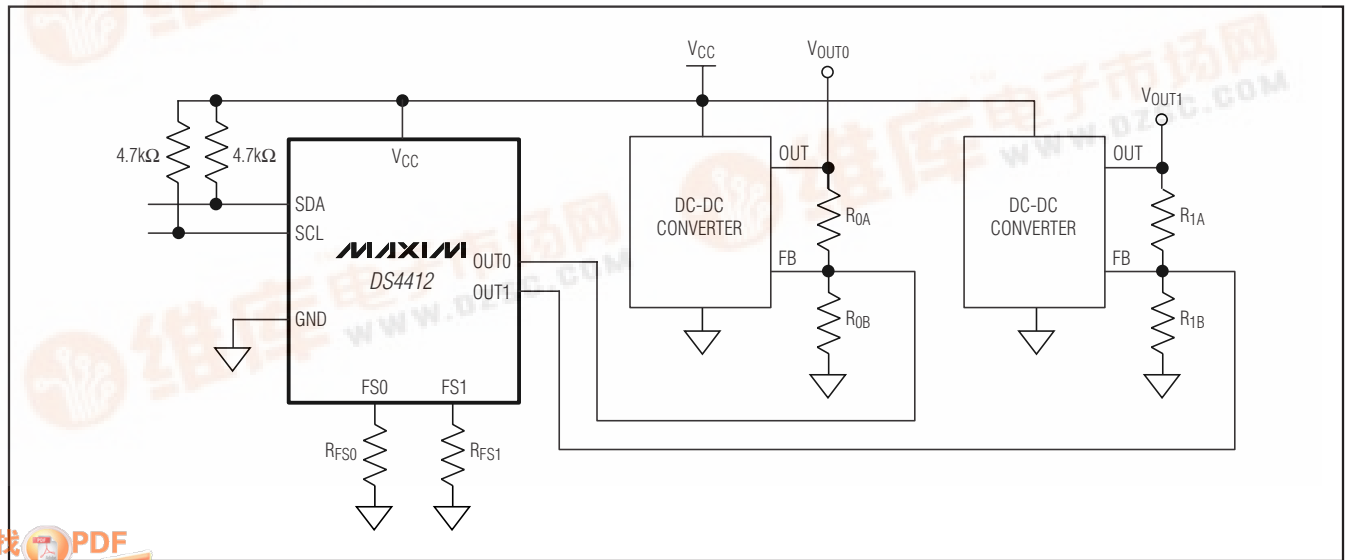


Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS4412U+	-40°C to +85°C	8 µSOP
DS4412U+T&R	-40°C to +85°C	8 µSOP

+Denotes a lead-free package.
T&R = Tape and reel.

Typical Operating Circuit



Dual-Channel, I²C Adjustable Sink/Source Current DAC

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC}, SDA, and SCL Relative to Ground.....-0.5V to +6.0V
Voltage Range on OUT0, OUT1 Relative to Ground .....-0.5V to (V_{CC} + 0.5V) (Not to exceed 6.0V.)
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....Refer to IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.7		5.5	V
Input Logic 1 (SDA, SCL)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SDA, SCL)	V_{IL}		-0.3		0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	V_{CC} = 5.5V (Note 2)			500	µA
Input Leakage (SDA, SCL)	I_{IL}	V_{CC} = 5.5V			1	µA
Output Leakage (SDA)	I_L				1	µA
Output Current Low (SDA)	I_{OL}	V_{OL} = 0.4V	3			mA
		V_{OL} = 0.6V	6			
R_{FS} Voltage	V_{RFS}			0.607		V

OUTPUT CURRENT CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage for Sinking	$V_{OUT:SINK}$	V_{CC} > $V_{OUT:SINK}$ (Note 3)	0.5		3.5	V
Output Voltage for Sourcing Current	$V_{OUT:SOURCE}$	(Note 3)	0		V_{CC} - 0.75	V
Full-Scale Sink Output Current	$I_{OUT:SINK}$	(Note 3)	0.5		2.0	mA
Full-Scale Source Output Current	$I_{OUT:SOURCE}$	(Note 3)	-2.0		-0.5	mA
Output-Current Full-Scale Accuracy	$I_{OUT:FS}$	+25°C, V_{CC} = 4.0V; using 0.1% R_{FS} resistor (Note 4) V_{OUT0} = V_{OUT1} = 1.2V			±6	%
Output-Current Temperature Coefficient	$I_{OUT:TC}$	(Note 5)		±75		ppm/°C
Output-Current Variation due to Power-Supply Change		DC source		+0.36		%/V
		DC sink		+0.12		

OUTPUT CURRENT CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Current Variation due to Output Voltage Change		DC source, V_{OUT} measured at 1.2V		-0.02		%/V
		DC sink, V_{OUT} measured at 1.2V		+0.12		
Output Leakage Current at Zero Current Setting	I_{ZERO}		-1		+1	µA
Output-Current Differential Linearity	DNL	(Note 6)			0.5	LSB
Output-Current Integral Linearity	INL	(Note 7)			1	LSB

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 8)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{DH:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 9)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 9)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 9)			400	pF

Note 1: All voltages with respect to ground, currents entering the IC are specified positive and currents exiting the IC are negative.

Note 2: Supply current specified with all outputs set to zero current setting with all inputs driven to well-defined logic levels. SDA and SCL are connected to V_{CC}. Excludes current through R_{FS} resistors (I_{RFS}). Total current includes I_{CC} + 2.5 x (I_{RFS0} + I_{RFS0}).

Note 3: The output voltage range must be satisfied to ensure the device meets its accuracy and linearity specifications.

Note 4: Input resistors R_{FS} must be between 2.25kΩ and 9.0kΩ to ensure the device meets its accuracy and linearity specifications.

Note 5: Temperature drift excludes drift caused by external resistor.

Note 6: Differential linearity is defined as the difference between the expected incremental current increase with respect to position and the actual increase. The expected incremental increase is the full-scale range divided by 15.

Note 7: Integral linearity is defined as the difference between the expected value as a function of the setting and the actual value. The expected value is a straight line between the zero and the full-scale values proportional to the setting.

Note 8: Timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I²C standard-mode timing.

Note 9: C_B—total capacitance of one bus line in pF.

Dual-Channel, I²C Adjustable Sink/Source Current DAC

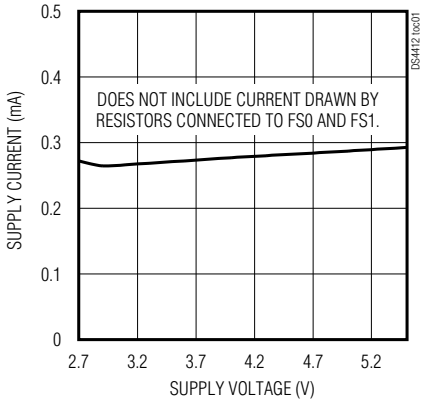
Pin Description

NAME	PIN	FUNCTION
SDA	1	I²C Serial Data. Input/output for I²C data.
SCL	2	I²C Serial Clock. Input for I²C clock.
FS1	3	Full-Scale Calibration Inputs. A resistor to ground on these pins determines the full-scale current for each output. FS0 controls OUT0, FS1 controls OUT1.
FS0	5	
GND	4	Ground
OUT0	6	Current Outputs. Sinks or sources the current determined by the register settings and the resistance connected to FS0 and FS1.
OUT1	7	
V_{CC}	8	Power Supply

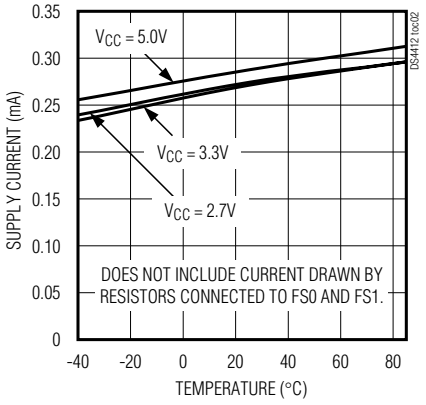
Typical Operating Characteristics

(Applies to OUT0 and OUT1. V_{CC} = 2.7V to 5.0V, SDA = SCL = V_{CC}, T_A = +25°C, and no loads on OUT0, OUT1, FS0, or FS1, unless otherwise noted.)

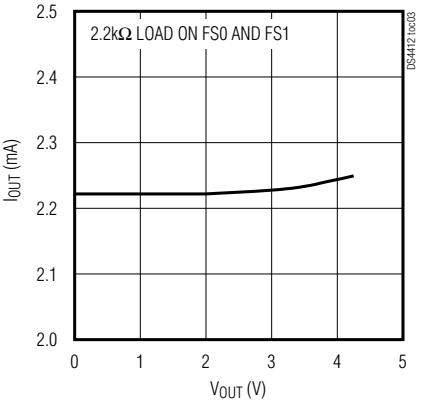
SUPPLY CURRENT vs. SUPPLY VOLTAGE



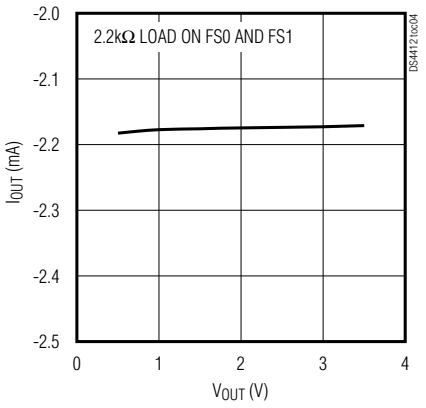
SUPPLY CURRENT vs. TEMPERATURE



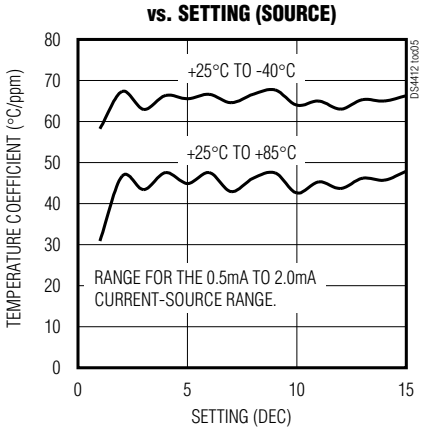
VOLTCO (SOURCE)



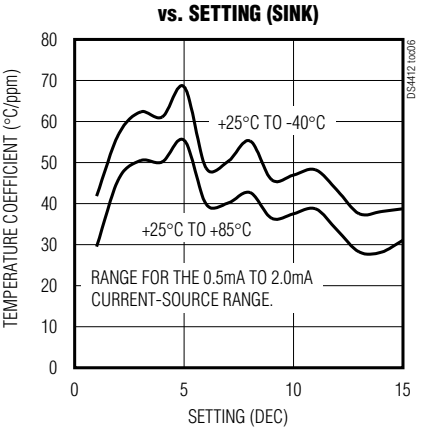
VOLTCO (SINK)



TEMPERATURE COEFFICIENT vs. SETTING (SOURCE)



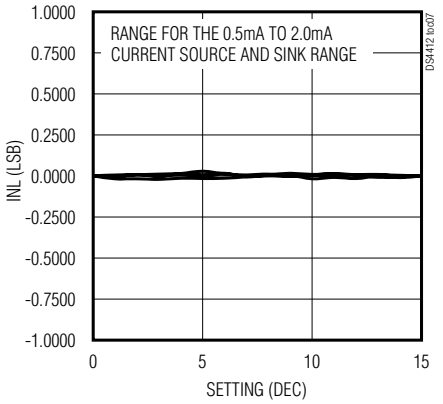
TEMPERATURE COEFFICIENT vs. SETTING (SINK)



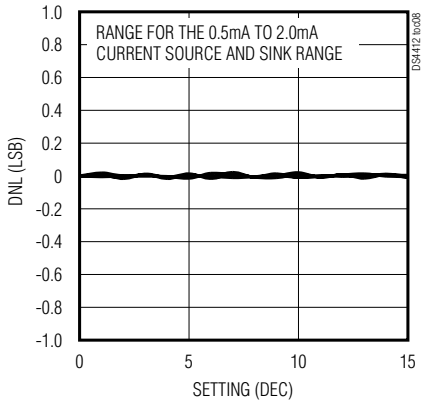
Typical Operating Characteristics (continued)

(Applies to OUT0 and OUT1. V_{CC} = 2.7V to 5.0V, SDA = SCL = V_{CC}, T_A = +25°C, and no loads on OUT0, OUT1, FS0, or FS1, unless otherwise noted.)

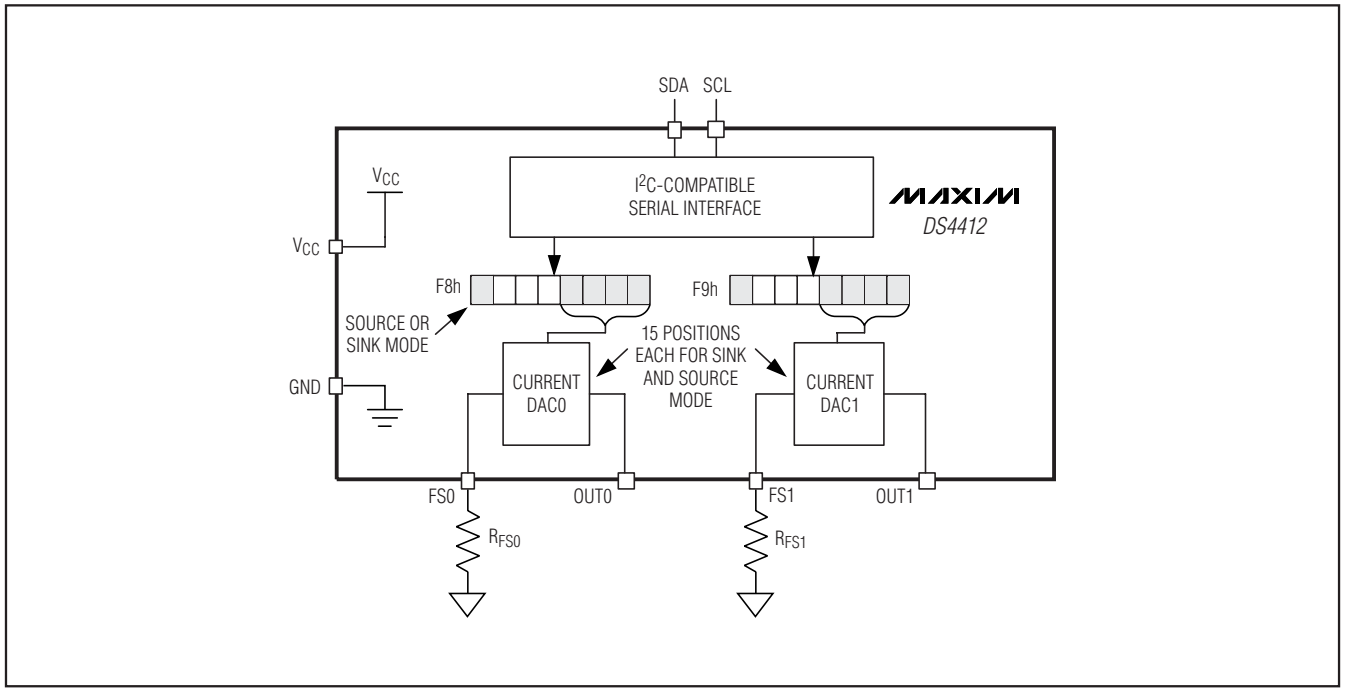
INTEGRAL LINEARITY



DIFFERENTIAL LINEARITY



Block Diagram



Dual-Channel, I²C Adjustable Sink/Source Current DAC

Detailed Description

The DS4412 contains two I²C adjustable-current sources that are each capable of sinking and sourcing current. Each output, OUT0 and OUT1, has 15 sink and 15 source settings that are programmed through the I²C interface. The full-scale ranges and corresponding step sizes of the outputs are determined by external resistors, connected to pins FS0 and FS1, which can adjust the output currents over a 4:1 range. The formula to determine the positive and negative full-scale current ranges for each of the four outputs is given by:

$$R_{FS} = (V_{RFS} / I_{FS}) \times (15 / 1.974)$$

where V_{RFS} is the R_{FS} voltage (see *DC Electrical Characteristics*), and R_{FS} is the external resistor value.

On power-up, the DS4412 outputs zero current. This is done to prevent it from sinking or sourcing an incorrect current before the system host controller has had a chance to modify the device's setting.

As a source for biasing instrumentation or other circuits, the DS4412 provides a simple and inexpensive current source with an I²C interface for control. The adjustable full-scale range allows the application to get the most out of its 4-bit sink or source resolution.

When used in adjustable power-supply applications (see *Typical Operating Circuit)*, the DS4412 does not affect the initial power-up supply voltage because it defaults to providing zero output current on power-up. As it sources or sinks current into the feedback voltage node, it changes the amount of output voltage required by the regulator to reach its steady state operating point. Using the external resistor, R_{FS}, to set the output current range, the DS4412 provides some flexibility for adjusting the range over which the power supply can be controlled or margined.

Memory Organization

The DS4412's current sources are controlled by writing to the memory addresses in Table 1.

Table 1. Memory Addresses

MEMORY ADDRESS (HEXADECIMAL)	CURRENT SOURCE
0xF8	OUT0
0xF9	OUT1

The format of each output control register is given by:

MSB							LSB
S	X	X	X	D_3	D_2	D_1	D_0

Where:

BIT	NAME	FUNCTION	POWER-ON DEFAULT
S	Sign Bit	Determines if DAC sources or sinks current. For sink S = 0, for source S = 1.	0b
X	Reserved	Reserved.	XXX
D_X	Data	4-Bit Data Word Controlling DAC Output. Setting 0000b outputs zero current regardless of the state of the sign bit.	0000b

Example: R_{FS0} = 4.8kΩ and register 0xF8h is written to a value of 0x8Ah. Calculate the output current.

$$I_{FS} = (0.607V / 4.8k\Omega) \times (15 / 1.974) = 949.85\mu A$$

The MSB of the output register is 1, so the output is sourcing the value corresponding to position Ah (10 decimal). The magnitude of the output current is equal to:

$$949.85\mu A \times (10 / 15) = 633.23\mu A$$

I²C Serial Interface Description

I²C Slave Address

The DS4412's slave address is 90h.

I²C Definitions

The following terminology is commonly used to describe I²C data transfers:

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 1 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 1 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 1 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL, plus the setup and hold time requirements (Figure 1). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 1) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the ninth bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the ninth bit. A device performs a NACK by transmitting a one during the ninth bit. Timing for the ACK and NACK is identical to all other bit writes (Figure 2). An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a

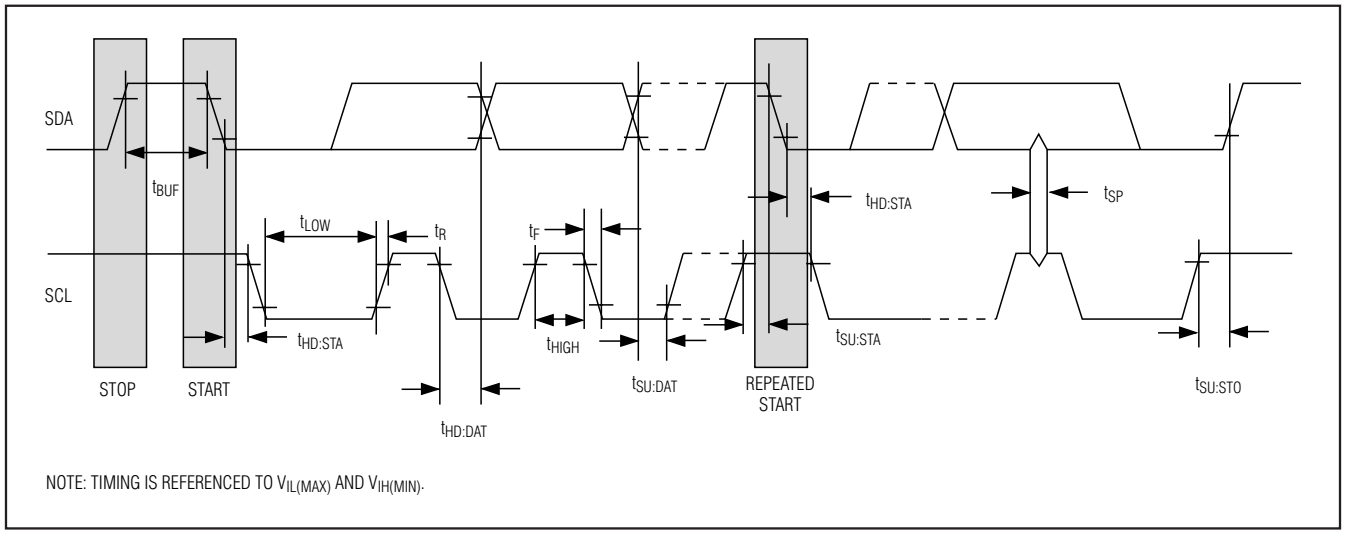


Figure 1. I²C Timing Diagram

Dual-Channel, I²C Adjustable Sink/Source Current DAC

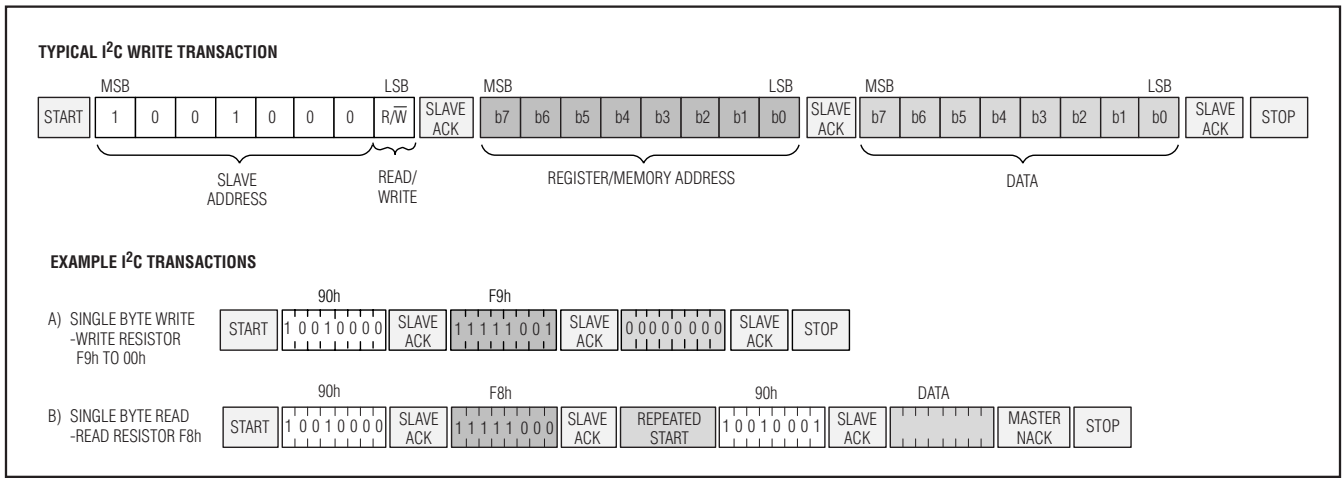


Figure 2. I²C Communication Examples

read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition, and the acknowledgement is read using the bit-read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminated communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The DS4412's slave address is 90h.

When the R/$\overline{W}$ bit is 0 (such as in 90h), the master is indicating it will write data to the slave. If R/$\overline{W}$ = 1 (91h in this case), the master is indicating it wants to read from the slave. If an incorrect slave address is written, the DS4412 assumes the master is communicating with another I²C device and ignores the communication until the next START condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte-write operations.

Reading from a Slave: To read from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Application Information

Example Calculation for an Adjustable Power Supply

In this example, the Typical Operating Circuit is used as a base to create Figure 3, a 2.0V voltage supply with ±20% margin. The adjustable power supply has a DC-DC converter output voltage, V_{OUT}, of 2.0V and a DC-DC converter feedback voltage, V_{FB}, of 0.8V. To determine the relationship of R_{0A} and R_{0B}, we start with the equation:

$$V_{FB} = \frac{R_{0B}}{R_{0A} + R_{0B}} \times V_{OUT}$$

Substituting V_{FB} = 0.8V and V_{OUT} = 2.0V, the relationship between R_{0A} and R_{0B} is determined to be:

$$R_{0A} = 1.5 \times R_{0B}$$

I_{OUT0} is chosen to be 1mA (midrange source/sink current for the DS4412). Summing the currents into the feedback node, we have the following

$$I_{OUT0} = I_{R0B} - I_{R0A}$$

Where:

$$I_{R0B} = \frac{V_{FB}}{R_{0B}}$$

And

$$I_{R0A} = \frac{V_{OUT} - V_{FB}}{R_{0A}}$$

To create a 20% margin in the supply voltage, the value of V_{OUT} is set to 2.4V. With these values in place, R_{0B} is calculated to be 267Ω, and R_{0A} is calculated to be 400Ω. The current DAC in this configuration allows the output voltage to be moved linearly from 1.6V to 2.4V using 15 settings. This corresponds to a resolution of 25.8mV/step.

VCC Decoupling

To achieve the best results when using the DS4412, decouple the power supply with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

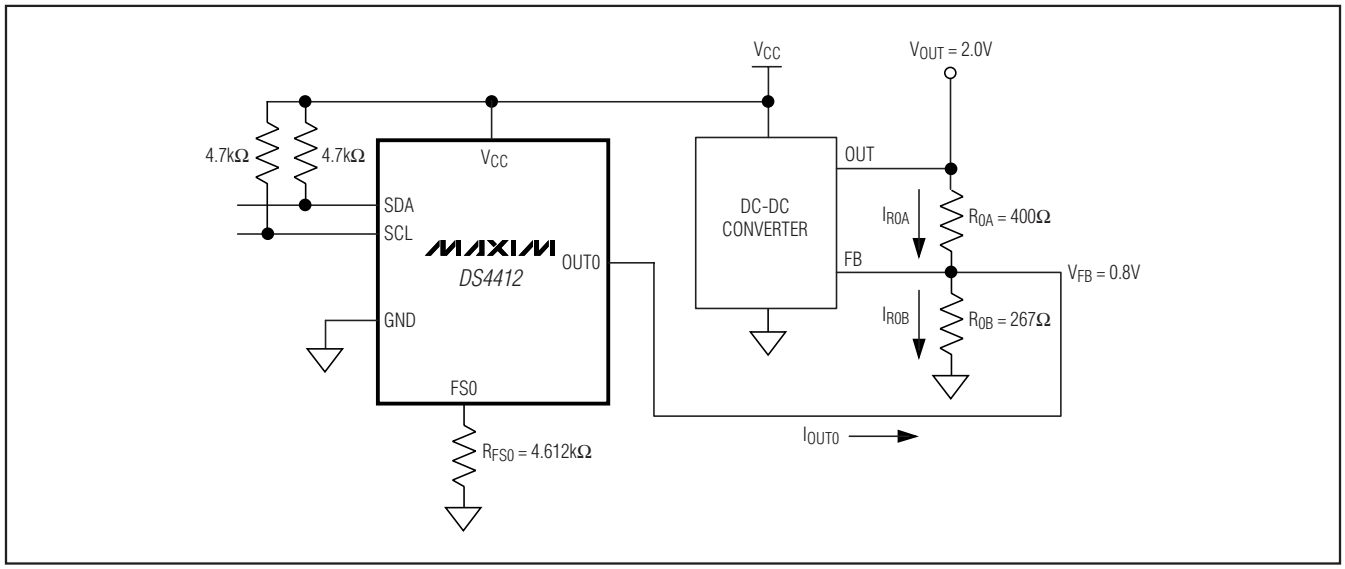


Figure 3. Example Application Circuit

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.