FAN7382
Half-Bridge Gate-Driver IC

Features
- Floating Channels Designed for Bootstrap Operation to +600V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative V_S Swing to -9V for Signal Propagation at V_CC=V_BS=15V
- V_CC & V_BS Supply Range from 10V to 20V
- UVLO Functions for Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50nsec
- Output In-phase with Input

Applications
- PDP Scan Driver
- Fluorescent Lamp Ballast
- SMPS
- Motor Driver

Description
The FAN7382, a monolithic half-bridge gate-driver IC, can drive MOSFETs and IGBTs that operate up to +600V. Fairchild’s high-voltage process and common-mode noise canceling technique provides stable operation of the high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to V_S=-9.8V (typical) for V_BS=15V. The input logic level is compatible with standard TTL-series logic gates. UVLO circuits for both channels prevent malfunction when V_CC or V_BS is lower than the specified threshold voltage. Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for fluorescent lamp ballasts, PDP scan drivers, motor controls, etc.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Pb-Free</th>
<th>Operating Temperature Range</th>
<th>Packing Method</th>
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<td>FAN7382N</td>
<td>8-DIP</td>
<td></td>
<td></td>
<td>Tube</td>
</tr>
<tr>
<td>FAN7382M¹</td>
<td>8-SOP</td>
<td></td>
<td>-40°C ~ 125°C</td>
<td>Tube</td>
</tr>
<tr>
<td>FAN7382MX¹</td>
<td></td>
<td>Yes</td>
<td></td>
<td>Tape &amp; Reel</td>
</tr>
<tr>
<td>FAN7382M1(¹)</td>
<td>14-SOP</td>
<td></td>
<td></td>
<td>Tube</td>
</tr>
<tr>
<td>FAN7382M1X(¹)</td>
<td></td>
<td></td>
<td></td>
<td>Tape &amp; Reel</td>
</tr>
</tbody>
</table>

Note:
1. These devices passed wave soldering test by JESD22A-111.
**Typical Application Circuit**

![Application Circuit Diagram](attachment:image.png)

**Figure 1. Application Circuit for Half-Bridge**

**Internal Block Diagram**

![Block Diagram](attachment:image.png)

**Figure 2. Functional Block Diagram**
Pin Assignments

Figure 3. Pin Configuration (Top View)

Pin Definitions

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Low-Side Supply Voltage</td>
</tr>
<tr>
<td>HIN</td>
<td>Logic Input for High-Side Gate Driver Output</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic Input for Low-Side Gate Driver Output</td>
</tr>
<tr>
<td>COM</td>
<td>Logic Ground and Low-Side Driver Return</td>
</tr>
<tr>
<td>LO</td>
<td>Low-Side Driver Output</td>
</tr>
<tr>
<td>VS</td>
<td>High-Voltage Floating Supply Return</td>
</tr>
<tr>
<td>HO</td>
<td>High-Side Driver Output</td>
</tr>
<tr>
<td>VB</td>
<td>High-Side Floating Supply</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings
Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
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<tr>
<td>$V_S$</td>
<td>High-side offset voltage</td>
<td>$V_B-25$</td>
<td>$V_B+0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_B$</td>
<td>High-side floating supply voltage</td>
<td>-0.3</td>
<td>625</td>
<td></td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>High-side floating output voltage HO</td>
<td>$V_S-0.3$</td>
<td>$V_B+0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low-side and logic fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td></td>
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<tr>
<td>$V_{LO}$</td>
<td>Low-side output voltage LO</td>
<td>-0.3</td>
<td>$V_{CC}+0.3$</td>
<td></td>
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<tr>
<td>$V_{IN}$</td>
<td>Logic input voltage (HIN, LIN)</td>
<td>-0.3</td>
<td>$V_{CC}+0.3$</td>
<td></td>
</tr>
<tr>
<td>COM</td>
<td>Logic ground</td>
<td>$V_{CC}-25$</td>
<td>$V_{CC}+0.3$</td>
<td></td>
</tr>
<tr>
<td>$dV_S/dt$</td>
<td>Allowable offset voltage slew rate</td>
<td>50</td>
<td></td>
<td>V/nsec</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power dissipation</td>
<td>8-SOP</td>
<td>0.625</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14-SOP</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-DIP</td>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal resistance, junction-to-ambient</td>
<td>8-SOP</td>
<td>200</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14-SOP</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-DIP</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction temperature</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage temperature</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
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</table>
Electrical Characteristics

$V_{\text{BIAS}} (V_{CC}, V_{BS})=15.0\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified. The $V_{\text{IN}}$, $V_{\text{TH}}$, and $I_{\text{IN}}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and $V_S$ is applicable to HO and LO.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Test Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$V_{CC UV+}$</td>
<td>$V_{CC}$ and $V_{BS}$ supply under-voltage positive going threshold</td>
<td>$8.2$</td>
<td>$9.2$</td>
<td>$10.0$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{BS UV+}$</td>
<td>$V_{CC}$ and $V_{BS}$ supply under-voltage negative going threshold</td>
<td>$7.6$</td>
<td>$8.7$</td>
<td>$9.6$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CC UVH}$</td>
<td>$V_{CC}$ supply under-voltage lockout hysteresis</td>
<td>$0.6$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LK}$</td>
<td>Offset supply leakage current</td>
<td>$V_B=V_S=600\text{V}$</td>
<td></td>
<td>$50$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{QBS}$</td>
<td>Quiescent $V_{BS}$ supply current</td>
<td>$V_{IN}=0\text{V}$ or $5\text{V}$</td>
<td>$45$</td>
<td>$120$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{QCC}$</td>
<td>Quiescent $V_{CC}$ supply current</td>
<td>$V_{IN}=0\text{V}$ or $5\text{V}$</td>
<td>$70$</td>
<td>$180$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{PBS}$</td>
<td>Operating $V_{BS}$ supply current</td>
<td>$f_{IN}=20\text{kHz}$, rms value</td>
<td></td>
<td>$600$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{PCC}$</td>
<td>Operating $V_{CC}$ supply current</td>
<td>$f_{IN}=20\text{kHz}$, rms value</td>
<td></td>
<td>$600$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Logic &quot;1&quot; input voltage</td>
<td></td>
<td>$2.9$</td>
<td></td>
<td>V</td>
<td></td>
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<tr>
<td>$V_{IL}$</td>
<td>Logic &quot;0&quot; input voltage</td>
<td></td>
<td>$0.8$</td>
<td></td>
<td>V</td>
<td></td>
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<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage, $V_{\text{BIAS}}-V_O$</td>
<td>$I_O=20\text{mA}$</td>
<td>$1.0$</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage, $V_O$</td>
<td></td>
<td>$0.6$</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{IN+}$</td>
<td>Logic &quot;1&quot; input bias current</td>
<td>$V_{IN}=5\text{V}$</td>
<td>$10$</td>
<td>$20$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{IN-}$</td>
<td>Logic &quot;0&quot; input bias current</td>
<td>$V_{IN}=0\text{V}$</td>
<td>$1.0$</td>
<td>$2.0$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{O+}$</td>
<td>Output high short-circuit pulsed current</td>
<td>$V_O=0\text{V}$, $V_{IN}=5\text{V}$ with $PW&lt;10\mu\text{s}$</td>
<td>$250$</td>
<td>$350$</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{O-}$</td>
<td>Output low short-circuit pulsed current</td>
<td>$V_O=15\text{V}$, $V_{B}=V_B$, $V_{IN}=0\text{V}$ with $PW&lt;10\mu\text{s}$</td>
<td>$500$</td>
<td>$650$</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Allowable negative $V_S$ pin voltage for $HIN$ signal propagation to HO</td>
<td></td>
<td>$-9.8$</td>
<td>$-7.0$</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Dynamic Electrical Characteristics

$V_{\text{BIAS}} (V_{CC}, V_{BS})=15.0\text{V}$, $V_S=\text{COM}$, $C_L=1000\text{pF}$ and, $T_A = 25^\circ\text{C}$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristics</th>
<th>Test Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td>Turn-on propagation delay</td>
<td>$V_S=0\text{V}$</td>
<td>$100$</td>
<td>$170$</td>
<td>$300$</td>
<td>nsec</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-off propagation delay</td>
<td>$V_S=0\text{V}$ or $600\text{V}$</td>
<td>$100$</td>
<td>$200$</td>
<td>$300$</td>
<td>nsec</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Turn-on rise time</td>
<td></td>
<td>$20$</td>
<td>$60$</td>
<td>$140$</td>
<td>nsec</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Turn-off fall time</td>
<td></td>
<td>$30$</td>
<td>$80$</td>
<td></td>
<td>nsec</td>
</tr>
<tr>
<td>MT</td>
<td>Delay matching, HS &amp; LS turn-on/off</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50</td>
</tr>
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</table>
Typical Characteristics

Figure 4. Turn-On Propagation Delay vs. Supply Voltage

Figure 5. Turn-On Propagation Delay vs. Temp.

Figure 6. Turn-Off Propagation Delay vs. Supply Voltage

Figure 7. Turn-Off Propagation Delay vs. Temp.

Figure 8. Turn-On Rising Time vs. Supply Voltage

Figure 9. Turn-On Rising Time vs. Temp.
Typical Characteristics (Continued)

Figure 10. Turn-Off Falling Time vs. Supply Voltage

Figure 11. Turn-Off Falling Time vs. Temp.

Figure 12. Output Sourcing Current vs. Supply Voltage

Figure 13. Output Sourcing Current vs. Temp

Figure 14. Output Sinking Current vs. Supply Voltage

Figure 15. Output Sinking Current vs. Temp.
Typical Characteristics (Continued)

Figure 16. Allowable Negative $V_S$ Voltage for Signal Propagation to High Side vs. Supply Voltage

Figure 17. Allowable Negative $V_S$ Voltage for Signal Propagation to High Side vs. Temp.

Figure 18. $I_{QCC}$ vs. Supply Voltage

Figure 19. $I_{QCC}$ vs. Temp.

Figure 20. $I_{QBS}$ vs. Supply Voltage

Figure 21. $I_{QBS}$ vs. Temp.
Typical Characteristics (Continued)

Figure 22. High-Level Output Voltage vs. Supply Voltage

Figure 23. High-Level Output Voltage vs. Temp.

Figure 24. Low-Level Output Voltage vs. Supply Voltage

Figure 25. Low-Level Output Voltage vs. Temp.

Figure 26. Input Bias Current vs. Supply Voltage

Figure 27. Input Bias Current vs. Temp.
Typical Characteristics (Continued)

Figure 28. V_CC UVLO Threshold Voltage vs. Temp.

Figure 29. V_BS UVLO Threshold Voltage vs. Temp.

Figure 30. V_B to COM Leakage Current vs. Temp.

Figure 31. Input Logic Threshold Voltage vs. Temp.
Typical Characteristics (Continued)

Figure 32. Switching Time Test Circuit

Figure 33. Input / Output Timing Diagram

Figure 34. Switching Time Waveform Definition

Figure 35. Delay Matching Waveform Definition

$HIN$  $VCC$  $LIN$  $COM$  $LO$  $VS$  $HO$  $VB$

$15V_{DC} 15V_{DC}$ $1nF 1nF$ $100nF 100nF$ $10\mu F 10\mu F$

FAN7382 Rev.03

$ton$  $toff$  $tr$  $tf$

$50\% 50\%$ $10\% 90\%$ $10\% 90\%$

$HIN$  $LIN$  $LO$  $HO$

$ton-L$  $ton-H$  $toff-L$  $toff-H$

$MT$  $HOLO$

$FAN7382$  $Rev.03$

$FAN7382$  $Rev.04$
Mechanical Dimensions

8-SOP
Dimensions are in millimeters (inches) unless otherwise noted.

Figure 36. 8-Lead Small Outline Package
Mechanical Dimensions (Continued)

8-DIP
Dimensions are in millimeters (inches) unless otherwise noted.

Figure 37. 8-Lead Dual Inline Package
Mechanical Dimensions (Continued)

14-SOP

Dimensions are in millimeters (inches) unless otherwise noted.

Figure 38. 14-Lead Small Outline Package
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- FAST®
- FASTr™
- FPS™
- FRFET™
- FACT Quiet Series™
- GlobalOptoisolator™
- OPTOLOGIC®
- OPTOPLANAR™
- PACMAN™
- POP™
- Power247™
- PowerEdge™
- PowerSaver™
- PowerTrench®
- QFET®
- QS™
- QT Optoelectronics™
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- RapidConnect™
- µSerDes™
- ScalarPump™
- OCX™
- OCXPro™
- SMART START™
- SILENT SWITCHER®
- SMART START™
- SPM™
- Stealth™
- SuperFET™
- SuperSOT™-3
- SuperSOT™-6
- SuperSOT™-8
- SyncFET™
- TCM™
- TinyBoost™
- TinyBuck™
- TinyPWM™
- TinyPower™
- TinyLogic®
- TINYOPTO™
- TruTranslation™
- UniFET™
- VCX™
- Wire™
- I²C™
- i-Lo™
- ImpliedDisconnect™
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- LittleFET™
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- Quiet Series™
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- RapidConnect™
- µSerDes™
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- SPM™
- Stealth™
- SuperFET™
- SuperSOT™-3
- SuperSOT™-6
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

<table>
<thead>
<tr>
<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
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<tbody>
<tr>
<td>Advance Information</td>
<td>Formative or In Design</td>
<td>This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary</td>
<td>First Production</td>
<td>This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
</tr>
<tr>
<td>No Identification Needed</td>
<td>Full Production</td>
<td>This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
</tr>
<tr>
<td>Obsolete</td>
<td>Not In Production</td>
<td>This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.</td>
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