January 2006

FAIRCHILD SEMICONDUCTOR®

UniFET™

# FDA20N50
# 500V N-Channel MOSFET

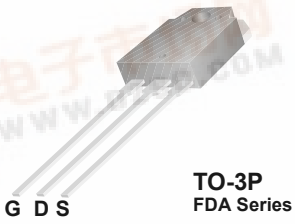
## Features

- 20A, 500V, $R_{DS(on)}$ = 0.24Ω @$V_{GS}$ = 10 V
- Low gate charge ( typical 45.6 nC)
- Low $C_{rss}$ ( typical 27 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

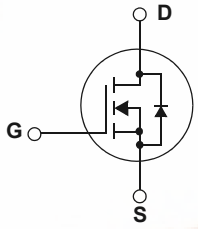
## Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.




TO-3P
FDA Series




## Absolute Maximum Ratings

| Symbol | Parameter | | FDA20N50 | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 500 | V |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C)<br>- Continuous ($T_C$ = 100°C) | 20<br>12.9 | A<br>A |
| $I_{DM}$ | Drain Current | - Pulsed (Note 1) | 80 | A |
| $V_{GSS}$ | Gate-Source voltage | | ± 30 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 1110 | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 20 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 25.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 4.5 | V/ns |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C)<br>- Derate above 25°C | 250<br>2.0 | W<br>W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds | | 300 | °C |

* Drain current limited by maximum junction termperature.

## Thermal Characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 0.50 | °C/W |
| $R_{\theta CS}$ | Thermal Resistance, Case-to-Sink | 0.24 | -- | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 40 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDA20N50 | FDA20N50 | TO-3P | -- | -- | 30 |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted

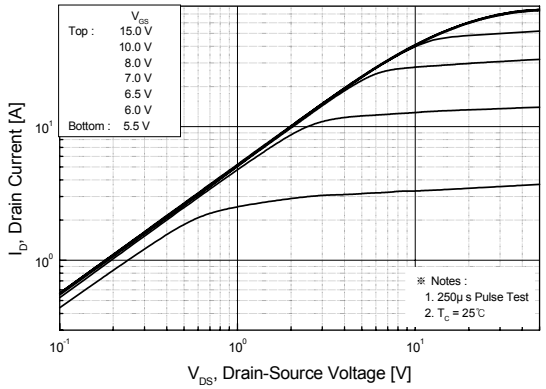
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = 250μA, $T_J$ = 25°C | 500 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, Referenced to 25°C | -- | 0.50 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 500V, $V_{GS}$ = 0V<br>$V_{DS}$ = 400V, $T_C$ = 125°C | --<br>-- | --<br>-- | 1<br>10 | μA<br>μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30V, $V_{DS}$ = 0V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30V, $V_{DS}$ = 0V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 3.0 | -- | 5.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10V, $I_D$ = 10A | -- | 0.20 | 0.24 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 40V, $I_D$ = 10A (Note 4) | -- | 24.6 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1.0MHz | -- | 2400 | 3120 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 355 | 465 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 27 | -- | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 250V, $I_D$ = 20A, $R_G$ = 25Ω | -- | 95 | 200 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 375 | 760 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 100 | 210 | ns |
| $t_f$ | Turn-Off Fall Time | (Note 4, 5) | -- | 105 | 220 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 400V, $I_D$ = 20A, $V_{GS}$ = 10V | -- | 45.6 | 59.5 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 14.8 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | (Note 4, 5) | -- | 21.6 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 20 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 80 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = 20A | -- | -- | 1.4 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0V, $I_S$ = 20A, $dI_F/dt$ =100A/μs (Note 4) | -- | 507 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 7.20 | -- | μC |

**NOTES:**

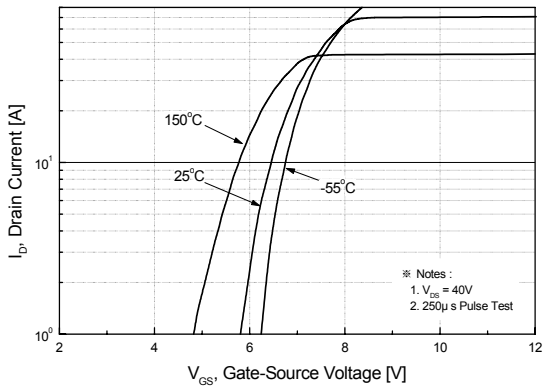
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 5.0mH, $I_{AS}$ = 20A, $V_{DD}$ = 50V, $R_G$ = 25Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 20A, di/dt ≤ 200A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

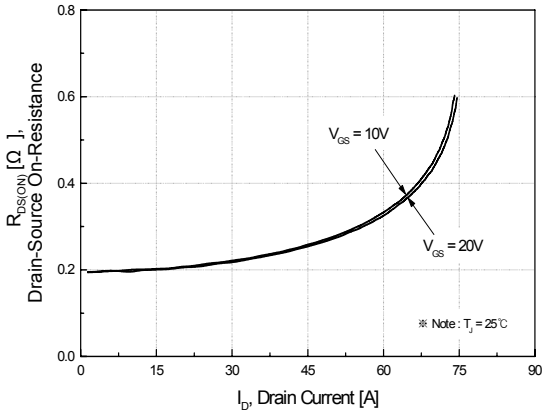
### Figure 1. On-Region Characteristics



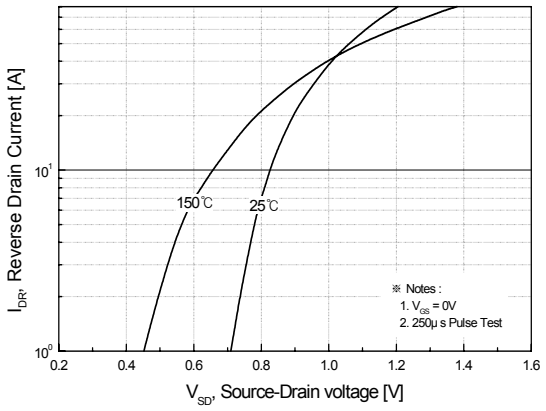

### Figure 2. Transfer Characteristics



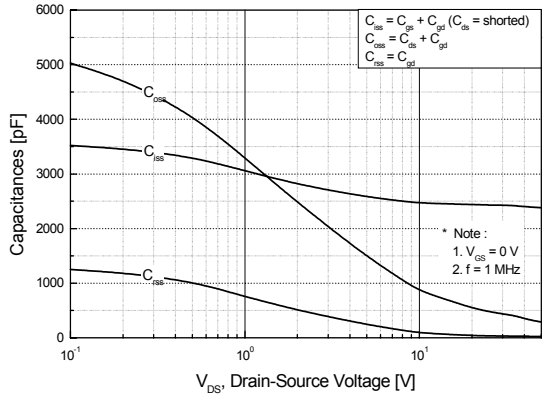

### Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage



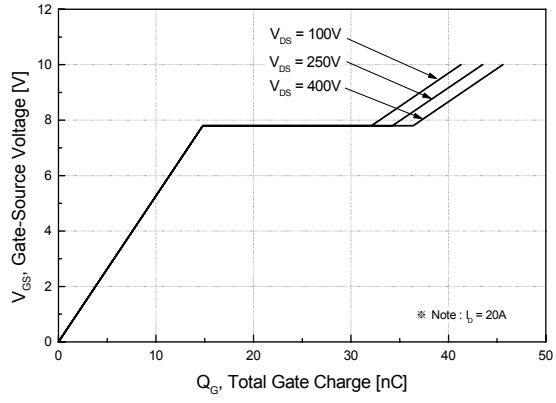

### Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue




### Figure 5. Capacitance Characteristics




### Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

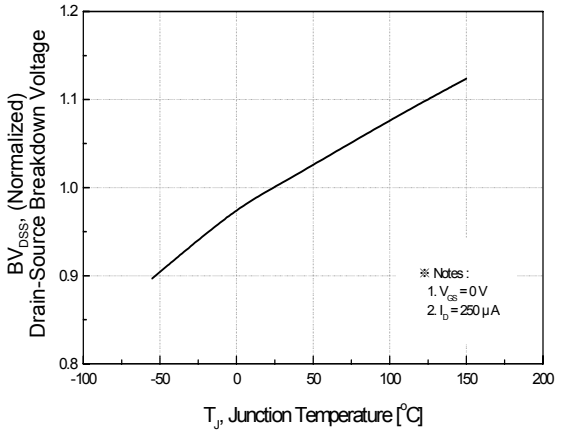



**Figure 8. On-Resistance Variation vs. Temperature**

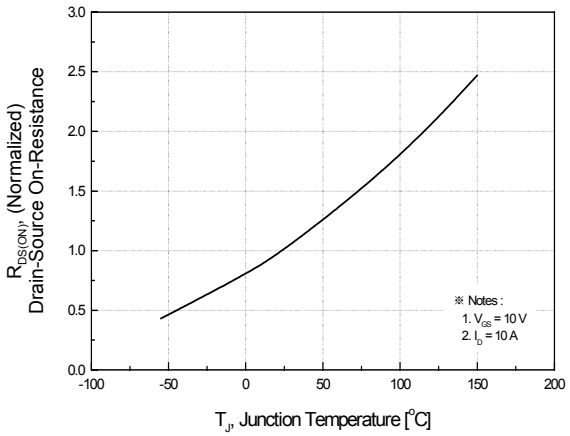



**Figure 9. Safe Operating Area**

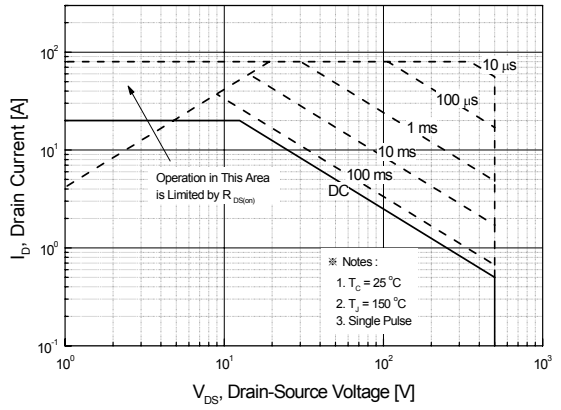



**Figure 10. Maximum Drain Current vs. Case Temperature**

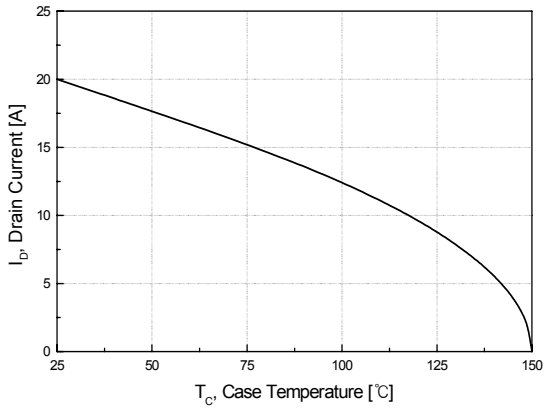
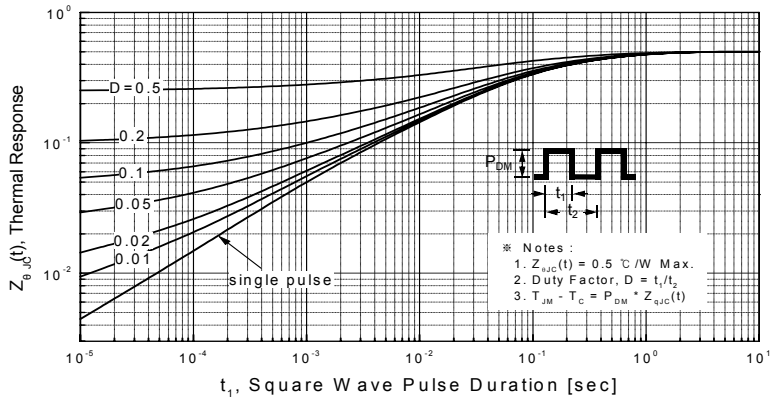
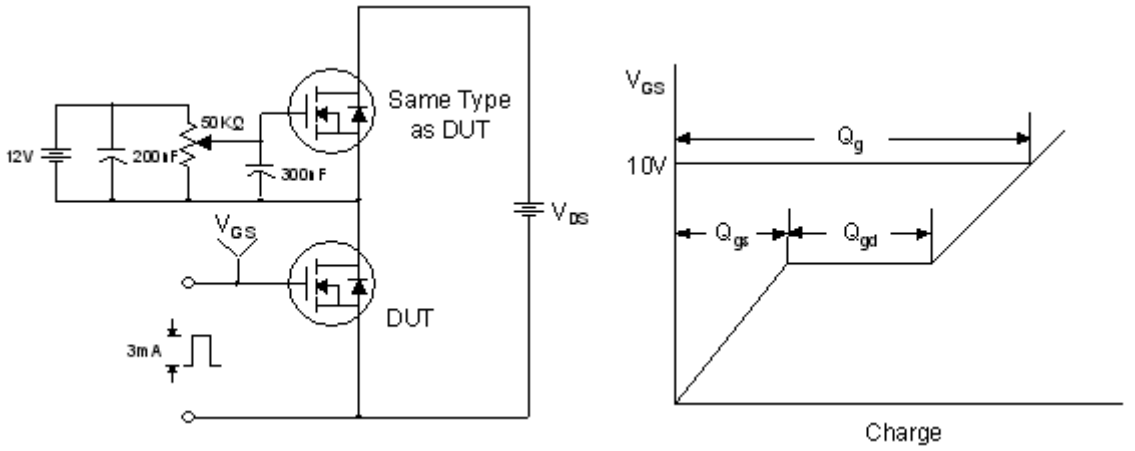


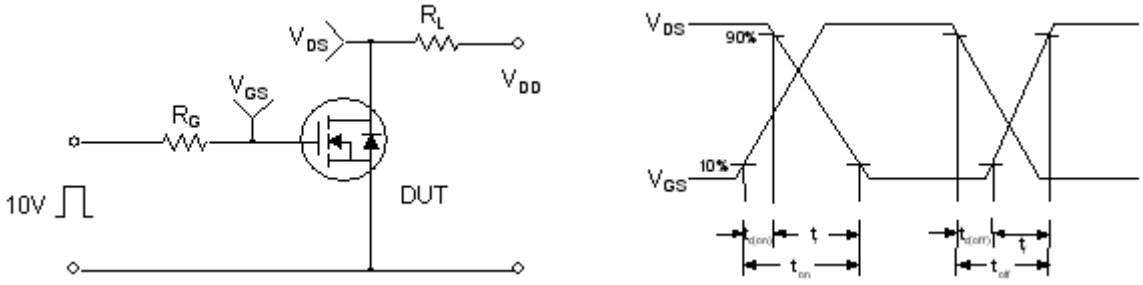

**Figure 11. Transient Thermal Response Curve**



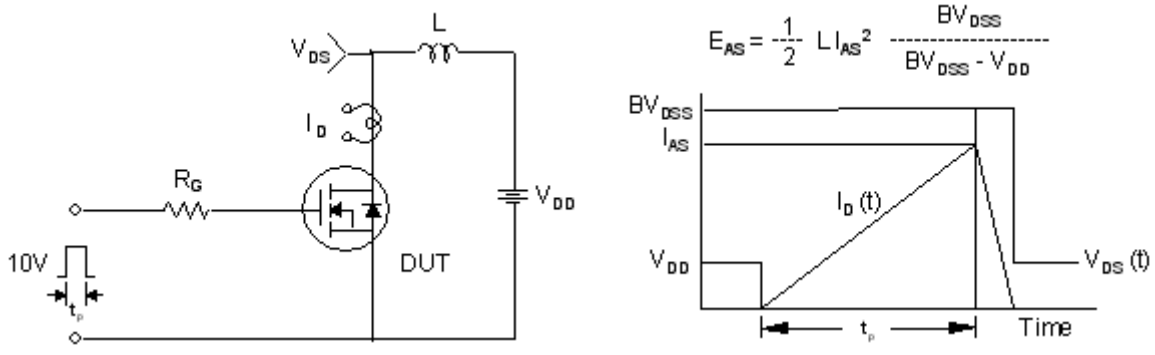
**Gate Charge Test Circuit & Waveform**



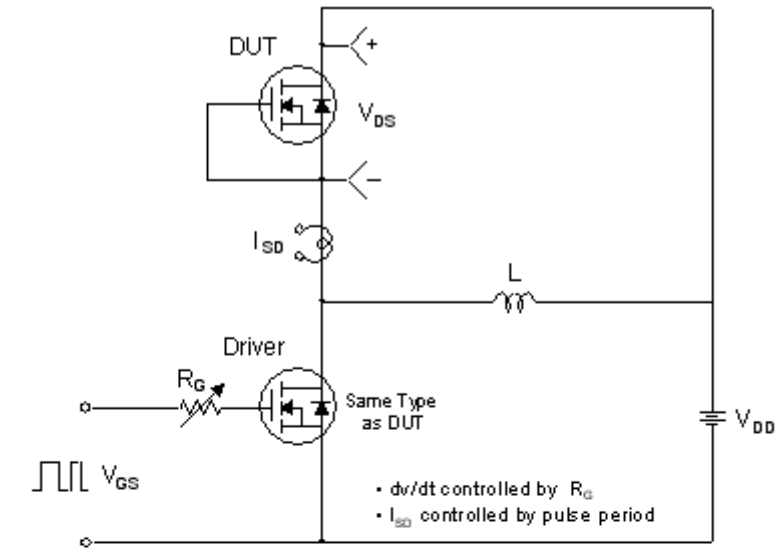

**Resistive Switching Test Circuit & Waveforms**

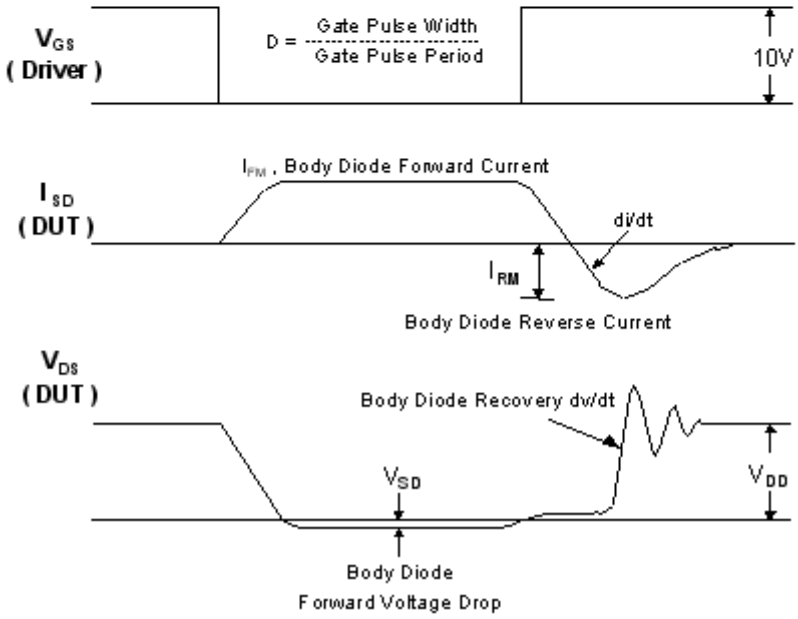



**Unclamped Inductive Switching Test Circuit & Waveforms**



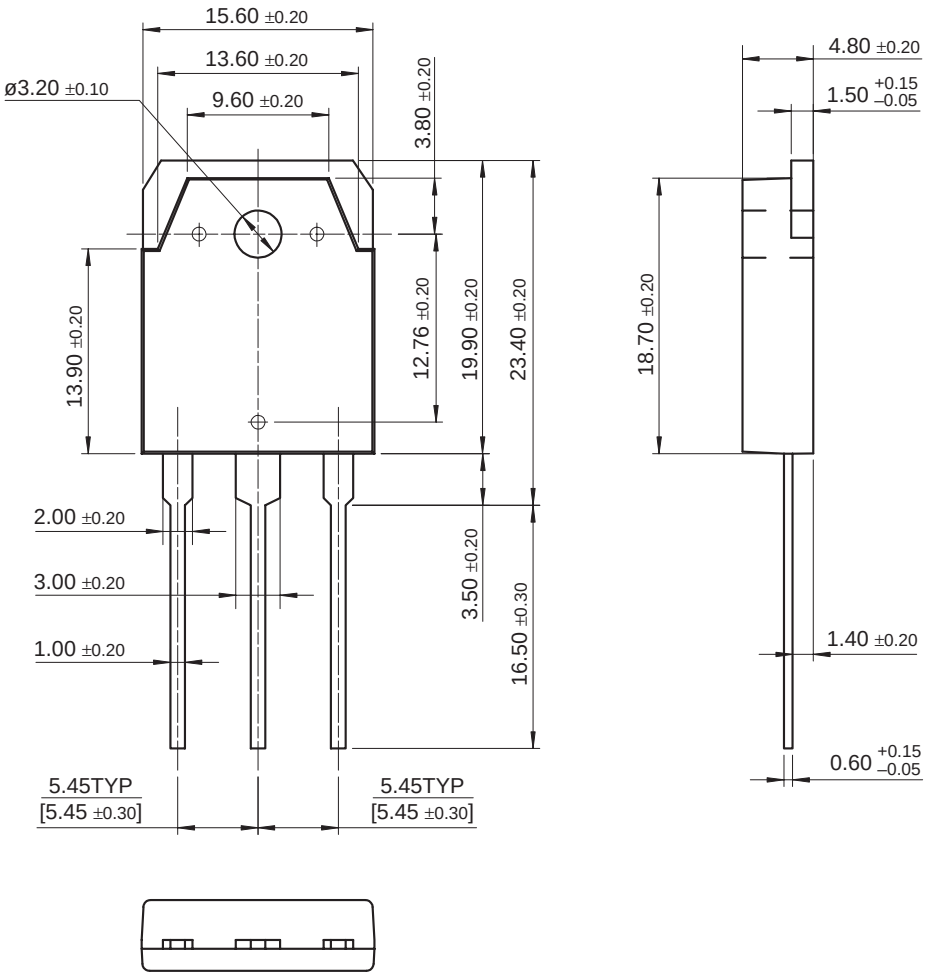
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



## Mechanical Dimensions

TO-3P




Dimensions in Millimeters

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

| | | | | |
|---|---|---|---|---|
| ACEx™ | FAST® | ISOPLANAR™ | PowerSaver™ | SuperSOT™-6 |
| ActiveArray™ | FASTr™ | LittleFET™ | PowerTrench® | SuperSOT™-8 |
| Bottomless™ | FPS™ | MICROCOUPLER™ | QFET® | SyncFET™ |
| Build it Now™ | FRFET™ | MicroFET™ | QS™ | TinyLogic® |
| CoolFET™ | GlobalOptoisolator™ | MicroPak™ | QT Optoelectronics™ | TINYOPTO™ |
| *CROSSVOLT*™ | GTO™ | MICROWIRE™ | Quiet Series™ | TruTranslation™ |
| DOME™ | HiSeC™ | MSX™ | RapidConfigure™ | UHC™ |
| EcoSPARK™ | $I^2C$™ | MSXPro™ | RapidConnect™ | UltraFET® |
| $E^2CMOS$™ | *i-Lo*™ | OCX™ | µSerDes™ | UniFET™ |
| EnSigna™ | ImpliedDisconnect™ | OCXPro™ | ScalarPump™ | VCX™ |
| FACT™ | IntelliMAX™ | OPTOLOGIC® | SILENT SWITCHER® | Wire™ |
| FACT Quiet Series™ | | OPTOPLANAR™ | SMART START™ | |
| | | PACMAN™ | SPM™ | |
| Across the board. Around the world.™ | | POP™ | Stealth™ | |
| The Power Franchise® | | Power247™ | SuperFET™ | |
| Programmable Active Droop™ | | PowerEdge™ | SuperSOT™-3 | |

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| Obsolete | Not In Production | This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only. |

Rev. I17