

# HM65256B Series

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捷多邦, 专业PCB打样工厂, 24小时

5.0 V Supply

32,768-word × 8-bit High Speed Psuedo Static RAM

## Features

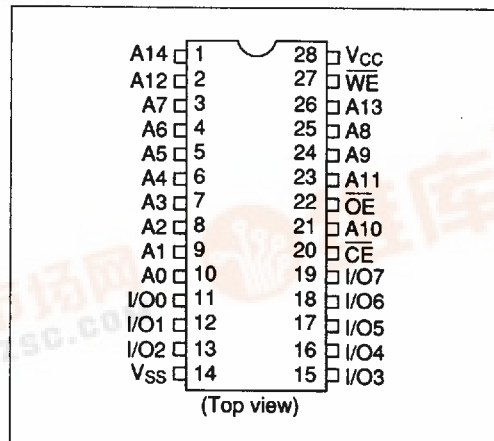
- Single 5 V (±10%)
- Access time
  - $\overline{CE}$  access time: 100/120/150/200 ns
  - Address access time: 50/60/75/100 ns (in static column mode)
- Cycle time
  - Random read/write cycle time: 160/190/235/310 ns
  - Static column mode cycle time: 55/65/80/105 ns
- Low power: 175 mW typ. active
- All inputs and outputs TTL compatible
- Static column mode capability
- Non-multiplexed address
- 256 refresh cycles (4 ms)
- Refresh functions
  - Address refresh
  - Automatic refresh
  - Self refresh

Type No.	Access time	Package
HM65256BLSP-10	100 ns	300-mil 28-pin plastic DIP
HM65256BLSP-12	120 ns	plastic DIP (DP-28N)
HM65256BLSP-15	150 ns	
HM65256BLSP-20	200 ns	
HM65256BFP-10T	100 ns	28-pin plastic SOP (FP-28DA)
HM65256BFP-12T	120 ns	
HM65256BFP-15T	150 ns	
HM65256BFP-20T	200 ns	
HM65256BLFP-10T	100 ns	
HM65256BLFP-12T	120 ns	
HM65256BLFP-15T	150 ns	
HM65256BLFP-20T	200 ns	

## Ordering Information

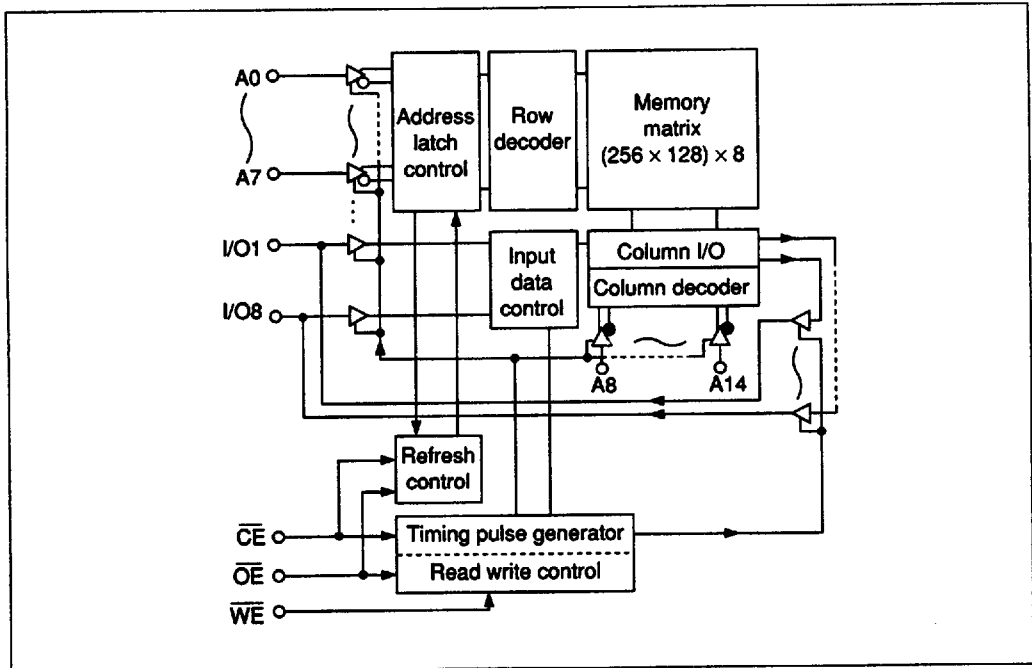
Type No.	Access time	Package
HM65256BP-10	100 ns	600-mil 28-pin plastic DIP
HM65256BP-12	120 ns	(DP-28)
HM65256BP-15	150 ns	
HM65256BP-20	200 ns	
HM65256BLP-10	100 ns	
HM65256BLP-12	120 ns	
HM65256BLP-15	150 ns	
HM65256BLP-20	200 ns	
HM65256BSP-10	100 ns	300-mil 28-pin plastic DIP
HM65256BSP-12	120 ns	(DP-28N)
HM65256BSP-15	150 ns	
HM65256BSP-20	200 ns	

## Pin Arrangement



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## Block Diagram



## Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	L	H	Low Z	Read
L	x	L	High Z	Write
L	H	H	High Z	—
H	L	x	High Z	Refresh
H	H	x	High Z	Standby

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### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

### Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input voltage	$V_{IH}$	2.2	—	6.0	V
	$V_{IL}$	-0.5*	—	0.8	V

Note:  $V_{IL}$  min = -3.0 V for pulse width  $\leq 10$  ns.

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DC Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ )

Parameter	Symbol	HM65256B			HM65256BL			Unit	Test conditions
		Min	Typ	Max	Min	Typ	Max		
Operating power supply current	$I_{CC1}$	—	35	65	—	35	65	mA	$I_{VO} = 0\text{ mA}$ , $t_{cyc} = \text{min}$
Standby power supply current	$I_{SB1}$	—	1	2	—	1	2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IH}$ , $V_{in} \geq 0\text{ V}$
	$I_{SB2}$	—	—	—	—	0.05	0.1	mA	$\overline{CE} > V_{CC} - 0.2\text{ V}$ , $\overline{OE} \geq V_{CC} - 0.2$ , $V_{in} \geq 0$
Operating power supply current in self refresh mode	$I_{CC2}$	—	1	2	—	0.6	1	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ , $V_{in} \geq 0\text{ V}$
	$I_{CC3}$	—	—	—	—	50	100	$\mu\text{A}$	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $\overline{OE} \leq 0.2\text{ V}$ , $V_{in} \geq 0\text{ V}$
Input leakage current	$I_{LI}$	-10	—	10	-10	—	10	$\mu\text{A}$	$V_{CC} = 5.5\text{ V}$ , $V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current	$I_{LO}$	-10	—	10	-10	—	10	$\mu\text{A}$	$\overline{OE} = V_{IH}$ , $V_{VO} = V_{SS}$ to $V_{CC}$
Output voltage	$V_{OL}$	—	—	0.4	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
	$V_{OH}$	2.4	—	—	2.4	—	—	V	$I_{OH} = -1\text{ mA}$

## Capacitance

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	$C_{in}$	—	5	pF	$V_{in} = 0\text{ V}$
Input/output capacitance	$C_{VO}$	—	7	pF	$V_{VO} = 0\text{ V}$

Note: These parameters are sampled and not 100% tested.

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### AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%)

#### AC Test Conditions:

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level: V<sub>OH</sub> = 2.0 V  
V<sub>OL</sub> = 0.8 V
- Output load: 1 TTL and 100 pF  
(including scope and jig)

Parameter	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Random read or write cycle time	t <sub>RC</sub>	160	—	190	—	235	—	310	—	ns
Static column mode read or write cycle	t <sub>RSC</sub>	55	—	65	—	80	—	105	—	ns
Chip enable access time	t <sub>CEA</sub>	—	100	—	120	—	150	—	200	ns
Address access time	t <sub>AA</sub>	—	50	—	60	—	75	—	100	ns
Output enable access time	t <sub>OEA</sub>	—	40	—	50	—	60	—	75	ns
Chip disable to output in high Z	t <sub>CHZ</sub>	—	25	—	25	—	30	—	35	ns
Chip enable to output in low Z	t <sub>CLZ</sub>	30	—	30	—	35	—	40	—	ns
Output enable to output in low Z	t <sub>OLZ</sub>	10	—	10	—	10	—	10	—	ns
Output disable to output in high Z	t <sub>OHZ</sub>	—	25	—	25	—	30	—	35	ns
Chip enable pulse width	t <sub>CE</sub>	100 ns 4 ms		120 ns 4 ms		150 ns 4 ms		200 ns 4 ms		
Chip enable precharge time	t <sub>p</sub>	50	—	60	—	75	—	100	—	ns
Address set-up time	t <sub>AS</sub>	0	—	0	—	0	—	0	—	ns
Row address hold time	t <sub>RAH</sub>	20	—	20	—	25	—	30	—	ns
Column address hold time	t <sub>CAH</sub>	100	—	120	—	150	—	200	—	ns
Read command set-up time	t <sub>RCS</sub>	0	—	0	—	0	—	0	—	ns
Read command hold time	t <sub>RCH</sub>	0	—	0	—	0	—	0	—	ns
Output enable hold time	t <sub>OHC</sub>	0	—	0	—	0	—	0	—	ns
Output enable to chip enable delay time	t <sub>OCD</sub>	0	—	0	—	0	—	0	—	ns
Output hold time from column address	t <sub>OH</sub>	5	—	5	—	5	—	10	—	ns
Write command pulse width	t <sub>WP</sub>	25	—	25	—	30	—	35	—	ns
Chip enable to end of write	t <sub>cw</sub>	100	—	120	—	150	—	200	—	ns

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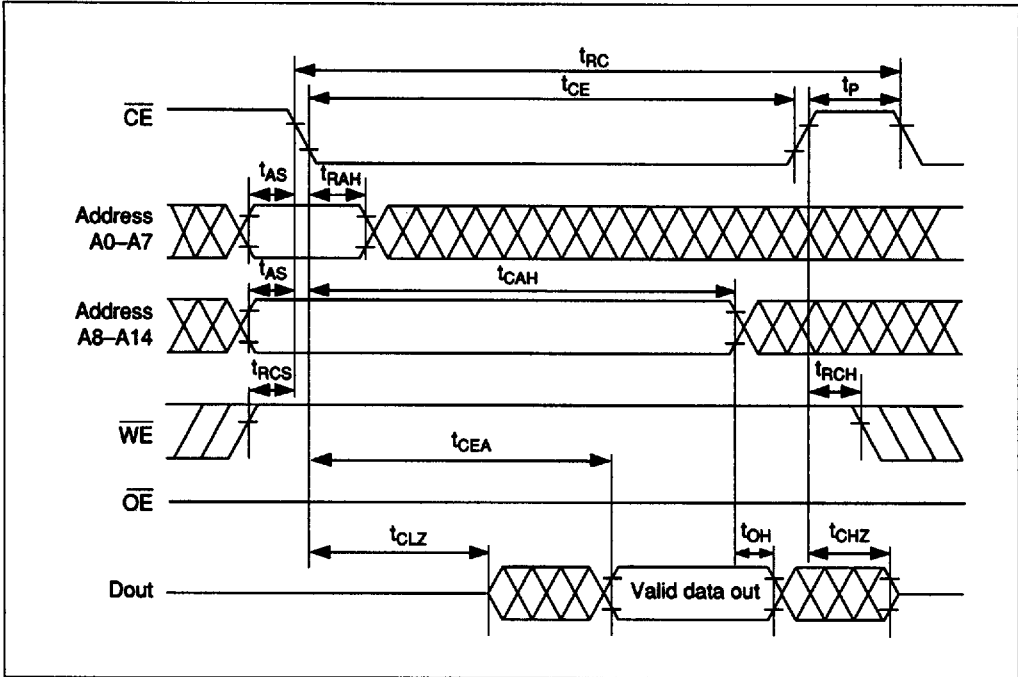
AC Characteristics ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ) (cont)

Parameter	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Column address set-up time	$t_{ASW}$	0	—	0	—	0	—	0	—	ns
Column address hold time after write	$t_{AHW}$	0	—	0	—	0	—	0	—	ns
Data valid to end of write	$t_{DW}$	20	—	20	—	25	—	30	—	ns
Data in hold time for write	$t_{DH}$	0	—	0	—	0	—	0	—	ns
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	5	—	ns
Write to output in high Z	$t_{WHZ}$	—	25	—	25	—	30	—	35	ns
Transition time (rise and fall)	$t_T$	3	50	3	50	3	50	3	50	ns
Refresh command delay time	$t_{RFD}$	50	—	60	—	75	—	100	—	ns
Refresh precharge time	$t_{FP}$	30	—	30	—	30	—	30	—	ns
Refresh command pulse width for automatic refresh	$t_{FAP}$	80	10000	80	10000	80	10000	80	10000	ns
Automatic refresh cycle time	$t_{FC}$	160	—	190	—	235	—	310	—	ns
Refresh command pulse width for self refresh	$t_{FAS}$	10000	—	10000	—	10000	—	10000	—	ns
Refresh reset time for self refresh	$t_{FRS}$	160	—	190	—	235	—	310	—	ns
Refresh period	$t_{REF}$	—	4	—	4	—	4	—	4	ns

- Notes:
1.  $t_{CHZ}$ ,  $t_{OHZ}$ , and  $t_{WHZ}$  are defined as the time at which the output achieves the open circuit conditions.
  2.  $t_{CLZ}$ ,  $t_{OLZ}$  and  $t_{OW}$  are sampled under the condition of  $t_T = 5$  ns, and not 100% tested.
  3. A write occurs during the overlap of a low  $\overline{CE}$  and low  $\overline{WE}$ .
  4. If  $\overline{CE}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high impedance state.
  5. If input signals of opposite phase to the outputs are applied in a write cycle,  $\overline{OE}$  or  $\overline{WE}$  must disable output buffers prior to applying data to the device and data inputs must be floating prior to  $\overline{OE}$  or  $\overline{WE}$  turning on output buffers.
  6.  $V_{IH}$  (min.) and  $V_{IL}$  (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  7. An initial pause of 100  $\mu\text{s}$  is required after power-up followed by a minimum of 8 initialization cycles.
  8. At the end of self refresh, refresh reset time ( $t_{FRS}$ ) is required to reset the internal self refresh operation of the RAM. During  $t_{FRS}$ ,  $\overline{CE}$  and  $\overline{OE}$  must be kept high. If auto refresh follows self refresh, low transition of  $\overline{OE}$  at the beginning of auto refresh must not occur during  $t_{FRS}$  period.

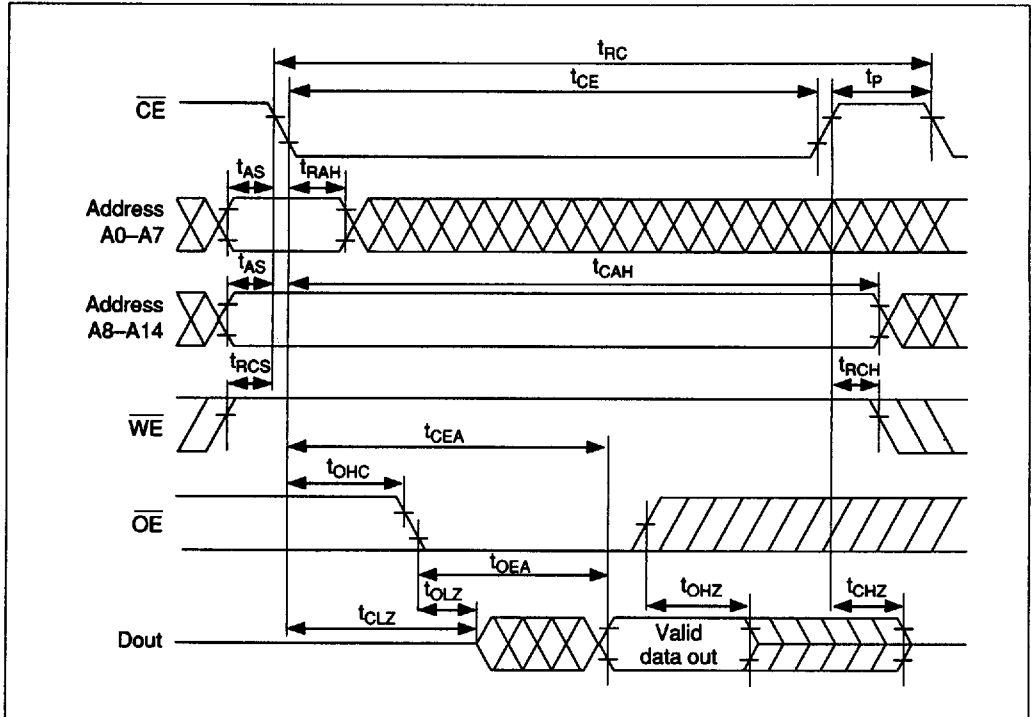
Timing Waveforms

Read Cycle (1) ( $\overline{CE}$  controlled)



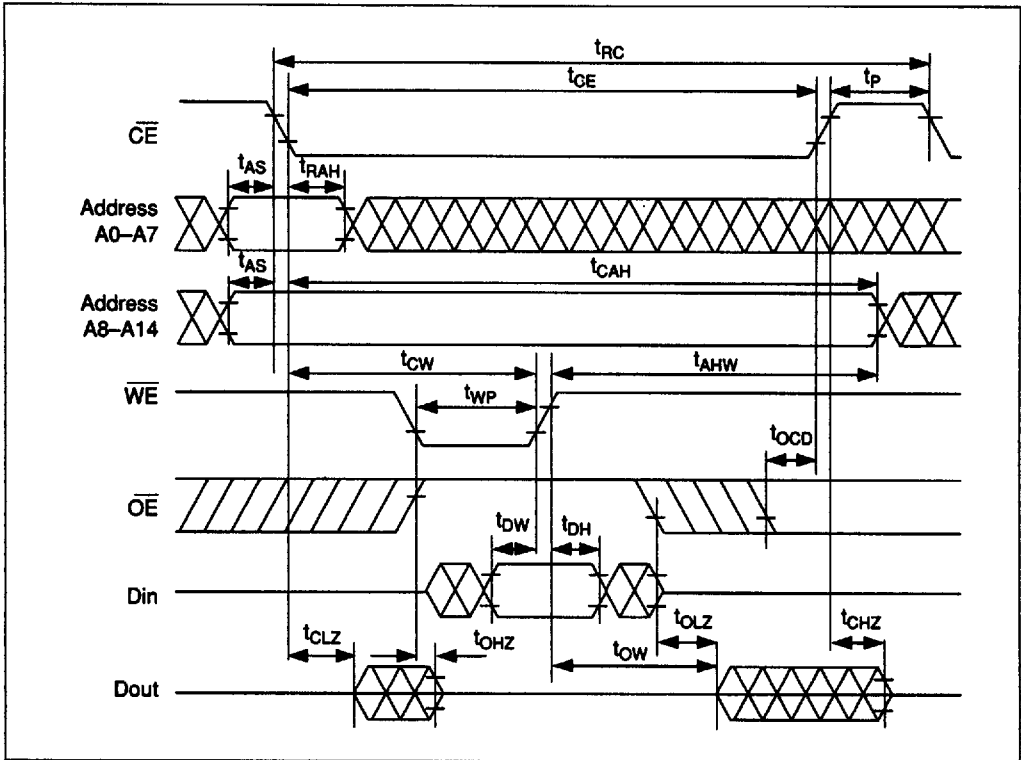
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## Read Cycle (2) ( $\overline{OE}$ controlled)



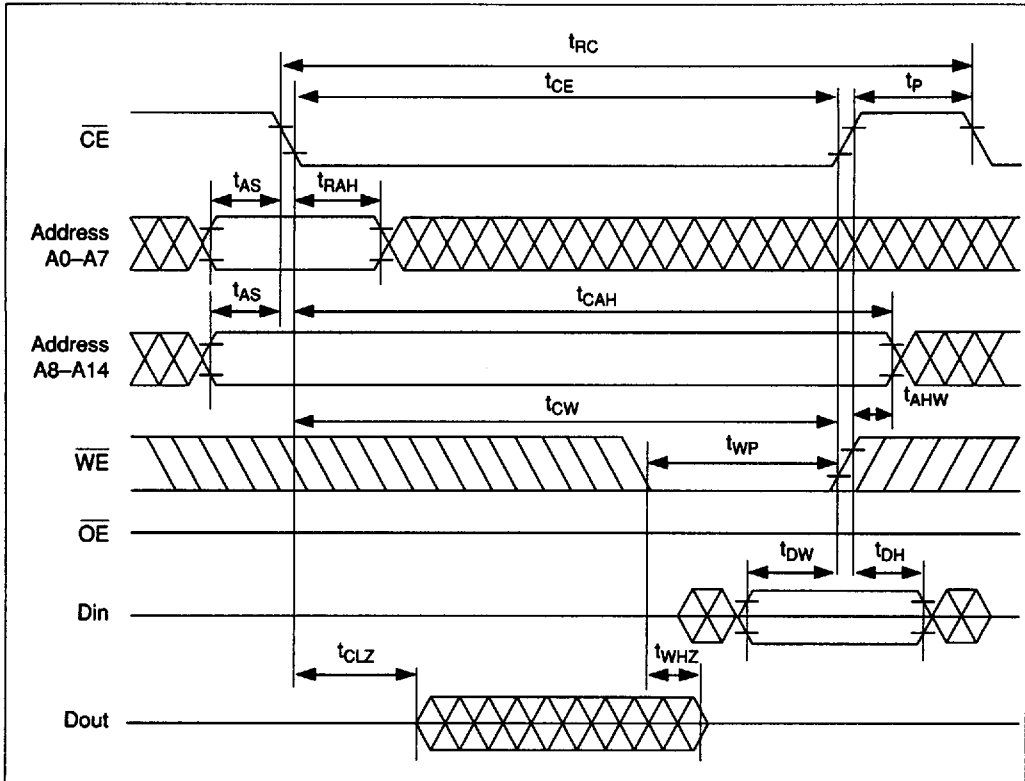


Write Cycle (1) ( $\overline{OE}$  Clock)

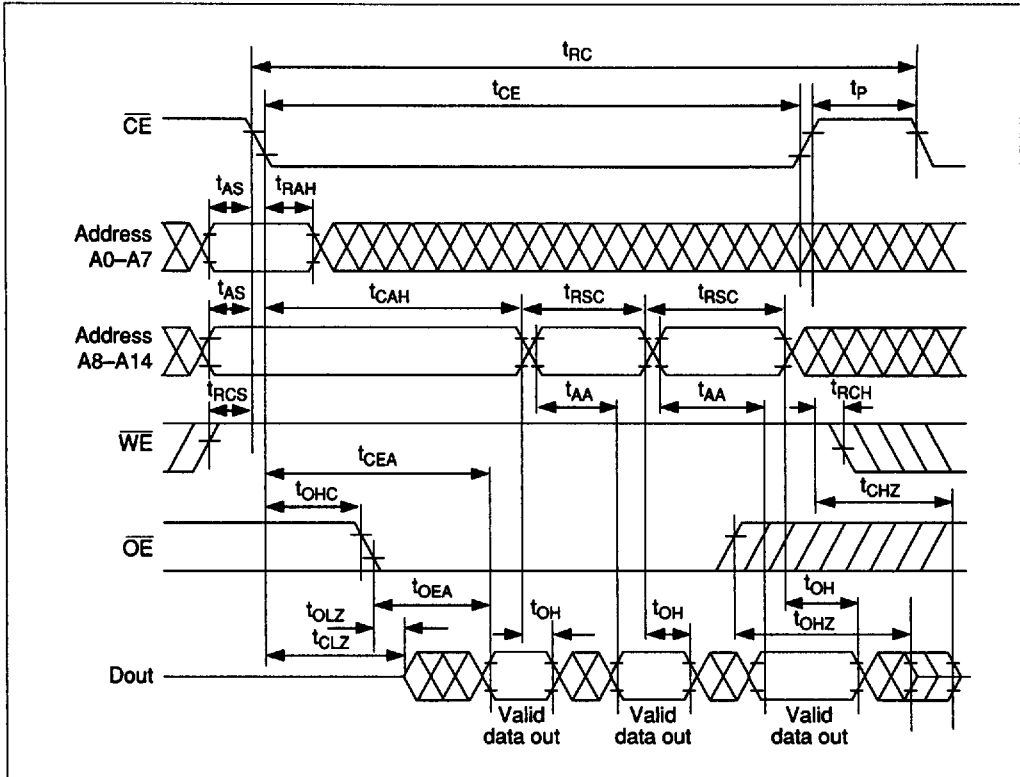


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## Write Cycle (2) (OE fixed low)

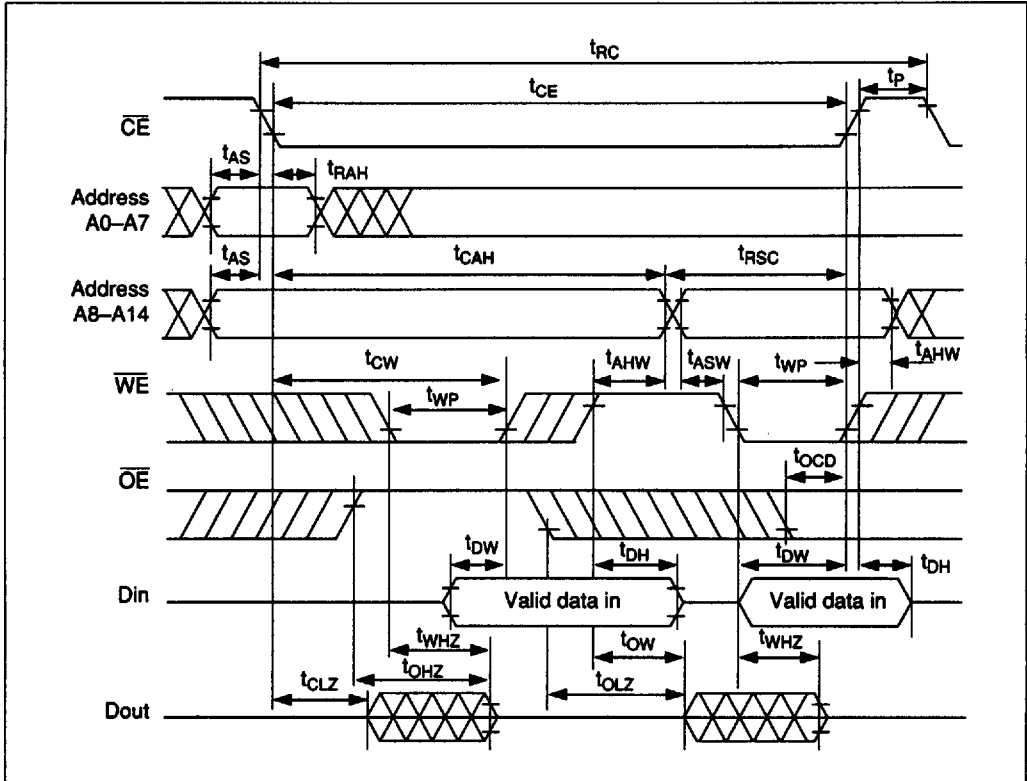


Static Column Mode Read Cycle

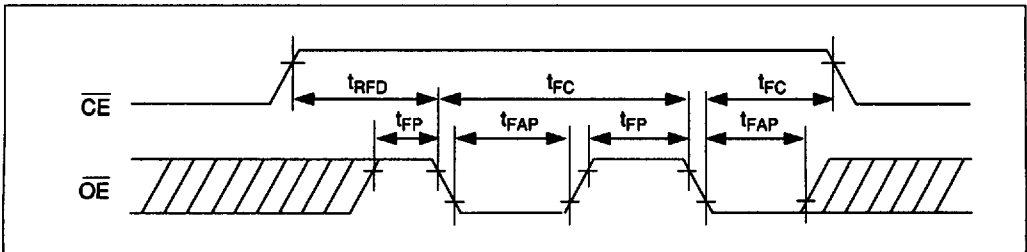


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## Static Column Mode Write Cycle



## Automatic Refresh Cycle



## Self Refresh Cycle

