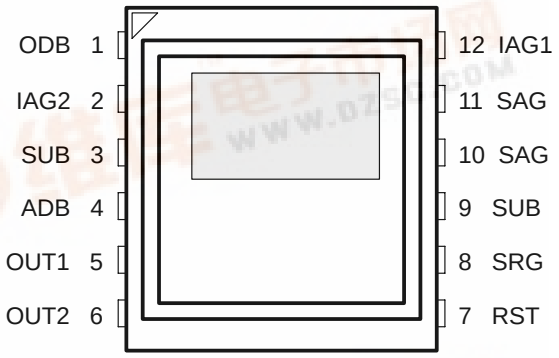
TC237B
680- × 500-PIXEL CCD IMAGE SENSOR

SOCS063 – APRIL 2001

- **High Resolution, 1/3-in Solid-State Image Sensor for NTSC Black and White Applications**
- **340,000 Pixels per Field**
- **Frame Memory**
- **658 (H) × 496 (V) Active Elements in Image Sensing Area Compatible With Electronic Centering**
- **Multimode Readout Capability**
  - **Progressive Scan**
  - **Interlaced Scan**
  - **Dual-Line Readout**
  - **Image Area Line Summing**
  - **Smear Subtraction**
- **Fast Single-Pulse Clear Capability**
- **Continuous Electronic Exposure Control From 1/60 – 1/50,000 s**
- **7.4-μm Square Pixels**
- **Advanced Lateral Overflow Drain Antiblooming**
- **Low Dark Current**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



- **High Photoresponse Uniformity**
- **High Dynamic Range**
- **High Sensitivity**
- **High Blue Response**
- **Solid-State Reliability With No Image Burn-In, Residual Imaging, Image Distortion, Image Lag, or Microphonics**

description

The TC237B is a frame-transfer, charge-coupled device (CCD) image sensor designed for use in single-chip black and white National Television Standards Committee (NTSC) TV, computer, and special-purpose applications that require low cost and small size.

The image-sensing area of the TC237B device is configured into 500 lines with 680 elements in each line. Twenty-two elements are provided in each line for dark reference. The antiblooming feature of the sensor is based on an advanced lateral overflow drain concept. The sensor can be operated in a true interlace mode as a 658(H) × 496(V) sensor with a low dark current. An important feature of the TC237B high-resolution sensor is the ability to capture a full 340,000 pixels per field. The image sensor also provides high-speed image transfer capability and a continuous electronic exposure control without the loss of sensitivity and resolution inherent in other technologies. Charge voltage is converted to signal voltage at 13 μV per electron by a high-performance structure with a reset and a voltage-reference generator. The signal is further buffered by a low-noise, two-stage, source-follower amplifier to provide high-output drive capability.

The TC237B sensor is built using TI-proprietary advanced virtual-phase (AVP) technology, which provides devices with high blue response, low dark current, high photoresponse uniformity, and single-phase clocking. The TC237B sensor is characterized for operation from –10°C to 45°C.

This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to V_{SS}. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to V_{SS} during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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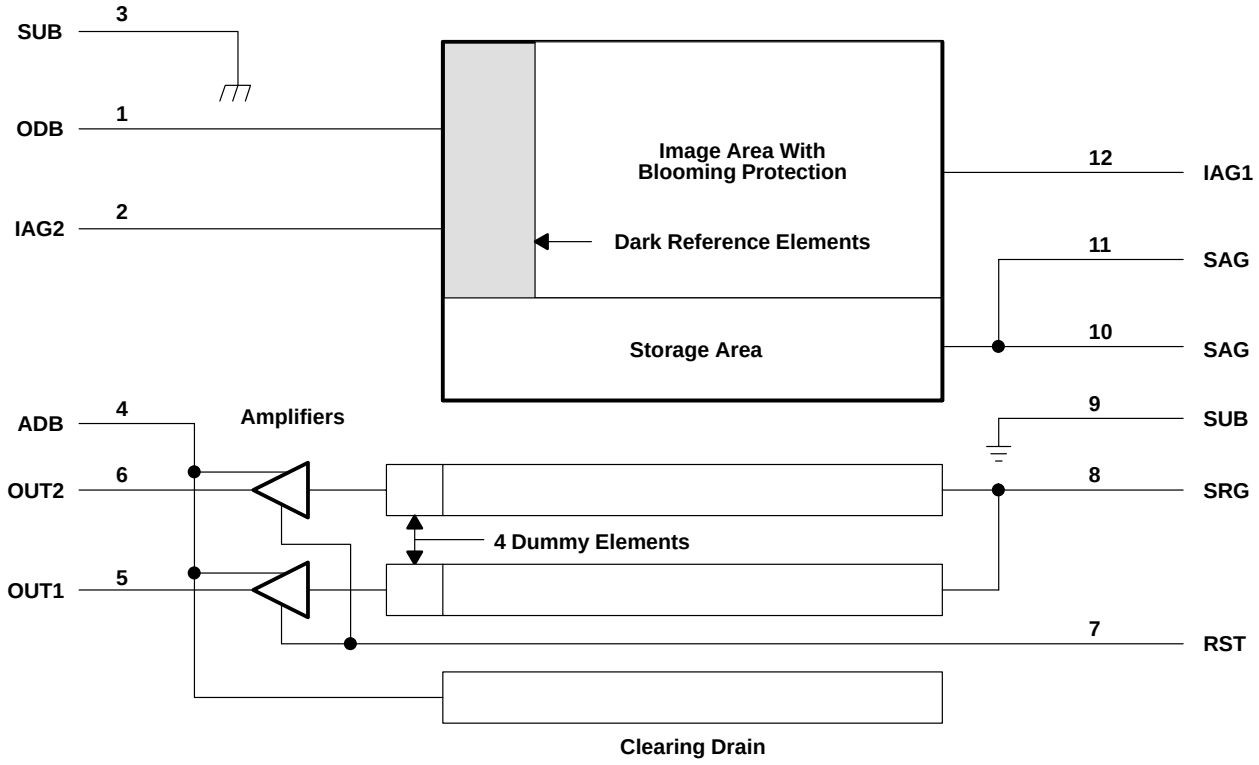
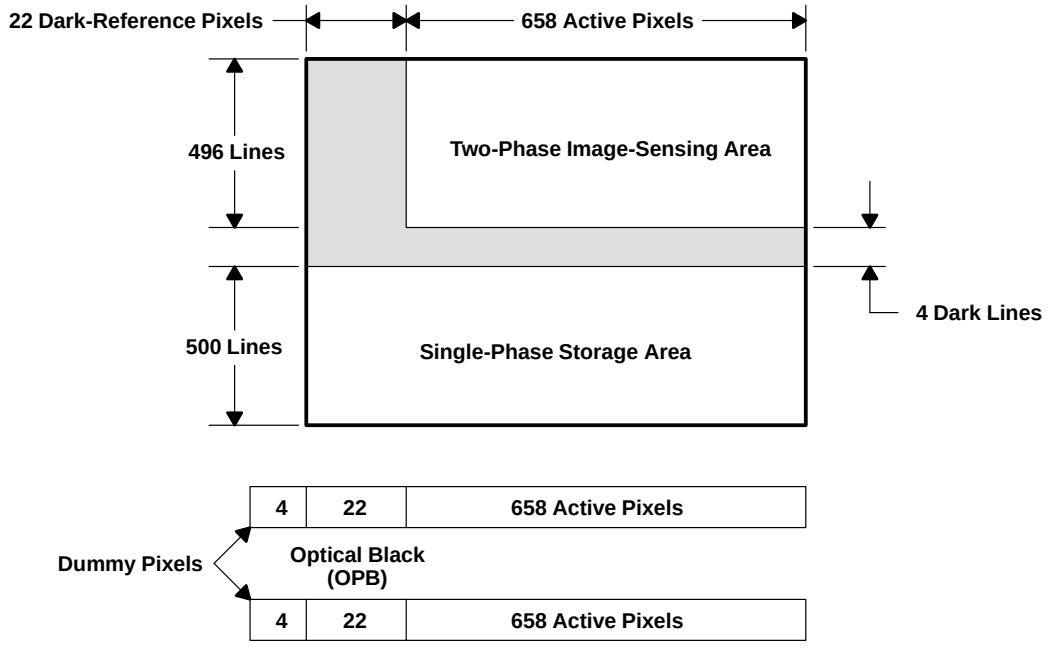
functional block diagram



sensor topology diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADB	4	I	Supply voltage for amplifier drain bias
IAG1	12	I	Image area gate 1
IAG2	2	I	Image area gate 2
ODB	1	I	Supply voltage for drain antiblooming bias
OUT1	5	O	Output signal 1
OUT2	6	O	Output signal 2
RST	7	I	Reset gate
SAG	10, 11	I	Storage area gate
SRG	8	I	Serial register gate
SUB	3, 9		Substrate

detailed description

The TC237B CCD image sensor consists of four basic functional blocks: the image-sensing area, the image storage area, the serial register gates, and the low-noise signal processing amplifier block with charge detection nodes and independent resets. The location of each of these blocks is identified in the functional block diagram.

image-sensing and image storage areas

Figure 1 and Figure 2 show cross sections with potential well diagrams and top views of the image-sensing and storage area elements. As light enters the silicon in the image-sensing area, electrons are generated and collected in the wells of the sensing elements. Blooming protection is provided by applying a dc bias to the overflow drain bias pin. To clear the image before beginning a new integration time (for implementation of electronic fixed shutter or electronic auto-iris), apply a pulse of at least 1 μs to the overflow drain bias. After integration is complete, charge voltage is transferred into the storage area. The transfer timing depends on whether the readout mode is interlace or progressive scan. If the progressive-scan readout mode is selected, the readout may be performed by using one serial register or at high speed by using both serial registers (see Figure 3 through Figure 5). A line-summing operation, which is useful in off-chip smear subtraction, can be implemented before the parallel transfer (see Figure 6).

Twenty-two columns at the left edge of the image-sensing area are shielded from incident light; these elements provide the dark reference used in subsequent video-processing circuits to restore the video black level. In addition, four dark lines between the image-sensing and the image storage area prevent charge leakage from the image-sensing area into the image storage area.

advanced lateral overflow drain

The advanced lateral overflow drain structure is shared by two neighboring pixels and provides several unique features in the sensor. By varying the dc bias of the drain pin, you can control the blooming protection level and trade it for the well capacity.

To clear charge voltages in the image area, apply a 10-V pulse for a minimum duration of 1 μs above the nominal dc bias level. This feature permits a precise control of the integration time on a frame-by-frame basis. The single-pulse clear capability also reduces smear by eliminating accumulated charge from the pixels before the start of the integration (single-sided smear).

Application of a negative 1-V pulse to the ODB signal during the parallel transfer is recommended to prevent slight column-to-column pixel well capacity variations in some artifacts.

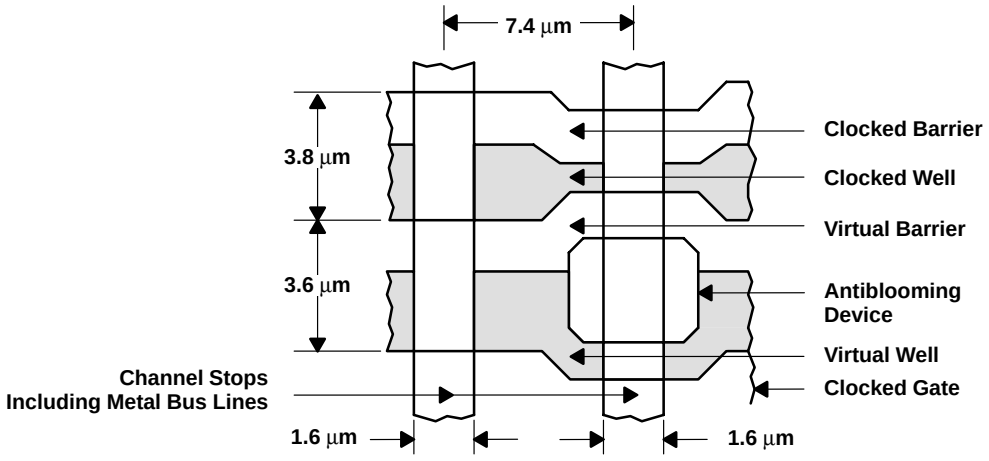


Figure 1. Image-Area Pixel Structure

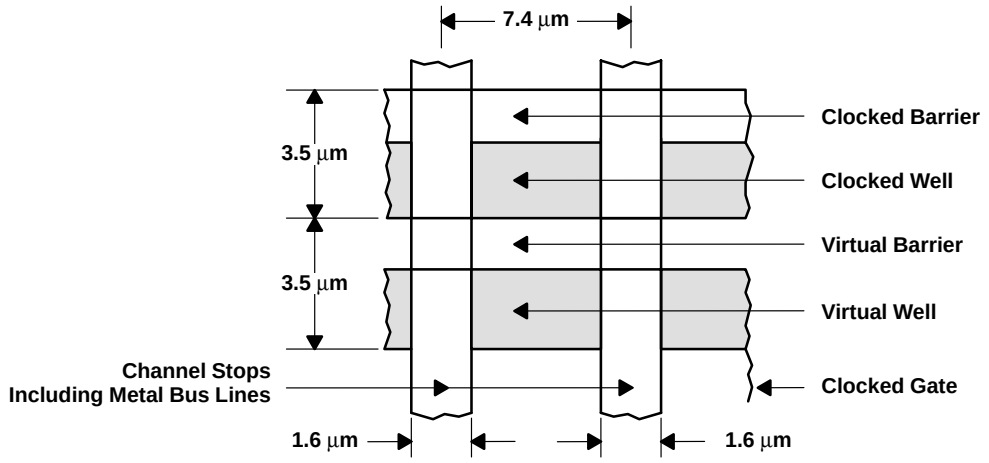


Figure 2. Storage-Area Pixel Structure

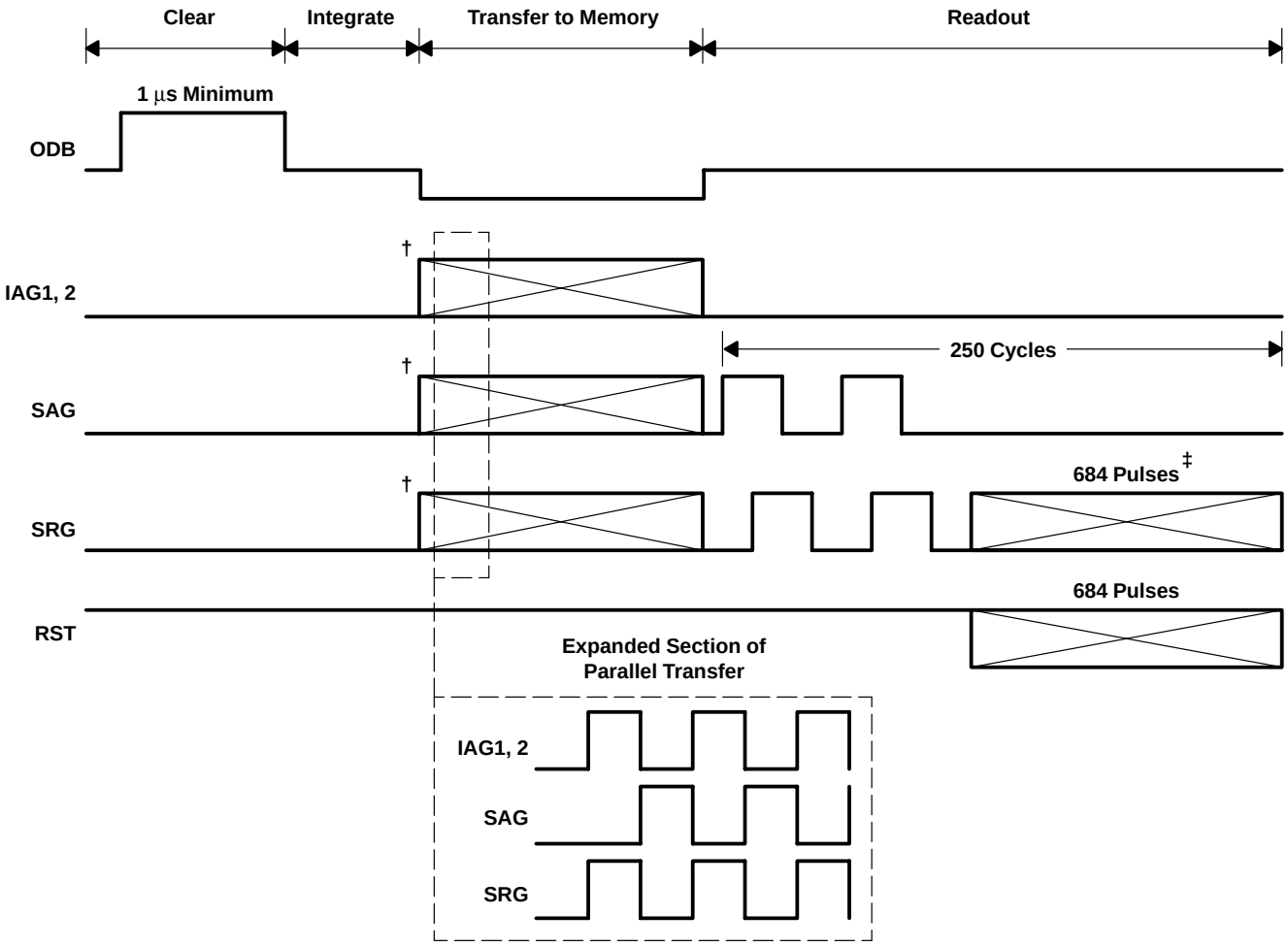
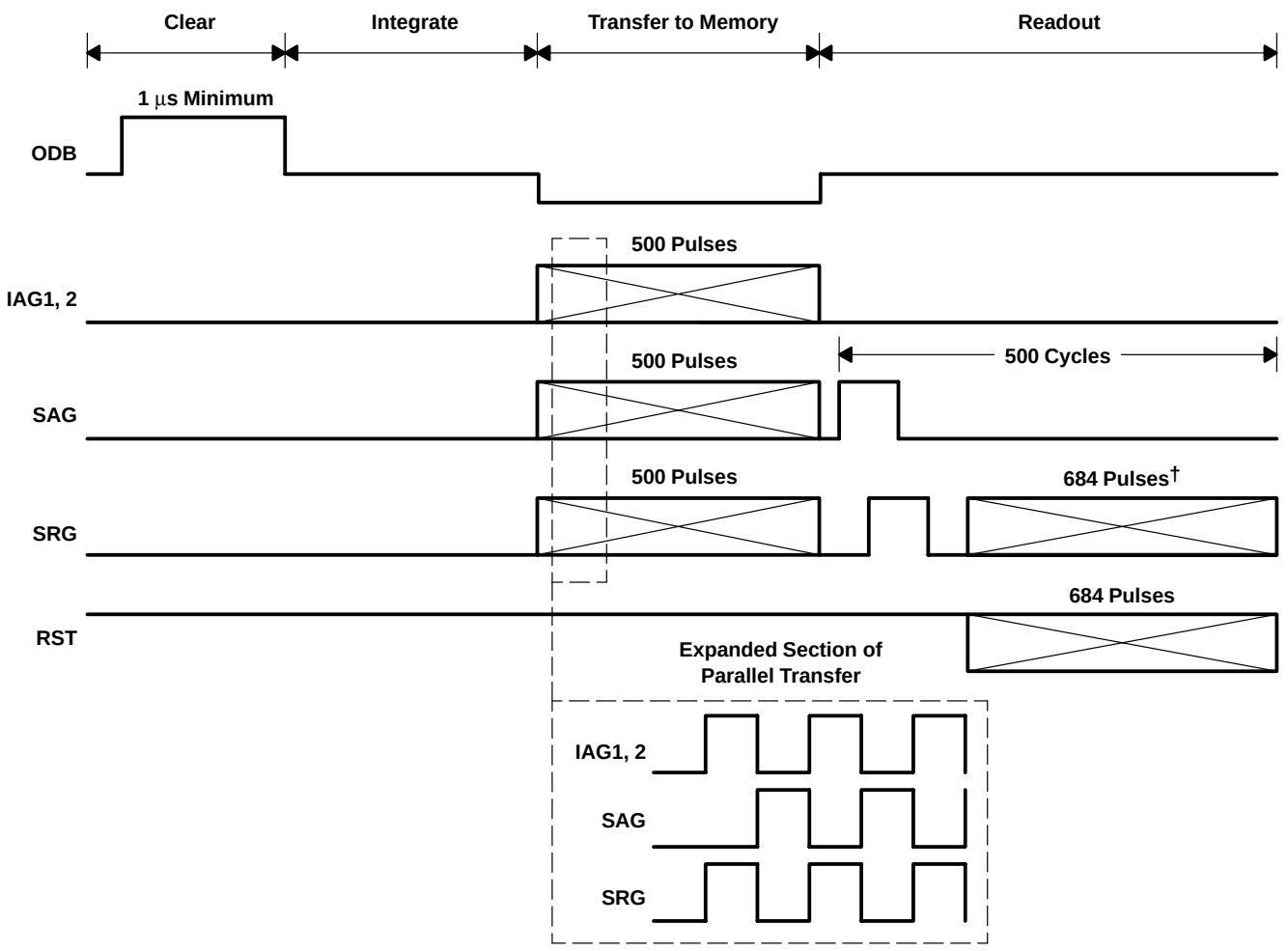


Figure 3. Interlace Timing

† The number of parallel-transfer pulses is field dependent. Field 1 has 500 pulses of IAG1, IAG2, SAG, and SRG with appropriate phasing. Field 2 has 501 pulses.
‡ The readout is from register 2.



† The readout is from register 2.

Figure 4. Progressive-Scan Timing With Single Register Readout

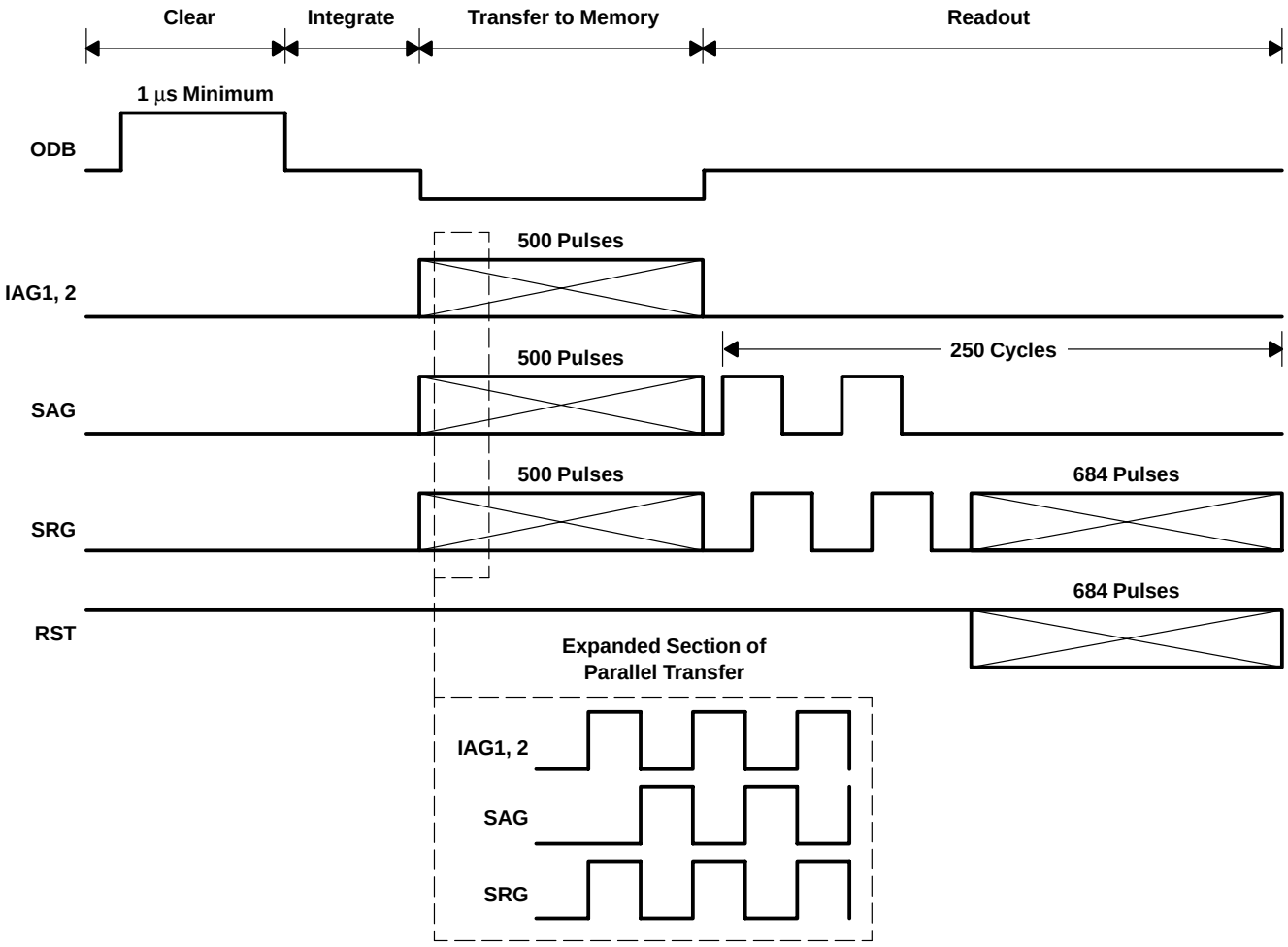


Figure 5. Progressive-Scan Timing With Dual-Register Readout

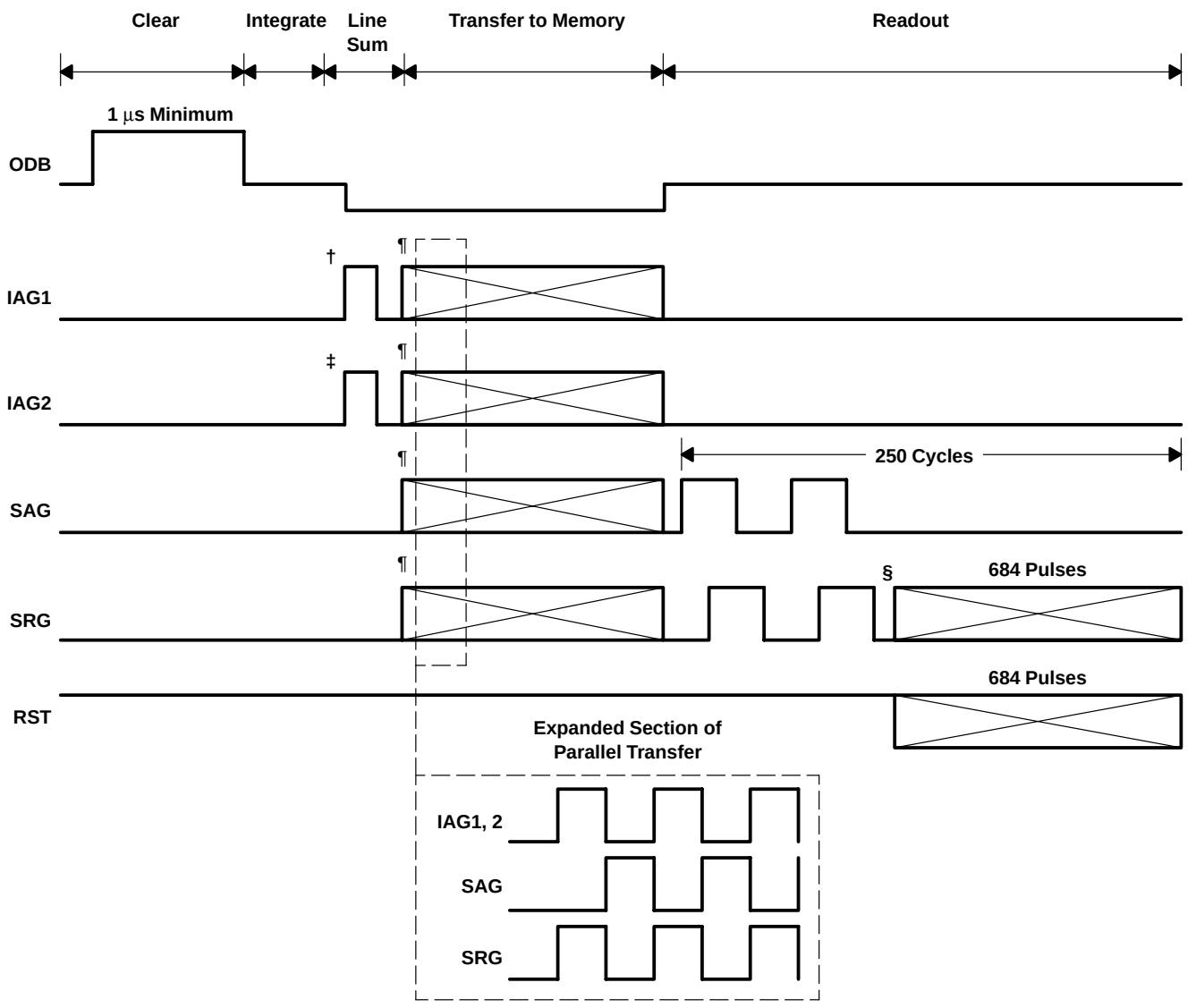


Figure 6. Line-Summing Timing

† This pulse occurs only during field 1.
‡ This pulse occurs only during field 2.
§ While readout is from register 2, register 1 can be read out for off-chip smear subtraction.
¶ The number of parallel transfer pulses if field dependent. Field 1 has 500 pulses, and field 2 has 501 pulses.

serial registers

The storage area gate and serial gate(s) are used to transfer charge line-by-line from the storage area into the serial register(s). Depending on the readout mode, one or both serial registers are used. If both are used, the registers are read out in parallel.

readout and video processing

After transfer into the serial register(s), the pixels are clocked out and sensed by a charge detection node. The node must be reset to a reference level before the next pixel is placed onto it. The timing for the serial-register readout, which includes the external pixel clamp and sample-and-hold signals needed to implement correlated double sampling, is shown in Figure 7. As charge is transferred onto the detection node, the potential of the node changes in proportion to the amount of the charge received. The change is sensed by an MOS transistor; after proper buffering, the signal is supplied to the output terminal of the image sensor. Figure 8 shows the circuit diagram of the charge detection node and output amplifier. The detection nodes and amplifiers are placed a short distance from the edge of the storage area; therefore, each serial register contains 4 dummy elements that are used to span the distance between the serial registers and the amplifiers.

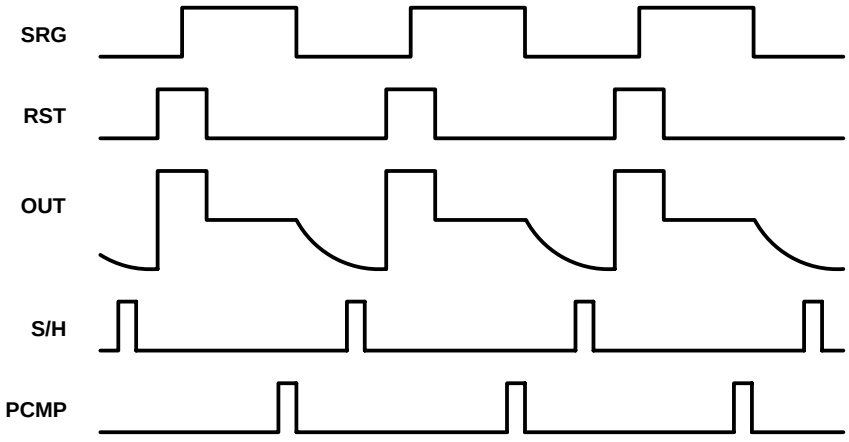


Figure 7. Serial Readout and Video-Processing Timing

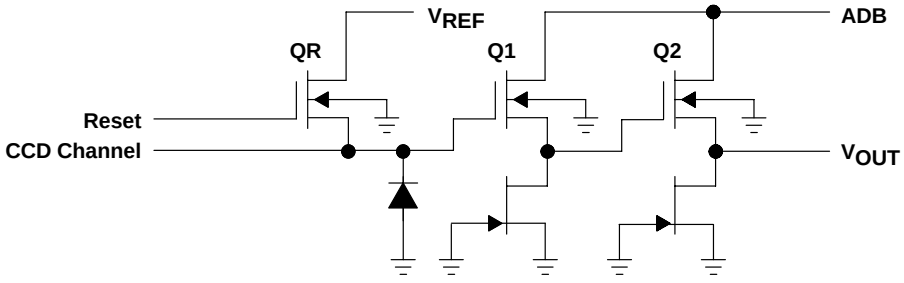


Figure 8. Output Amplifier and Charge Detection Node

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, ADB (see Note 1) . . . . . SUB to SUB + 15 V
Supply voltage range, ODB . . . . . SUB to SUB + 21 V
Input voltage range, V_I: IAG1, IAG2, SAG, SRG . . . . . 0 V to 15 V
Operating free-air temperature range, T_A . . . . . –10°C to 45°C
Storage temperature range, T_{stg} . . . . . –30°C to 85°C
Operating case temperature range, T_C . . . . . –10°C to 55°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to SUB.

recommended operating conditions

				MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	ADB			21	22	23	V
	ODB	For antiblooming control		15.5	16	16.5	
		For clearing		25.5	26	26.5	
		For transfer		14.5	15	15.5	
Substrate bias voltage					10		V
Input voltage, V_I		IAG1, IAG2	High level	11.5	12	12.5	V
			Low level		0		
		SAG	High level	11.5	12	12.5	
			Low level		0		
		SRG, RST	High level	11.5	12	12.5	
			Low level		0		
Clock frequency, f_{clock}		IAG1, IAG2			12.5		MHz
		SAG			12.5		
		SRG, RST			12.5		
Load capacitance		OUT1, OUT2				6	pF
Operating free-air temperature, T_A				–10		45	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 2)	With CDS‡§		64		dB
	Without CDS‡§		58	59	
Charge conversion factor			13		μV/e
Charge transfer efficiency (see Note 3)		0.9999	0.99995	1	
Signal response delay time, τ (see Note 4)			12.5		ns
Gamma (see Note 5)				1	
Output resistance		300	400	500	Ω
Amplifier noise equivalent signal	With CDS‡	15	18	21	electrons
	Without CDS‡	30	36	42	
Rejection ratio	ADB (see Note 6)		20		dB
	SRG (see Note 7)		45		
	ODB (see Note 8)		25		
Supply current			5	10	mA
Input capacitance, C_i	IAG1, IAG2		2000		pF
	SRG		70		
	RST		10		
	SAG		4000		

† All typical values are at T_A = 25°C.
‡ CDS = Correlated double sampling, a signal-processing technique that improves noise performance by subtraction of reset noise.
§ Performance depends on the particular implementation of the CDS technique and on the selected filter bandwidth that precedes sampling.

NOTES:
2. Dynamic range is –20 times the logarithm of the mean-noise signal divided by the saturation output signal.
3. Charge transfer efficiency is one minus the charge loss per transfer in the output register. The test is performed in the dark using an electrical input signal.
4. Signal response delay time is the time between the falling edge of the SRG pulse and the output signal valid state.
5. Gamma (γ) is the value of the exponent in the equation below for two points on the linear portion of the transfer function curve (this value represents points near saturation).

$$\left(\frac{\text{Exposure (2)}}{\text{Exposure (1)}}\right)^{\gamma} = \left(\frac{\text{Output signal (2)}}{\text{Output signal (1)}}\right)$$

6. ADB rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at ADB.
7. SRG rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at SRG.
8. ODB rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at ODB.

optical characteristics, T_A = 40°C (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Sensitivity (see Note 9)	No IR filter			256		mV/lux
	With IR filter			32		
Saturation signal, V_{sat} (see Note 10)	Antiblooming disabled	T_A =45°C	320			mV
Maximum usable signal, V_{use}	Antiblooming enabled	T_A =45°C	120			mV
Blooming overload ratio (see Note 11)			500			
Image area well capacity			22K	30K	38K	electrons
Smear (see Note 12)		See Note 13			–78	dB
Dark current		T_A = 21°C			0.05	nA/cm^2
Dark signal		T_A = 45°C			1	mV
Dark-signal uniformity		T_A = 45°C			0.5	mV
Dark-signal shading		T_A = 45°C			0.5	mV
Spurious nonuniformity	Dark	T_A = 45°C			10	mV
	Illuminated, F#8	T_A = 45°C			15	%
Column uniformity					0.5	mV
Electronic shutter capability			1/50,000	1/60		s

NOTES: 9. Theoretical value
10. Saturation is the condition in which further increase in exposure does not lead to further increase in output signal.
11. Blooming is the condition in which charge is induced in an element by light incident on another element. Blooming-overload ratio is the ratio of blooming exposure to saturation exposure.
12. Smear is a measure of the error introduced by transferring charge through an illuminated pixel in shutterless operation. It is equivalent to the ratio of the single-pixel transfer time to the exposure time using an illuminated section that is 1/10 of the image-area vertical height with recommended clock frequencies.
13. The exposure time is 16.67 ms, the fast-dump clocking rate during vertical transfer is 12.5 MHz, and the illuminated section is 1/10 the height of the image section.

TYPICAL CHARACTERISTICS

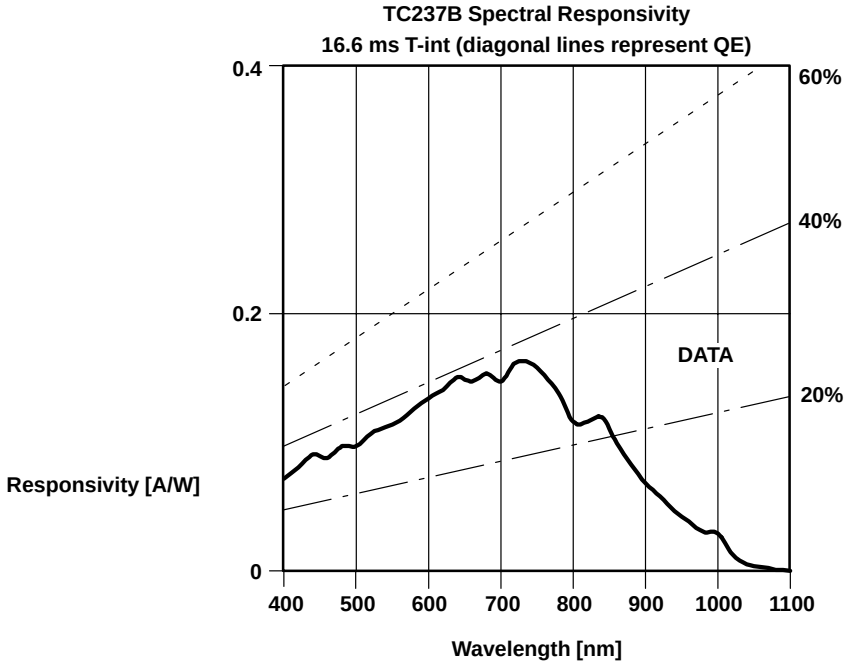
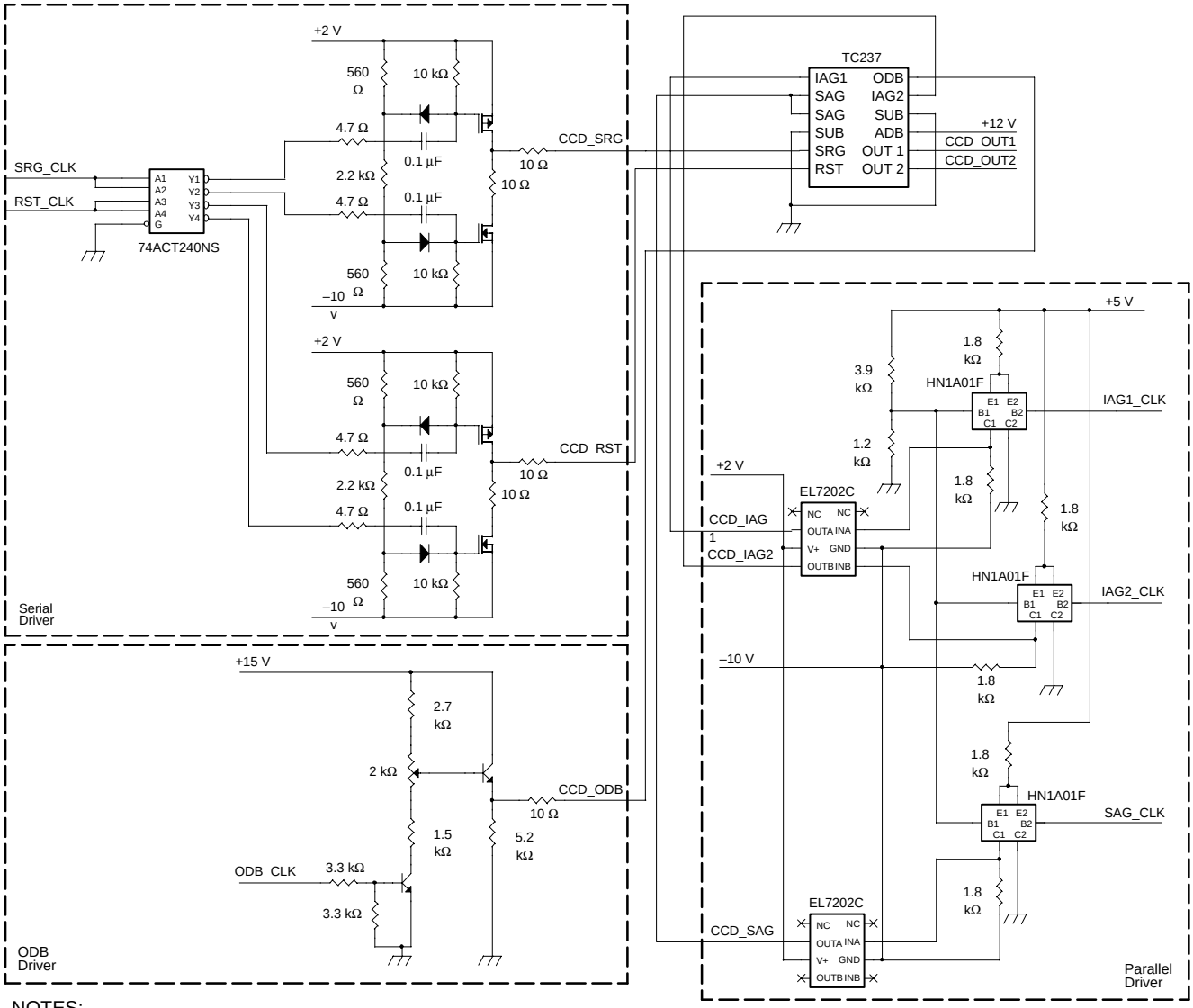


Figure 9. Spectral Characteristics of the TC237B CCD Sensor

APPLICATION INFORMATION



NOTES: A. Support circuits

DEVICE	APPLICATION	FUNCTION
EL7202C	Parallel driver	Driver for IAG1, IAG2,SAG
74ACT240NS	Serial pre-driver	Driver for SRG, RST

B. Clock, DC voltages

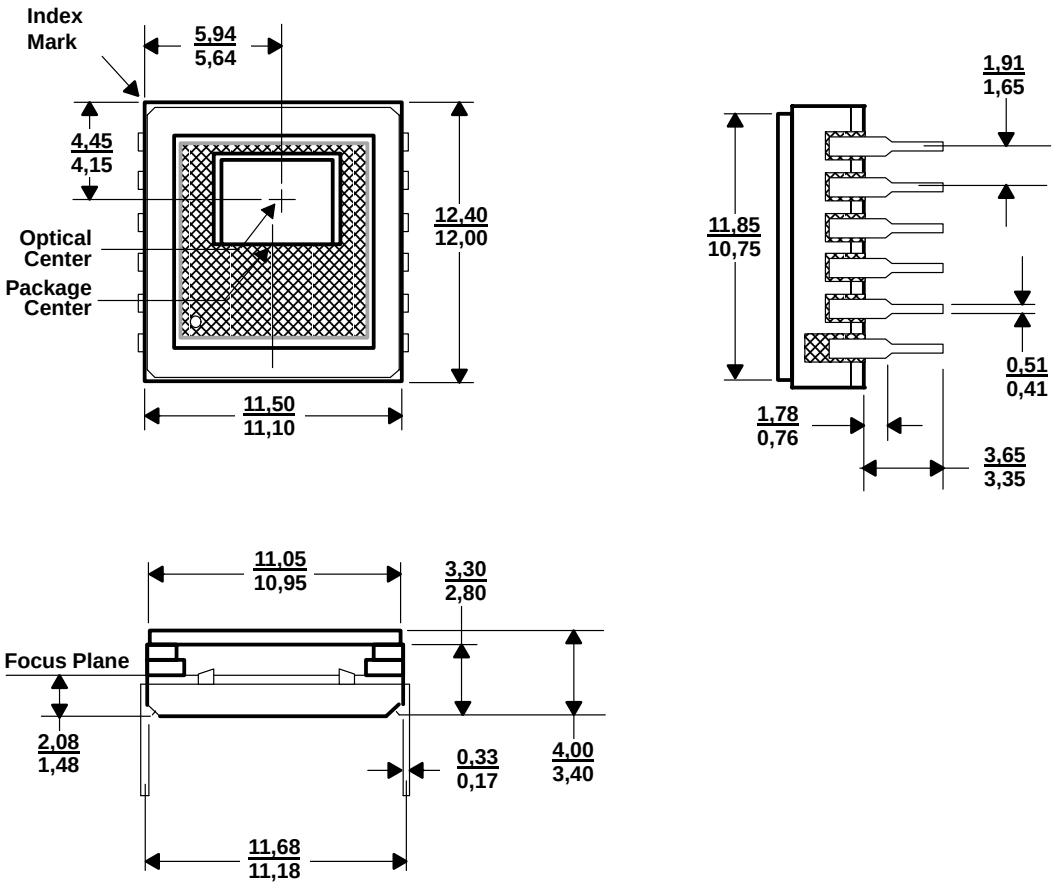
Clock	SRG_CLK, RST_CLK, ODB_CLK, IAG1_CLK, IAG2_CLK, SAG_CLK	TTL level
DC	+15 V, +12 V, +5 V, +2 V, 0 V, (Ground), –10 V	

Figure 10. Typical Application Circuit Diagram

MECHANICAL DATA

The package for the TC237B consists of a ceramic base, a glass window, and a 12-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual-in-line organization and fit into mounting holes with 1,78 mm center-to-center spacings.

TC237 (12 pin)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

11/00

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