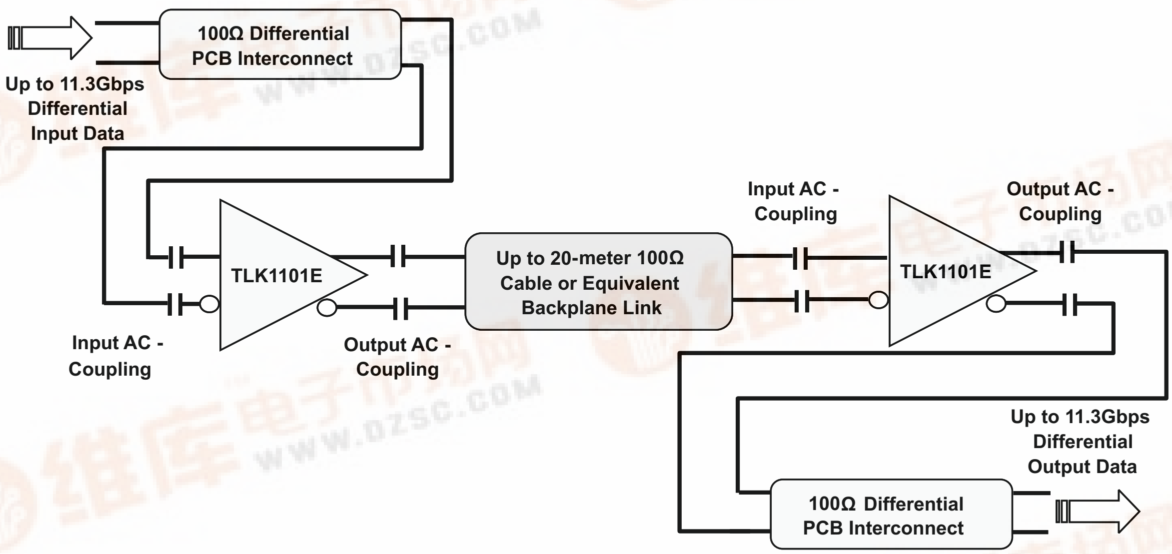
11.3-Gbps Cable and PC Board Equalizer

FEATURES

- Multi-Rate Operation up to 11.3Gbps
- Compensates for up to 30dB Loss on the Receive Side and up to 7dB Loss on the Transmit Side at 5.65GHz
- Input Offset Cancellation
- Output Disable/Squelch Function
- Loss Of Signal Detection
- Adjustable Output Swing
- Adjustable Output De-Emphasis
- Two-Wire Serial Interface
- Single 3.3V Supply
- Surface Mount Small Footprint 4-mm × 4-mm 20-Pin QFN Package

APPLICATIONS

- High-Speed Links In Communication And Data Systems
- SFP+ and XFP Active Cables
- Backplane, Daughtercard, and Cable Interconnects for 10GE, 8GFC, 10GFC, 10G SONET, SAS, SATA



DESCRIPTION

The TLK1101E is a versatile and flexible high-speed equalizer for applications in digital high-speed links with data rates up to 11.3Gbps.

The TLK1101E can be configured in many ways to optimize its performance. It provides output de-emphasis adjustable from 0dB to 7dB using pins DE0 and DE1.

The output differential voltage swing can be set to 300mV$_{p-p}$, 600mV$_{p-p}$, or 900mV$_{p-p}$ using the SWG pin. A controlling voltage on pin VTH can be used to adjust the input threshold voltage.

Pins LN0 and LN1 can be used to optimize the device performance for various interconnect lengths, e.g. from 0 to 20 meters of 24-AWG twinaxial cable.

The LOS (loss of signal) assert level can be set to a desired level through a controlling voltage connected to pin LOSL. The LOS assert levels can be chosen from two LOS assert level ranges selectable with the LOSR pin.

The output can be disabled using the DIS pin. The DIS and the LOS pin can be connected together to implement a squelch function.

The de-emphasis, the output voltage swing, the input threshold voltage, the output disable, and the LOS assert levels and ranges can alternatively be set using the two-wire serial interface through the SCL and SDA pins. The external pin configuration is the default device setup method. The active device control method is selected through register address 0 bit 0 (see Table 4 and Table 20). The two-wire serial interface also allows for the control of the input bandwidth to optimize the device performance for various data rates.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1600mV$_{p\text{-}p}$ differential.

The low-frequency cut-off is low enough to support low-frequency control signals such as SAS and SATA out-of-band (OOB) signals.

BLOCK DIAGRAM

A simplified block diagram of the TLK1101E is shown in Figure 1. This compact, low power, 11.3-Gbps equalizer consists of a high-speed data path with offset cancellation block combined with an analog input threshold selection circuitry, a loss of signal detection block, a two-wire interface with a control-logic block, a bandgap voltage reference, and a bias current generation block.

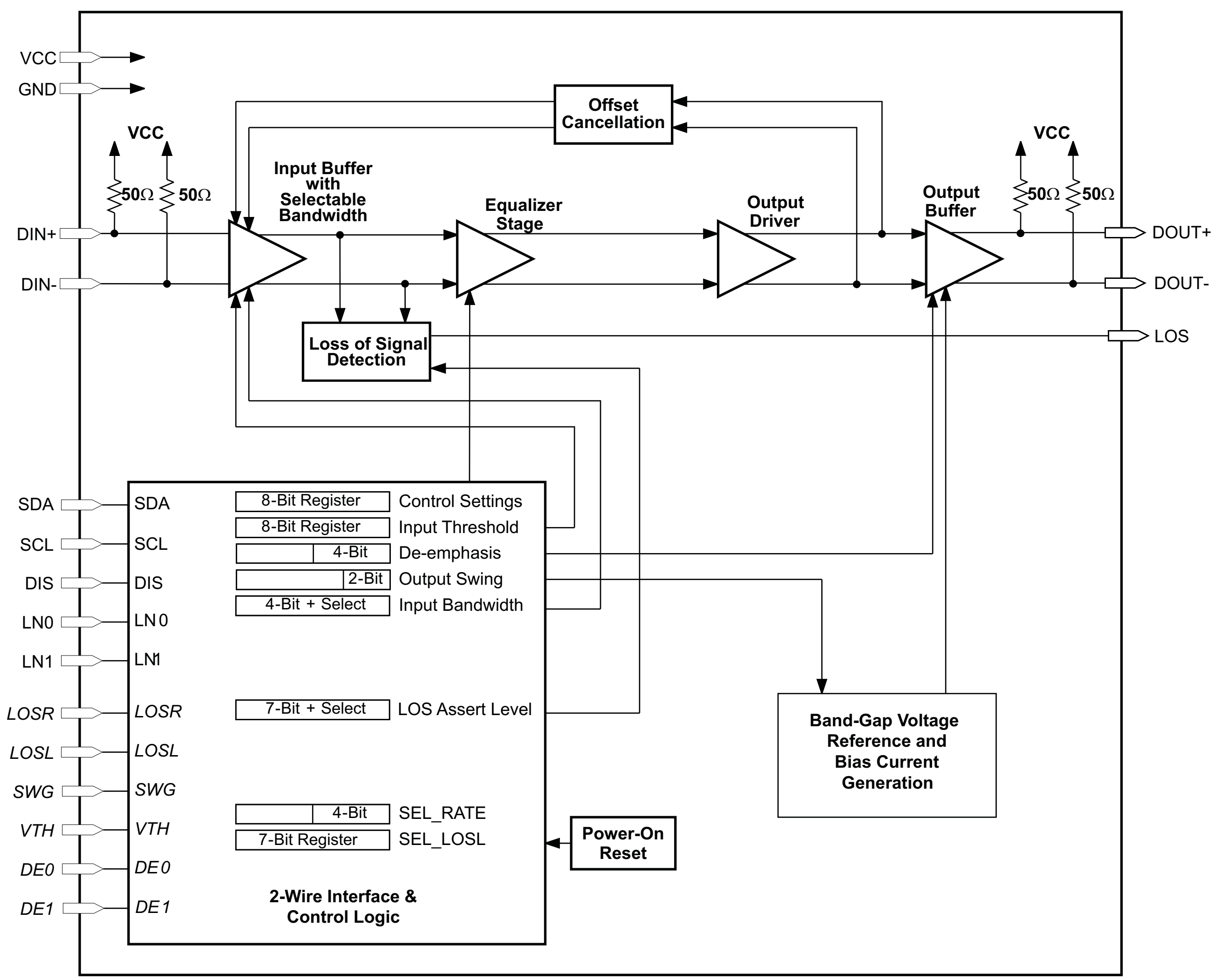


Figure 1. Simplified Block Diagram of the TLK1101E

PACKAGE

For the TLK1101E a small footprint 4-mm × 4-mm 20-pin QFN package is used, with a lead pitch of 0.5mm. The pin-out is shown in Figure 2.

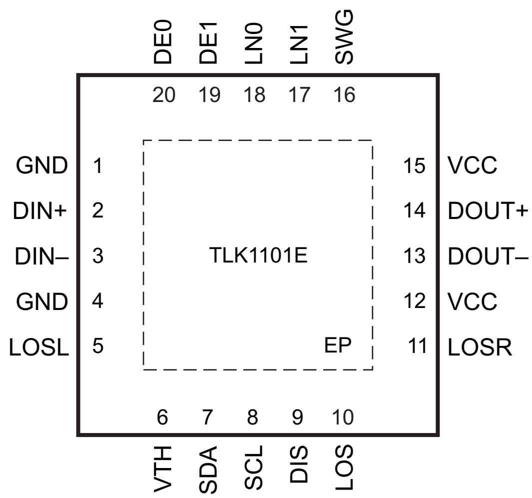


Figure 2. Pin-Out of the TLK1101E in a 4-mm × 4-mm 20-Pin QFN Package

TERMINAL FUNCTIONS

PIN	SYMBOL	TYPE	DESCRIPTION
1, 4	GND	supply	Circuit ground.
2	DIN+	analog-in	Non-inverted data input. On-chip 50Ω terminated to VCC.
3	DIN–	analog-in	Inverted data input. On-chip 50Ω terminated to VCC.
5	LOSL	analog-in	LOS threshold control. A controlling voltage on this pin adjusts the LOS assert and de-assert levels.
6	VTH	analog-in	Input signal threshold control. A controlling voltage of 0V to 1V on this pin adjusts the input signal threshold. Leave open for the default 0V differential threshold.
7	SDA	digital-in/out	Bidirectional serial data pin for the SDA/SCL interface. Open drain. Always connect to a pull-up resistor.
8	SCL	digital-in	Serial clock pin for the SDA/SCL interface. Always connect to a pull-up resistor.
9	DIS	digital-in	Disables CML output stage when set to high level. Internally pulled down.
10	LOS	digital-out	High level indicates that the input signal amplitude is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
11	LOSR	digital-in	LOS range select. Set to high level or leave open for upper range, or set to low level for lower range.
12, 15	VCC	supply	3.3V ± 10% supply voltage.
13	DOUT–	CML-out	Inverted data output. On-chip 50Ω back-terminated to VCC.
14	DOUT+	CML-out	Non-inverted data output. On-chip 50Ω back-terminated to VCC.
16	SWG	three-state	Output voltage swing control. Set to high level for high swing, set to low level for low swing, or leave open for medium swing.
17	LN1	digital-in	Interconnect length select. Supports two logic levels: high and low. (see Table 2)
18	LN0	digital-in	
19	DE1	three-state	Output signal de-emphasis control. Supports three logic levels: high, low, and open. (see Table 1)
20	DE0	three-state	
EP	EP		Exposed die pad (EP) must be grounded.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{CC}	Supply voltage (2)	–0.3 to 4.0	V
V_{DIN+}, $V_{DIN–}$	Voltage at DIN+, DIN– (2)	0.5 to 4.0	V
V_{DIS}, V_{LOSL}, V_{LOSR}, V_{TH}, V_{DE0}, V_{DE1}, V_{LN0}, V_{LN1}, V_{SWG}, V_{SCL}, V_{SDA}	Voltage at DIS, LOSL, LOSR, VTH, DE0, DE1, LN0, LN1, SWG, SCL, SDA (2)	–0.3 to 4.0	V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±2.5	V
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs	–25 to 25	mA
ESD	ESD Rating at all pins	2.5	kV (HBM)
$T_{J,max}$	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.95	3.3	3.6	V
T_A	Operating lead temperature	–40		100	°C
V_{IH}	CMOS Input high voltage	2.0			V
V_{IL}	CMOS Input low voltage			0.8	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.95	3.3	3.6	V
I_{CC}	Supply current	SWG = Open (CML output current included)		76	110	mA
		SWG = High (CML output current included)		83	120	
	LOS High voltage	I_{SOURCE} = 50µA; 10kΩ Pull-up to V_{CC} on LOS pin	2.4			V
	LOS Low voltage	I_{SINK} = 10mA; 10kΩ Pull-up to V_{CC} on LOS pin			0.4	V

AC ELECTRICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency –3dB bandwidth	With 0.1µF input AC-coupling capacitors		30	50	kHz
$V_{IN,MIN}$	Data input sensitivity (1)	BER < 10^{-12} , K28.5 Pattern at 11.3Gbps over a 15-m 24-AWG cable including two SMA connectors, SWG = Open, No de-emphasis, Maximum interconnect length setting. Voltage measured at the input of the cable			250	mV_{p-p}
$V_{IN,MAX}$	Data input overload	BER < 10^{-12} , K28.5 Pattern at 11.3Gbps, K28.5 pattern at 11.3Gbps over a 15-m 24-AWG cable including two SMA connectors, SWG = Open, No de-emphasis, Maximum interconnect length setting. Voltage measured at the input of the cable	1600			mV_{p-p}
	High frequency boost	f = 5.65GHz	20	24		dB
V_{OD}	Differential data output voltage swing	DIS = Low, SWG = Low, V_{IN} = 400mV_{p-p}, No de-emphasis, No interconnect line	225	300	450	mV_{p-p}
		DIS = Low, SWG = Open, V_{IN} = 400mV_{p-p}, No de-emphasis, No interconnect line	450	600	800	
		DIS = Low, SWG = High, V_{IN} = 400mV_{p-p}, No de-emphasis, No interconnect line	600	900	1200	

(1) The given differential input signal swing is valid for the low-frequency components of the input signal. The high frequency components may be attenuated by up to 24dB at 5.65GHz.

AC ELECTRICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CM,OUT}$	Data output common-mode voltage	DIS = Low, SWG = Low, V_{IN} = 400mV_{p-p}, No de-emphasis, No interconnect line	V_{CC}–0.113	V_{CC}–0.075	V_{CC}–0.056	V
		DIS = Low, SWG = Open, V_{IN} = 400mV_{p-p}, No de-emphasis, No interconnect line	V_{CC}–0.2	V_{CC}–0.15	V_{CC}–0.113	
		DIS = Low, SWG = High, V_{IN} = 400mV_{p-p}, No de-emphasis, No interconnect line	V_{CC}–0.3	V_{CC}–0.225	V_{CC}–0.15	
V_{RIP}	Differential output ripple	DIS = High, 50% Transitions of K28.5 pattern at 11.3Gbps, No interconnect line, V_{IN} = 1600mV_{p-p}		1.5	5	mV_{RMS}
DE	Output de-emphasis(2)	K28.5 Pattern at 11.3Gbps, No interconnect line, V_{IN} = 400mV_{p-p}, SWG = Open, Output de-emphasis off: DE0 = Low, DE1 = Low		0		dB
		K28.5 Pattern at 11.3Gbps, No interconnect line, V_{IN} = 400mV_{p-p}, SWG = Open, Maximum output de-emphasis: DE0 = High, DE1 = High		7		
DJ	Deterministic jitter	K28.5 Pattern at 11.3Gbps, 10-m 28-AWG Cable, V_{IN} = 400mV_{p-p}, SWG = Open, No de-emphasis, Maximum interconnect length setting		12		ps_{p-p}
		K28.5 Pattern at 11.3Gbps, 15-m 24-AWG Cable, V_{IN} = 400mV_{p-p}, SWG = Open, No de-emphasis, Maximum interconnect length setting		12		
RJ	Random jitter	K28.5 Pattern at 11.3Gbps, 10-m 28-AWG Cable, V_{IN} = 400mV_{p-p}, SWG = Open, No de-emphasis, Maximum interconnect length setting		1.0		ps_{RMS}
		K28.5 Pattern at 11.3Gbps, 15-m 24-AWG Cable, V_{IN} = 400mV_{p-p}, SWG = Open, No de-emphasis, Maximum interconnect length setting		1.0		
t_R	Output rise time	20% to 80%, No interconnect line, V_{IN} = 400mV_{p-p}, SWG = Open, No de-emphasis	20	28		ps
t_F	Output fall time	20% to 80%, No interconnect line, V_{IN} = 400mV_{p-p}, SWG = Open, No de-emphasis	20	28		
SDD11	Differential input return loss	0.01GHz < f < 3.9GHz		16		dB
		3.9GHz < f < 12.1GHz		See (3)		
SDD22	Differential output return loss	0.01GHz < f < 3.9GHz		16		dB
		3.9GHz < f < 12.1GHz		See (3)		
SCD11	Input differential to common-mode conversion	0.01GHz < f < 7.5GHz		25		dB
		7.5GHz < f < 12.1GHz		20		
SCC22	Common-mode output return loss	0.01GHz < f < 2.5GHz		13		dB
		2.5GHz < f < 12.1GHz		7		
V_{AS}	LOS Assert threshold voltage	K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = Open	25	60		mV_{p-p}
		K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = 1.0V	75	180		
V_{DAS}	LOS De-assert threshold voltage	K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = Open		100	150	mV_{p-p}
		K28.5 Pattern at 11.3Gbps, No interconnect, LOSR = High, LOSL = 1.0V		300	450	
	LOS Hysteresis	20log(V_{DAS} / V_{AS})	2.5	4.5		dB
$T_{AS/DAS}$	LOS Assert/de-assert time		2.5		50	µs
T_{DIS}	Disable response time			20		ns
	Latency	From DIN+/DIN– to DOUT+/DOUT–		150		ps

(2) See Table 1 and Figure 3 for output de-emphasis settings
(3) Differential Return Loss given by SDD11, SDD22 = 19.3 + 26.66 $\log_{10}$(f/8.25), f in GHz

Table 1. Available Output De-emphasis Settings

		DE0		
		LOW	**OPEN**	**HIGH**
DE1	**LOW**	0dB	0.875dB	1.75dB
	OPEN	2.625dB	3.5dB	4.375dB
	HIGH	5.25dB	6.125dB	7dB

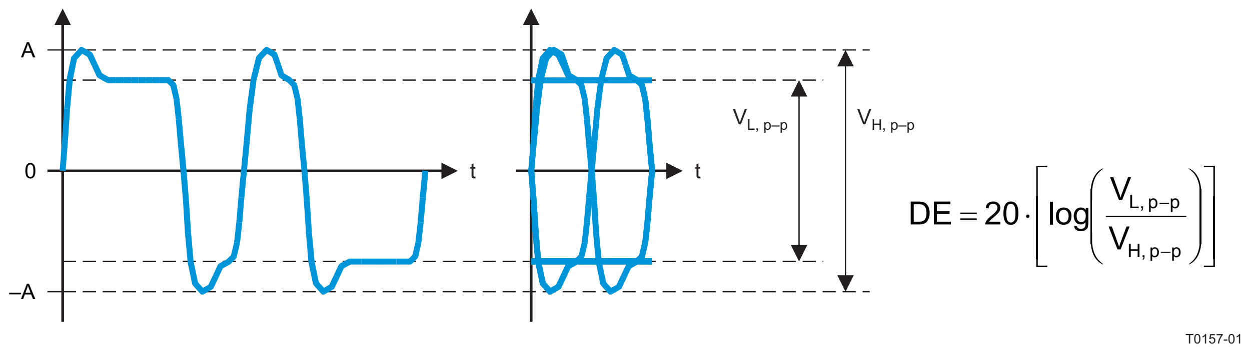


Figure 3. Output De-emphasis

Table 2. Available Interconnect Length Settings (24-AWG Twinaxial Cable Used as Reference)

		LN0	
		LOW	**HIGH**
LN1	**LOW**	0–5 meters	10–15 meters
	HIGH	5–10 meters	15–20 meters

TWO-WIRE SERIAL INTERFACE AND CONTROL LOGIC

FUNCTIONAL DESCRIPTION

The TLK1101E uses a two-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. Both inputs include 100kΩ pull-up resistors to VCC. For driving these inputs, an open-drain output is recommended.

The two-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The TLK1101E is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCL signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (0101000) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8-bit register address
4. 8-bit register data
5. STOP command

Regarding timing, the TLK1101E is I^{2}C-compatible. The typical timing is shown in Figure 4 and a complete data transfer is shown in Figure 5. Parameters for Figure 4 are defined in Table 3.

Bus Idle: Both SDA and SCL lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

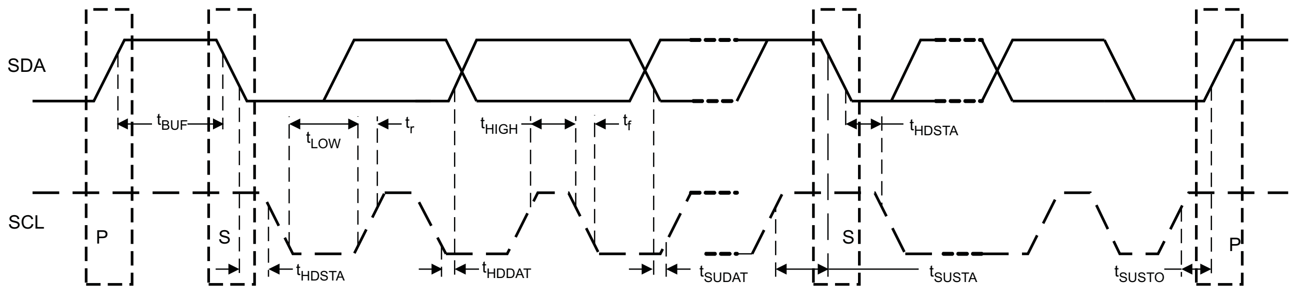


Figure 4. Two-Wire Serial Interface Timing Diagram.

Table 3. Two-Wire Serial Interface Timing Diagram Definitions

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SCL Clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCL clock	1.3		µs
t_{HIGH}	High period of the SCL clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCL signals		300	ns
t_F	Fall time of both SDA and SCL signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

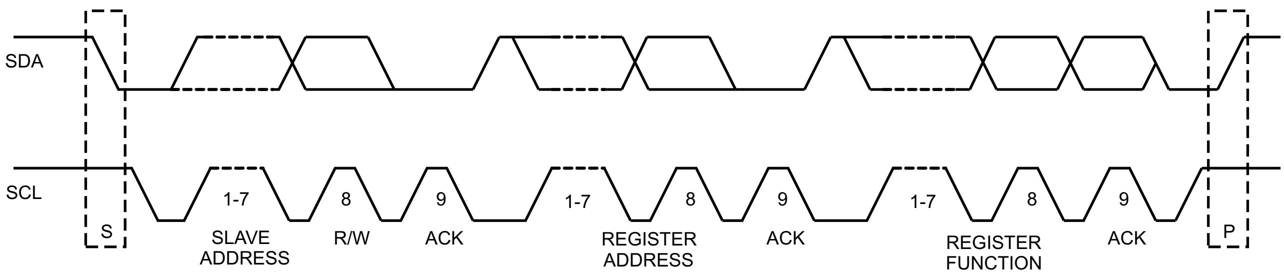


Figure 5. Two-Wire Serial Interface Data Transfer

REGISTER MAPPING

The register mapping for read/write register addresses 0 (0x00) through 13 (0x0D) are shown in Table 4 through Table 17. The register mapping for the read only register addresses 14 (0x0E) and 15 (0x0F) are shown in Table 18 and Table 19. Table 20 describes the circuit functionality based on the register settings.

Table 4. Register 0 (0x00) Mapping – Control Settings

register address 0 (0x00)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
REG11OFF	REG3OFF	REG2OFF	REG1OFF	DISABLE	LOS_RNG	OCOFF	I2CMODE

Table 5. Register 1 (0x01) Mapping – Input Threshold Adjust

register address 1 (0x01)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
THRESH7	THRESH6	THRESH5	THRESH4	THRESH3	THRESH2	THRESH1	THRESH0

Table 6. Register 2 (0x02) Mapping – De-emphasis Setting

register address 2 (0x02)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	DEEM3	DEEM2	DEEM1	DEEM0

Table 7. Register 3 (0x03) Mapping – Output Swing Control

register address3 (0x03)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	AMP1	AMP0

Table 8. Register 4 (0x04) Mapping

register address 4 (0x04)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 9. Register 5 (0x05) Mapping

register address 5 (0x05)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 10. Register 6 (0x06) Mapping

register address 6 (0x06)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 11. Register 7 (0x07) Mapping – Maximum Data Rate Setting

register address 7 (0x07)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
RATE_7	–	–	–	RATE_3	RATE_2	RATE_1	RATE_0

Table 12. Register 8 (0x08) Mapping

register address 8 (0x08)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 13. Register 9 (0x09) Mapping

register address 9 (0x09)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 14. Register 10 (0x0A) Mapping

register address 10 (0x0A)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 15. Register 11 (0x0B) Mapping – LOS Level Setting

register address 11 (0x0B)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
LOSLVL_7	LOSLVL_6	LOSLVL_5	LOSLVL_4	LOSLVL_3	LOSLVL_2	LOSLVL_1	LOSLVL_0

Table 16. Register 12 (0x0C) Mapping

register address 12 (0x0C)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 17. Register 13 (0x0D) Mapping

register address 13 (0x0D)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	–

Table 18. Register 14 (0x0E) Mapping – Selected Rate Setting (Read Only)

register address 14 (0x0E)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	SEL_RATE3	SEL_RATE2	SEL_RATE1	SEL_RATE0

Table 19. Register 15 (0x0F) Mapping – Selected LOS Level (Read Only)

register address 15 (0x0F)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	SEL_LOSL6	SEL_LOSL5	SEL_LOSL4	SEL_LOSL3	SEL_LOSL2	SEL_LOSL1	SEL_LOSL1

Table 20. Register Functionality

NAME	REGISTER DESCRIPTION	FUNCTION
REG11OFF	Address 0 bit 7: Register address 11 control	**Register address 11 control bit:** 1 = External LOS level (LOSL) control active 0 = Register address 11 settings active (default)
REG3OFF	Address 0 bit 6: Register address 3 control	**Register address 3 control bit:** 1 = External output swing (SWG) control active 0 = Register address 3 settings active (default)
REG2OFF	Address 0 bit 5: Register address 2 control	**Register address 2 control bit:** 1 = External output de-emphasis (DE) control active 0 = Register address 2 settings active (default)
REG1OFF	Address 0 bit 4: Register address 1 control	**Register address 1 control bit:** 1 = External input threshold (VTH) control active 0 = Register address 1 settings active (default)
DISABLE	Address 0 bit 3: Output disable	**Output disable bit:** 1 = Output disabled 0 = Output enabled (default)
LOS_RNG	Address 0 bit 2: LOS Range	**LOS Range bit:** 1 = High LOS assert voltage range 0 = Low LOS assert voltage range (default)
OCOFF	Address 0 bit 1: Offset cancellation disable	**Offset cancellation disable bit:** 1 = Offset cancellation is disabled 0 = Offset cancellation is enabled (default)
I2CMODE	Address 0 bit 0: Two-wire interface disable	**Two-wire interface disable bit:** 1 = Register settings active 0 = External control active (default)
THRESH7	Address 1 bit 7: Input threshold adjust bit 7 (MSB)	**Input threshold adjustment setting:** Maximum positive shift for 00000001 (1) Minimum positive shift for 01111111 (127) Zero shift for 10000000 (128) or 00000000 (0) (default) Minimum negative shift for 10000001 (129) Maximum negative shift for 11111111 (255)
THRESH6	Address 1 bit 6: Input threshold adjust bit 6	
THRESH5	Address 1 bit 5: Input threshold adjust bit 5	
THRESH4	Address 1 bit 4: Input threshold adjust bit 4	
THRESH3	Address 1 bit 3: Input threshold adjust bit 3	
THRESH2	Address 1 bit 2: Input threshold adjust bit 2	
THRESH1	Address 1 bit 1: Input threshold adjust bit 1	
THRESH0	Address 1 bit 0: Input threshold adjust bit 0 (LSB)	
DEEM3	Address 2 bit 3: De-emphasis adjust bit 3 (MSB)	**De-emphasis setting:**
DEEM2	Address 2 bit 2: De-emphasis adjust bit 2	
DEEM1	Address 2 bit 1: De-emphasis adjust bit 1	
DEEM0	Address 2 bit 0: De-emphasis adjust bit 0 (LSB)	

De-emphasis (dB)	Register Setting
0	0000 (default)
0.875	0001
1.75	0011
2.625	0100
3.5	0101
4.375	0111
5.25	1100
6.125	1101
7	1111

Table 20. Register Functionality (continued)

NAME	REGISTER DESCRIPTION	FUNCTION
AMP1	Address 3 bit 1: Output swing control bit 1 (MSB)	**Output swing control:** 00 = 300mV$_{p-p}$ 01 = 600mV$_{p-p}$ (default) 10 = 600mV$_{p-p}$ 11 = 900mV$_{p-p}$
AMP0	Address 3 bit 0: Output swing control bit 0 (LSB)	
RATE_7	Address 7 bit 7: Bandwidth selection bit 7 (MSB)	**Input filter bandwidth selection control bit:** 1 = Contents of register address 7 bits 3 to 0 are used to select the input filter bandwidth 0 = Bandwidth of 9.1GHz is used (default)
RATE_3	Address 7 bit 3: Bandwidth selection bit 3	**Input filter bandwidth selection bits:** Register 7 bits 3 to 0 are used to set the input filter bandwidth: 0000 = Maximum bandwidth 1111 = Minimum bandwidth
RATE_2	Address 7 bit 2: Bandwidth selection bit 2	
RATE_1	Address 7 bit 1: Bandwidth selection bit 1	
RATE_0	Address 7 bit 0: Bandwidth selection bit 0 (LSB)	
LOSLVL_7	Address 11 bit 7: LOS assert level bit 7 (MSB)	**LOS Assert level control bit:** 1 = Contents of register address 11 bits 6 to 0 are used to select the LOS assert level 0 = LOS Assert level of 50mV$_{p-p}$ is used (default)
LOSLVL_6	Address 11 bit 6: LOS assert level selection bit 6	**LOS Assert level selection bits:** Register 11 bits 6 to 0 are used to select the LOS assert level: 0000000 = Minimum LOS assert level 1111111 = Maximum LOS assert level
LOSLVL_5	Address 11 bit 5: LOS assert level selection bit 5	
LOSLVL_4	Address 11 bit 4: LOS assert level selection bit 4	
LOSLVL_3	Address 11 bit 3: LOS assert level selection bit 3	
LOSLVL_2	Address 11 bit 2: LOS assert level selection bit 2	
LOSLVL_1	Address 11 bit 1: LOS assert level selection bit 1	
LOSLVL_0	Address 11 bit 0: LOS assert level selection bit 0 (LSB)	
SEL_RATE3	Address 14 bit 3: Selected rate setting bit 3	**Selected rate setting (read only)**
SEL_RATE2	Address 14 bit 2: Selected rate setting bit 2	
SEL_RATE1	Address 14 bit 1: Selected rate setting bit 1	
SEL_RATE0	Address 14 bit 0: Selected rate setting bit 0	

Table 20. Register Functionality (continued)

NAME	REGISTER DESCRIPTION	FUNCTION
SEL_LOSL6	Address 15 bit 6: Selected LOS assert level bit 6 (MSB)	**Selected LOS assert level (read only)**
SEL_LOSL5	Address 15 bit 5: Selected LOS assert level bit 5	
SEL_LOSL4	Address 15 bit 4: Selected LOS assert level bit 4	
SEL_LOSL3	Address 15 bit 3: Selected LOS assert level bit 3	
SEL_LOSL2	Address 15 bit 2: Selected LOS assert level bit 2	
SEL_LOSL1	Address 15 bit 1: Selected LOS assert level bit 1	
SEL_LOS_0	Address 15 bit 0: Selected LOS assert level bit 0 (LSB)	

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C, V_{IN} = 400mV_{p-p}, DE0 = DE1 = low, SWG = open, LN0 = LN1 = high, and no interconnect line at the output (unless otherwise noted). Differential S-parameter characteristics of Spectra-Strip SkewClear EXD twinaxial cables and a 36-inch FR-4 stripline used for the measurements captured in this document are as shown in Figure 6.

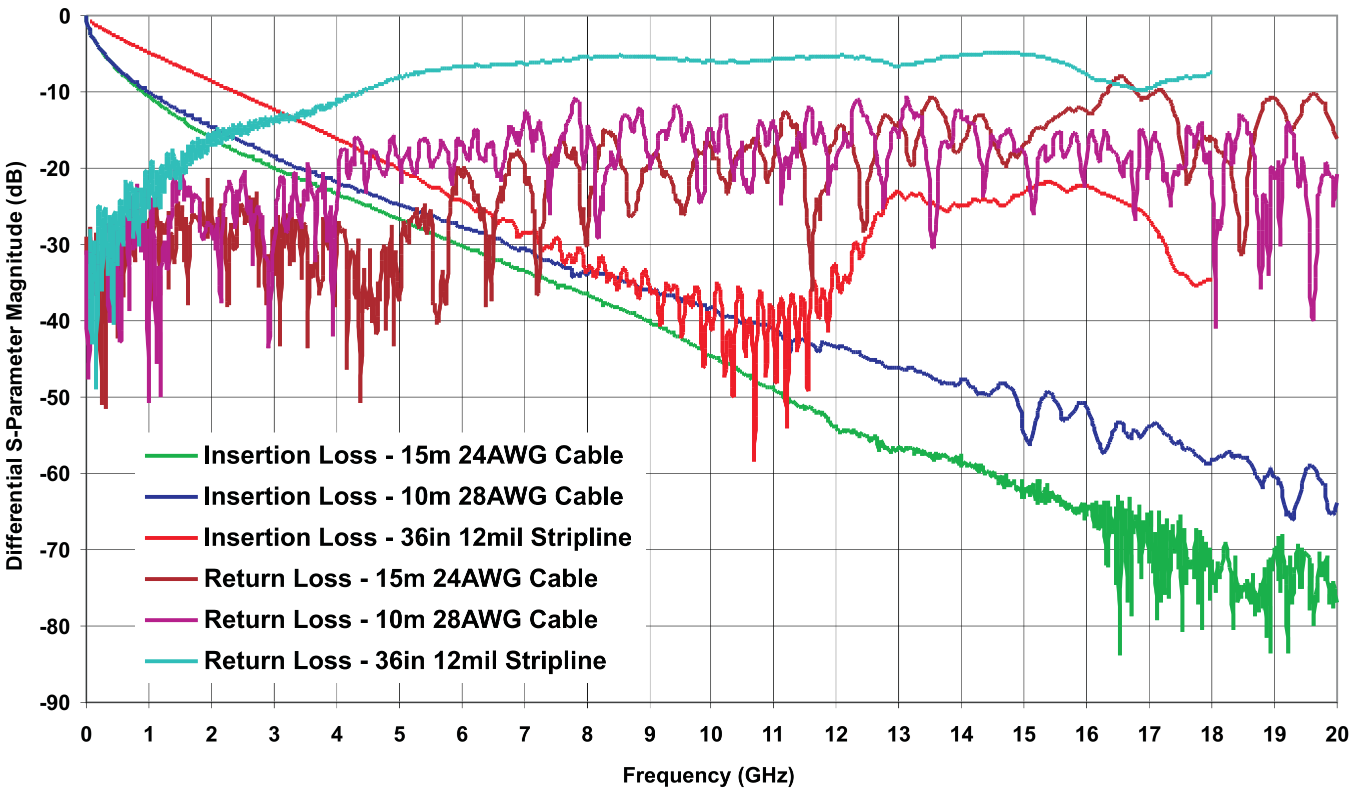


Figure 6. Typical Differential S-Parameter Characteristics of Interconnect Lines

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 11.3Gbps USING A K28.5 PATTERN

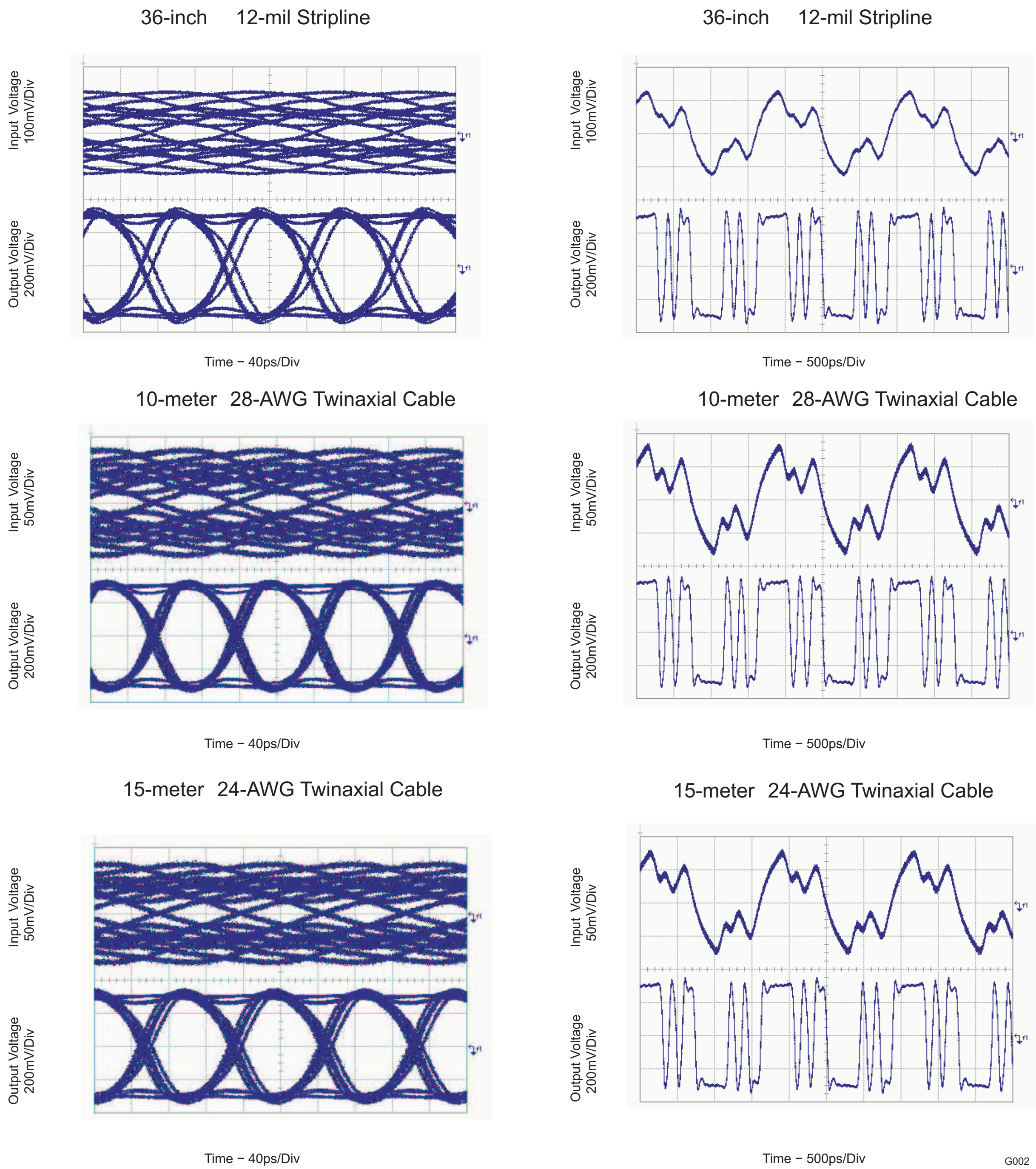


Figure 7. Equalizer Input and Output Signals with Different Interconnect Lines at 11.3Gbps

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 10.3125Gbps USING A K28.5 PATTERN

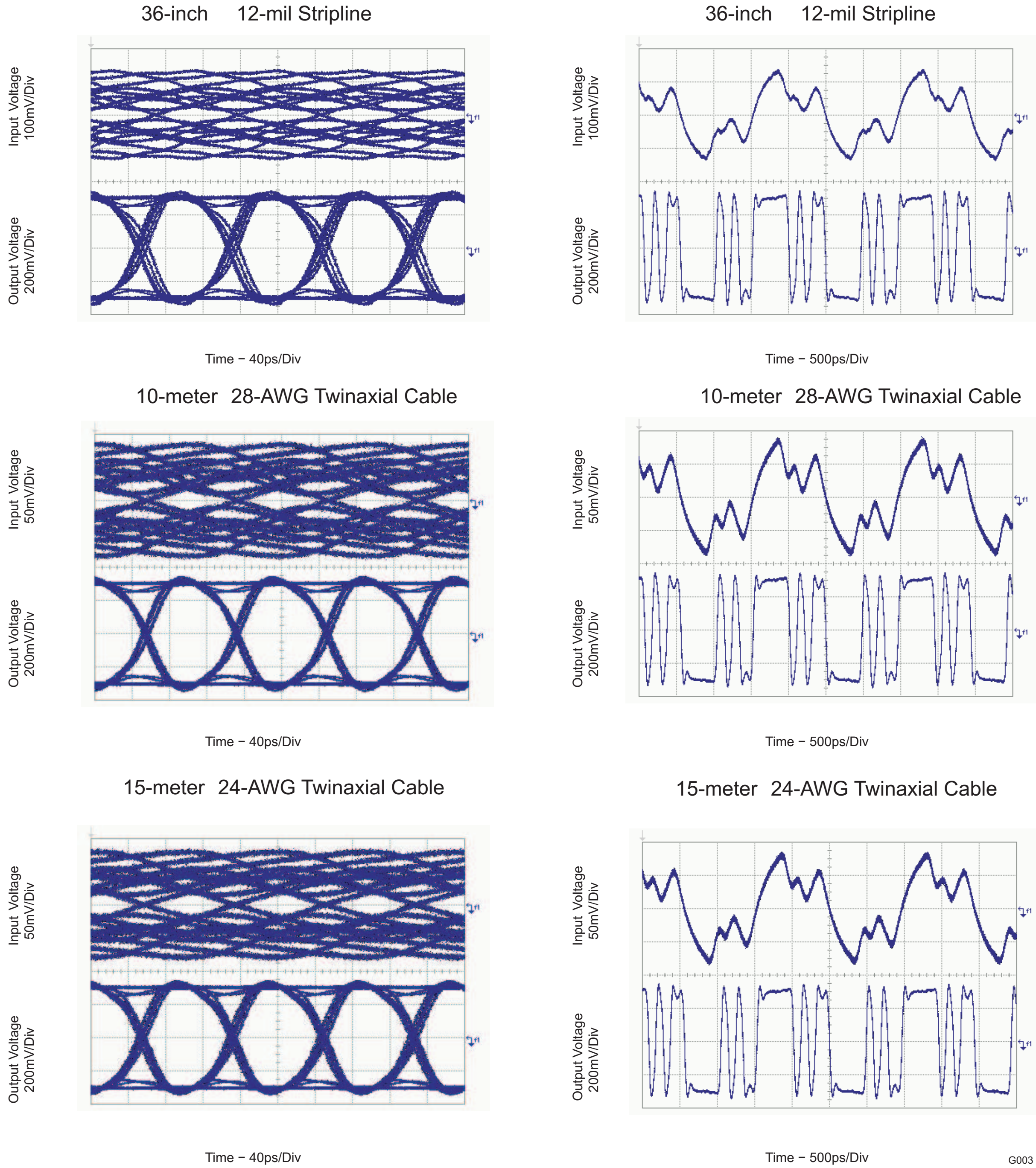


Figure 8. Equalizer Input and Output Signals with Different Interconnect Lines at 10.3125Gbps

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 8.5Gbps USING A K28.5 PATTERN

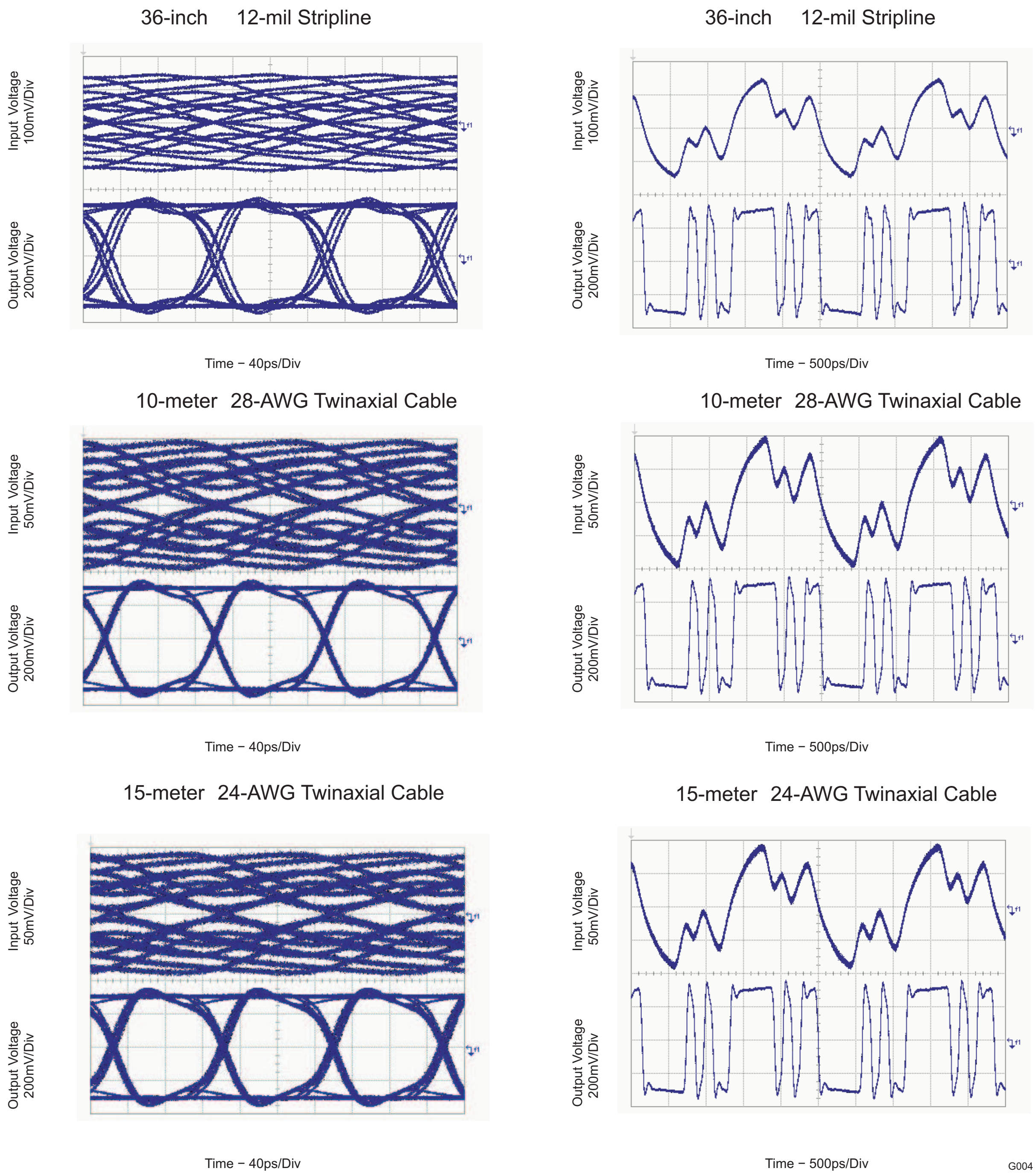


Figure 9. Equalizer Input and Output Signals with Different Interconnect Lines at 8.5Gbps.

TYPICAL CHARACTERISTICS (continued)

RANDOM JITTER
vs
INPUT VOLTAGE

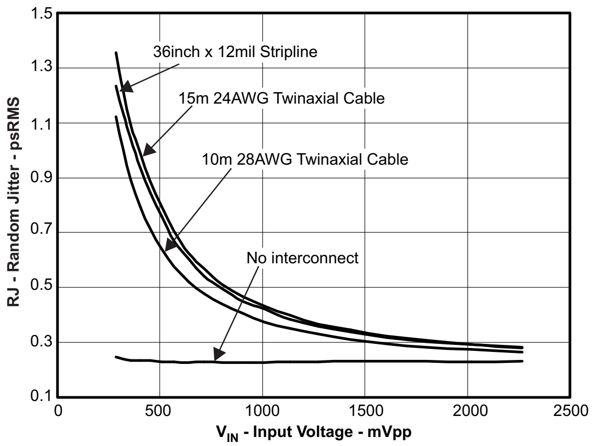


Figure 10.

RESIDUAL DETERMINISTIC JITTER
vs
INPUT VOLTAGE

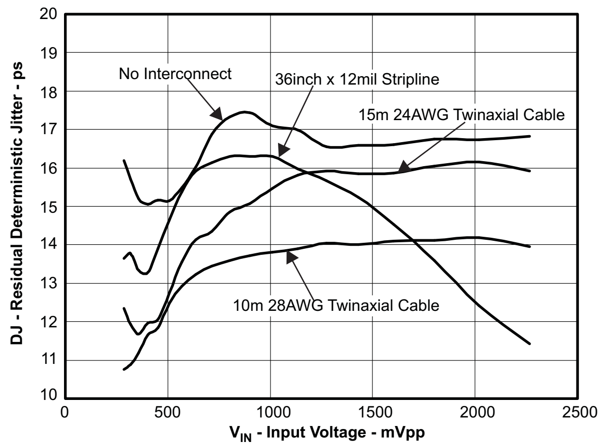


Figure 11.

DIFFERENTIAL INPUT RETURN LOSS
vs
FREQUENCY

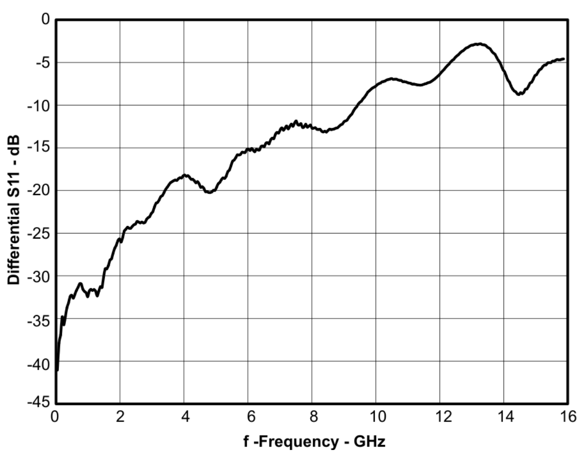


Figure 12.

DIFFERENTIAL OUTPUT RETURN LOSS
vs
FREQUENCY

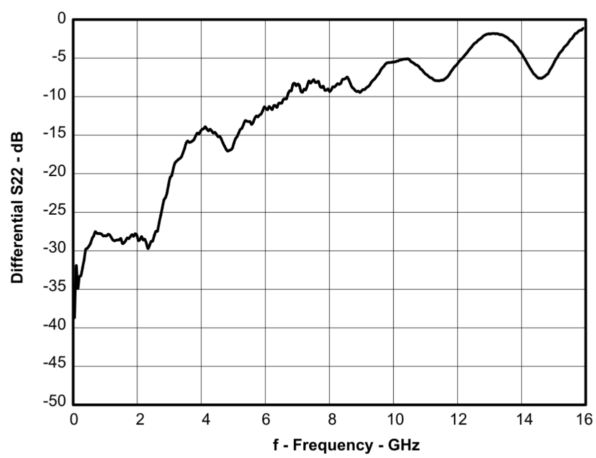


Figure 13.

TYPICAL CHARACTERISTICS (continued)

LOS THRESHOLD VOLTAGE vs LOSL VOLTAGE (LOSR = LOW)

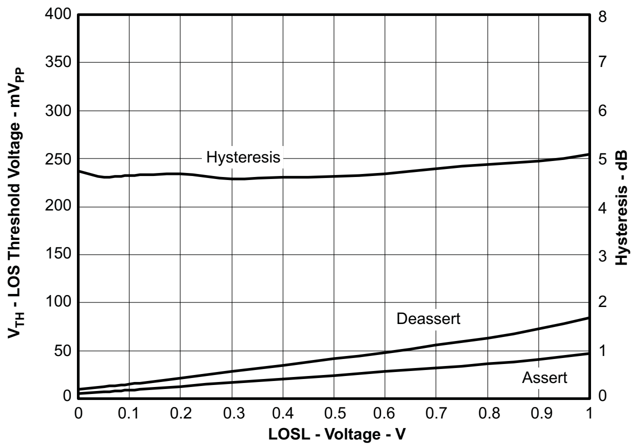


Figure 14.

LOS THRESHOLD VOLTAGE vs LOSL VOLTAGE (LOSR = HIGH)

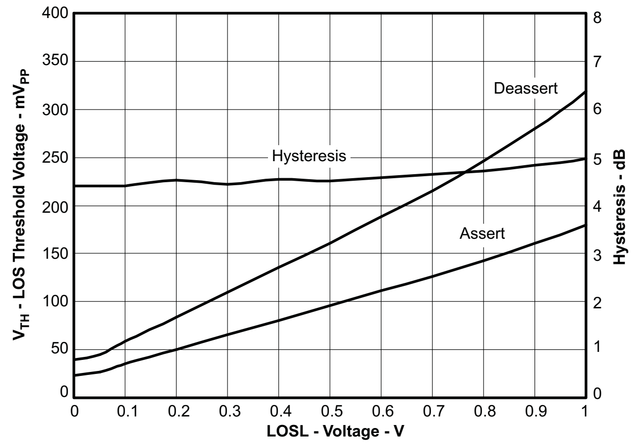


Figure 15.

LOS THRESHOLD VOLTAGE vs REGISTER 11 (0x0B) SETTING (LOSR = LOW)

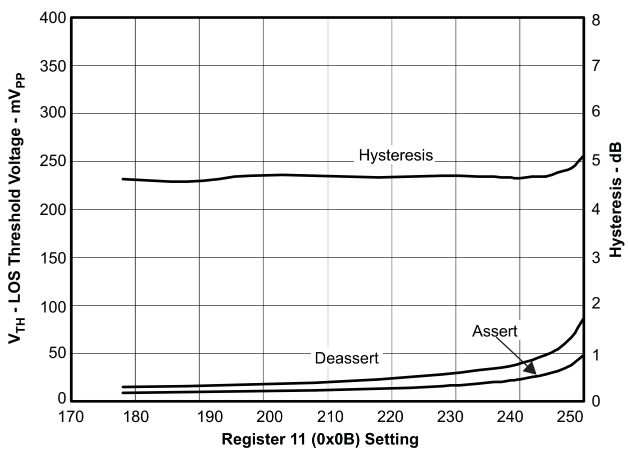


Figure 16.

LOS THRESHOLD VOLTAGE vs REGISTER 11 (0x0B) SETTING (LOSR = HIGH)

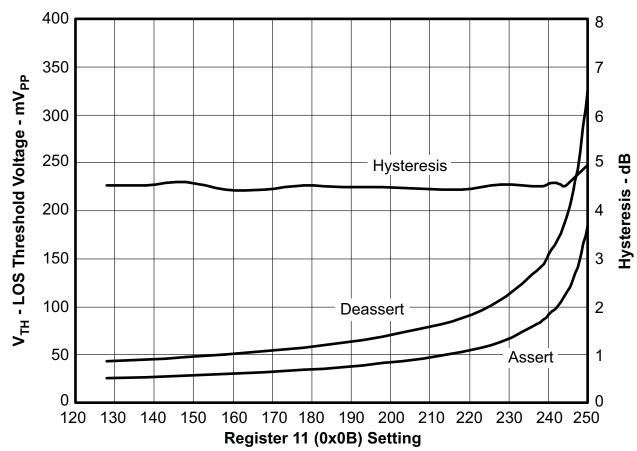


Figure 17.

TYPICAL CHARACTERISTICS (continued)

LOS THRESHOLD VOLTAGE vs DATA RATE (LOSL = 1V, LOSR = LOW)

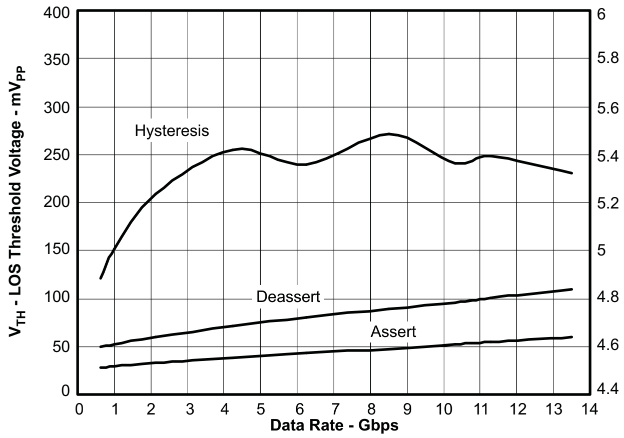


Figure 18.

LOS THRESHOLD VOLTAGE vs DATA RATE (LOSL = 1V, LOSR = HIGH)

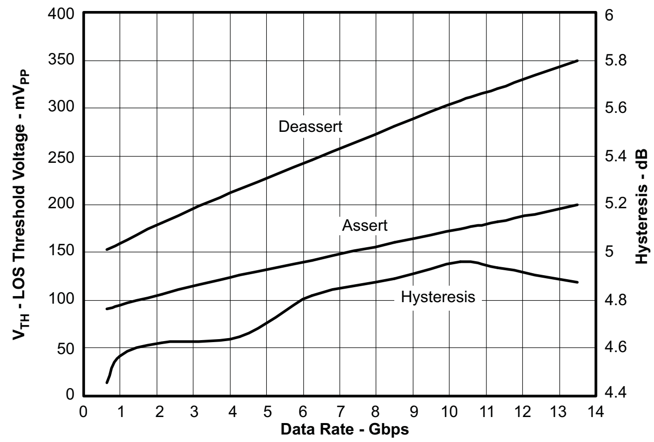


Figure 19.

Revision History

Changes from Original (August 2007) to Revision A	Page
• Added external pin configuration information - default device setup method to description	2
• Changed LN0 to LN1 in terminal functions table	3
• Changed LN1 to LN0 in terminal functions table	3
• Changed DE0 to DE1 in terminal functions table	3
• Changed DE1 to DE0 in terminal functions table	3
• Deleted fixed input equalizer in high frequency boost test conditions	4
• Added Twinaxial to Table 2 title	6
• Changed scale on Figure 7	15
• Changed scale on Figure 8	16
• Changed scale on Figure 9	17

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLK1101ERGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLK1101ERGPRG4	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLK1101ERGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLK1101ERGPTG4	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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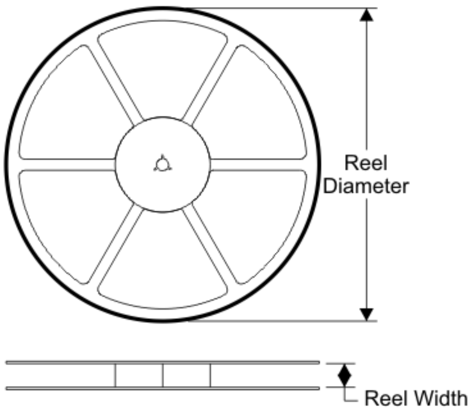
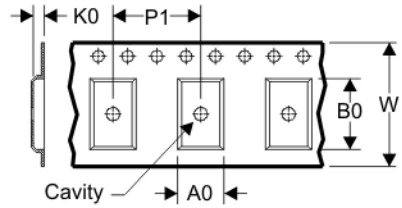
TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

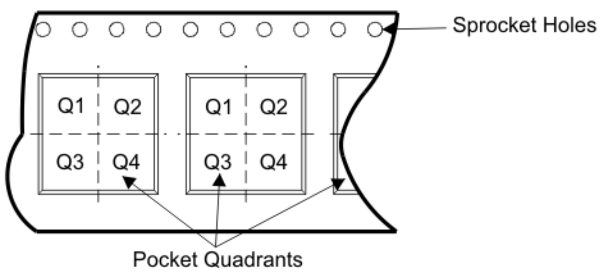


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

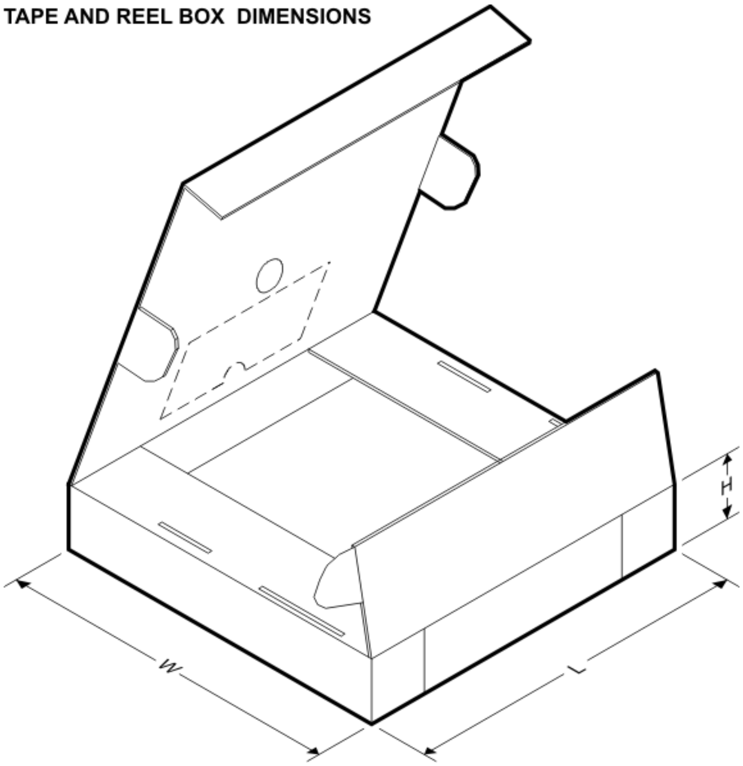
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK1101ERGPR	RGP	20	SITE 41	330	12	4.3	4.3	1.5	8	12	Q2
TLK1101ERGPT	RGP	20	SITE 41	180	12	4.3	4.3	1.5	8	12	Q2

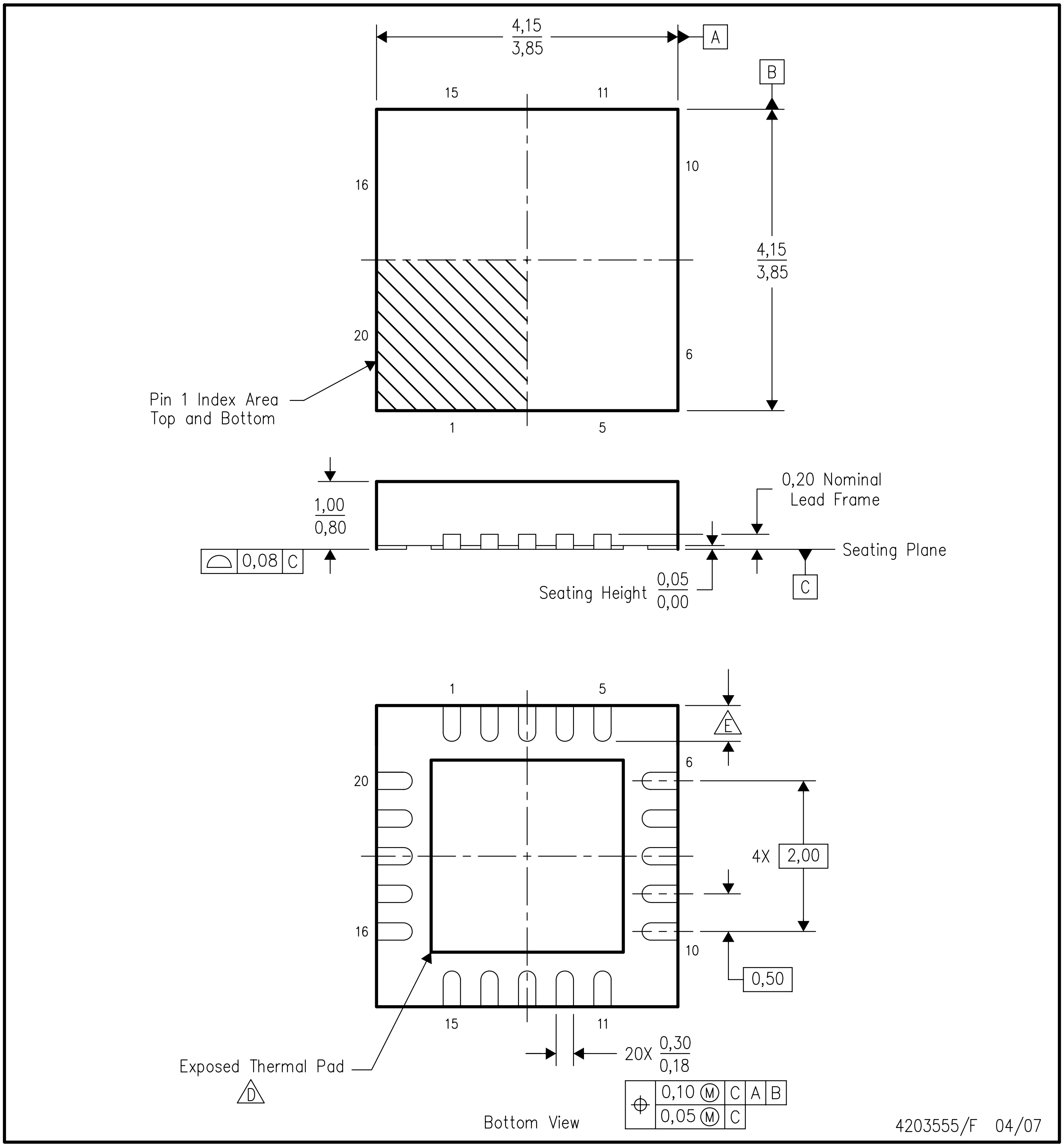
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TLK1101ERGPR	RGP	20	SITE 41	346.0	346.0	29.0
TLK1101ERGPT	RGP	20	SITE 41	190.0	212.7	31.75

RGP (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No–Lead) package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

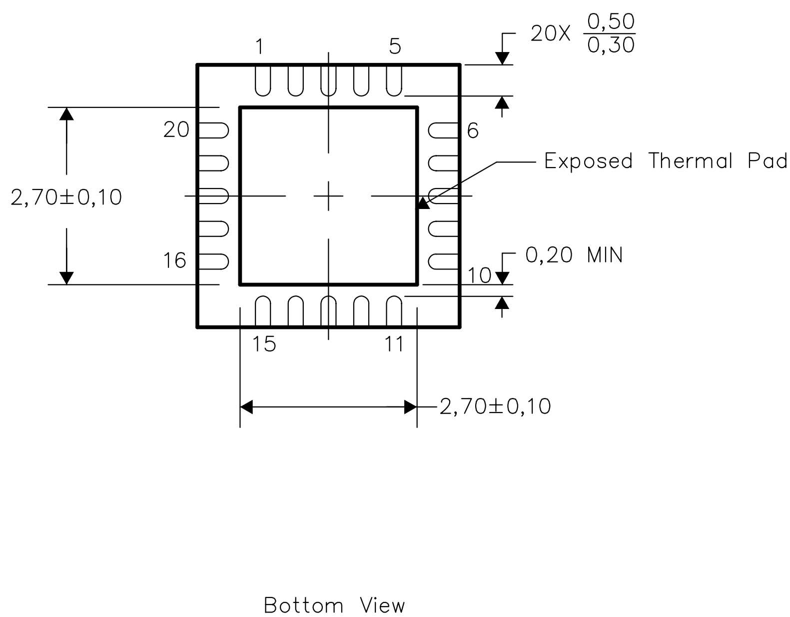
E. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

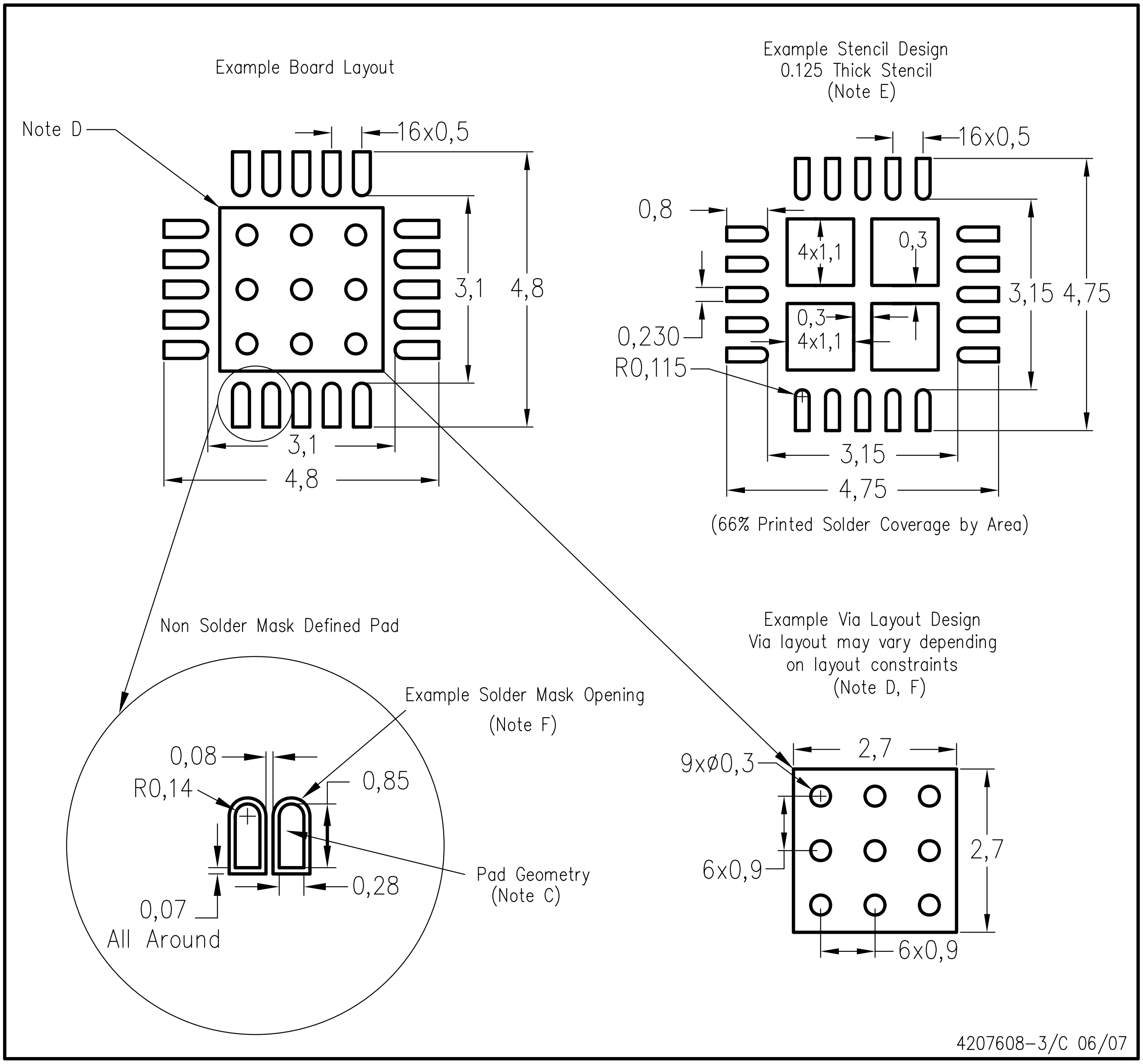
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGP (S–PQFP–N20)



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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