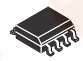
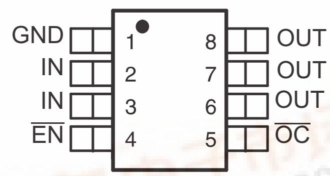

D–8

SINGLE-CHANNEL 100 mA POWER SWITCH

FEATURES

- **100-mA Continuous Current**
- **600-mΩ High-Side MOSFET**
- **Thermal and Short-Circuit Protection**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{\text{OC}}$)**
- **43 µA Quiescent Supply Current**
- **1-µA Maximum Standby Supply Current**
- **SOIC-8 Package**
- **Ambient Temperature Range: –40°C to 85°C**
- **2 µS Response Time to Short Circuit**

**D PACKAGE
(TOP VIEW)**



DESCRIPTION

The TPS2049 power-distribution switch is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. This device incorporates a 600-mΩ N-channel MOSFET power switch for power-distribution systems that require only one power distribution path. The switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{\text{OC}}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 150mA typically.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTION AND ORDERING INFORMATION(1)

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (mA)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (mA)	NUMBER OF SWITCHES	SOIC (D)
–40°C to 85°C	Active low	100	150	Single	TPS2049D(2)

(1) For the most current package and ordering nformation, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2042BDR)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			VALUE	UNIT
$V_{I(IN)}$	Input voltage range (2)		–0.3 to 6	V
$V_{O(OUT)}$	Output voltage range (2)		-0.3 to 6	V
$V_{I(\overline{EN})}$	Input voltage range		–0.3 to 6	V
$V_{I(\overline{OC})}$	Voltage range		–0.3 to 6	V
$I_{O(OUT)}$	Continuous output current		Internally limited	
	Continuous total power dissipation		See Dissipation Rating Table	
T_J	Operating virtual junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
	Electrostatic discharge (ESD) protection	Human body model MIL-STD-883C	2	kV
		Charge device model (CDM)	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATING RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D-8	585.82 mW	5.8582 mW/°C	322.20 mW	234.32 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{I(IN)}$	Input voltage	2.7	5.5	V
$V_{I(\overline{EN})}$	Input voltage	0	5.5	V
$I_{O(OUT)}$	Continuous output current	0	100	mA
T_J	Operating virtual junction temperature	–40	125	°C

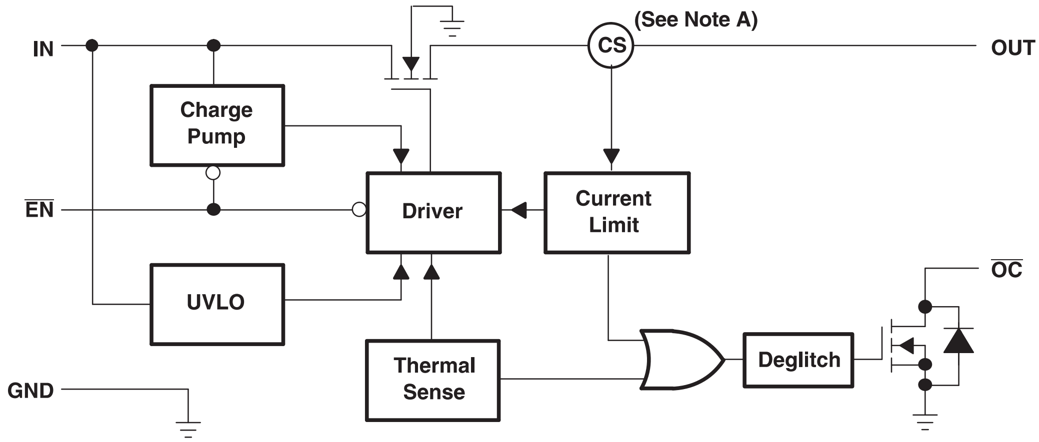
ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 90 mA, $V_{I(\overline{EN})}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
POWER SWITCH								
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation and 2.7-V operation	$V_{I(IN)}$ = 2.7 V or 5.5 V,	I_O = 90 A,	–40°C < T_J < 125°C		400	650	mΩ
t_r	Rise time, output	$V_{I(IN)}$ = 2.7 V	C_L = 1 µF,	R_L = 50 Ω, T_J = 25°C		0.1	0.4	ms
t_f	Fall time, output	$V_{I(IN)}$ = 2.7 V	C_L = 1 µF,	R_L = 50 Ω, T_J = 25°C	0.03		0.3	ms
ENABLE INPUT $\overline{EN}$								
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$≤ 5.5 V			2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$≤ 5.5 V					0.8	V
I_I	Input current	$V_{I(\overline{EN})}$ = 0 V or $V_{I(EN)}$ = $V_{I(IN)}$			–0.5		0.5	µA
t_{on}	Turnon time	C_L = 1 µF, R_L = 50 Ω, T_J = 25°C					1	ms
t_{off}	Turnoff time	C_L = 1 µF, R_L = 50 Ω, T_J = 25°C					1	ms
CURRENT LIMIT								
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short-circuit, 10°C < T_J < 40°C			100	150	200	mA
I_{OC_trip}	Overcurrent trip threshold	10°C < T_J < 40°C, 100 A/sec current rate increase					325	mA
	Short-circuit response tme					2		µs
SUPPLY CURRENT								
Supply current, low-level output		No load on OUT	$V_{I(\overline{EN})}$ = 5.5 V	T_J = 25°C		0.5	1	µA
				–40°C ≤ T_J ≤ 125°C		0.5	5	
Supply current, high-level output		No load on OUT	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C		43	60	µA
				–40°C ≤ T_J ≤ 125°C		43	70	
Leakage current		OUT connected to ground	$V_{I(\overline{EN})}$ = 5.5 V,	–40°C ≤ T_J≤ 125°C		1		µA
Reverse leakage current		IN = ground	$V_{I(OUT)}$ = 5.5 V, $V_{I(\overline{EN})}$ = 0 V	T_J = 25°C		0		µA
UNDERVOLTAGE LOCKOUT								
IN	Low-level input voltage				2		2.5	V
IN	Hysteresis	T_J = 25°C				75		mV
OVERCURRENT $\overline{OC}$								
$V_{OL(\overline{OC})}$	Output low voltage	$I_{O(\overline{OC})}$ = 5 mA					0.4	V
Off-state current		$V_{O(\overline{OC})}$ = 5 V or 3.3 V					1	µA
$\overline{OC}$ deglitch		$\overline{OC}$ assertion or deassertion			4	8	15	ms
THERMAL SHUTDOWN(2)								
Thermal shutdown threshold					135			°C
Recovery from thermal shutdown					125			°C
Hysteresis						10		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) The thermal shutdown only reacts under overcurrent conditions.

FUNCTIONAL BLOCK DIAGRAM



Note A: Current sense

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN1}$	4	I	Enable input, logic low turns on power switch
GND	1	I	Ground
IN	2, 3	I	Input voltage
$\overline{OC}$	5	O	Overcurrent, report, active-low, open-drain output
OUT	6, 7, 8	O	Power-switch output

PARAMETER MEASUREMENT INFORMATION

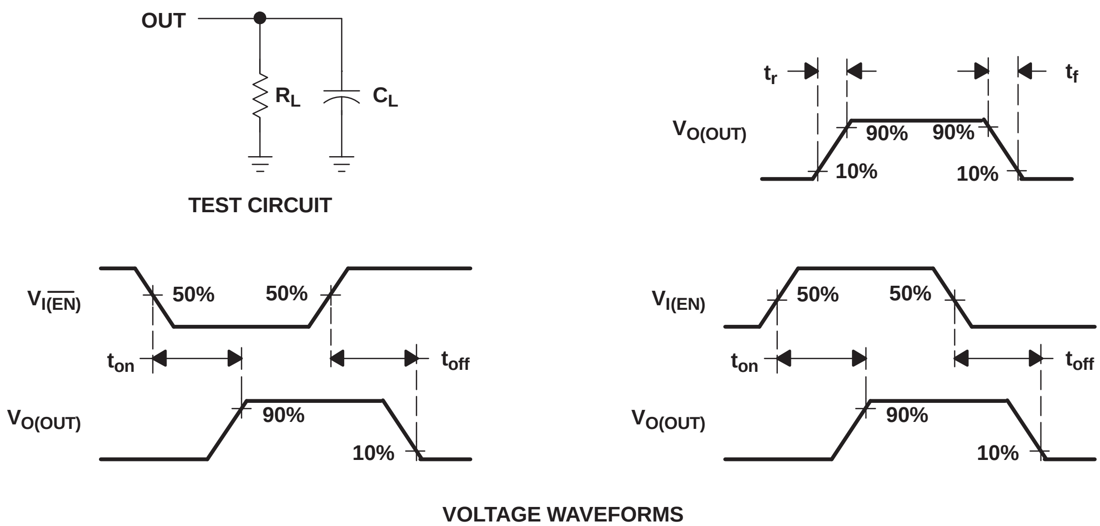


Figure 1. Test Circuit and Voltage Waveforms

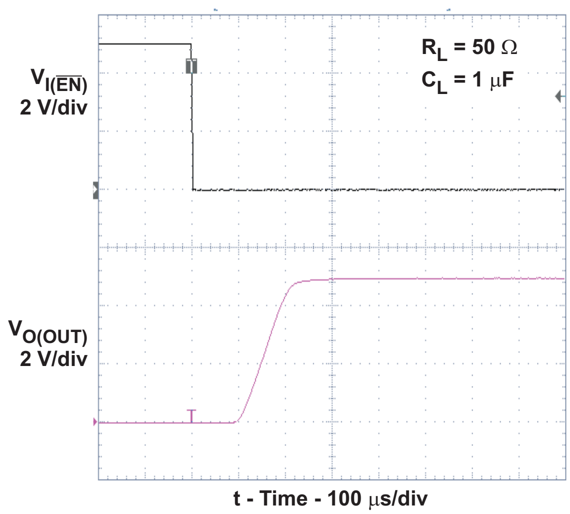


Figure 2. Turnon Delay and Rise Time With 1-µF Load

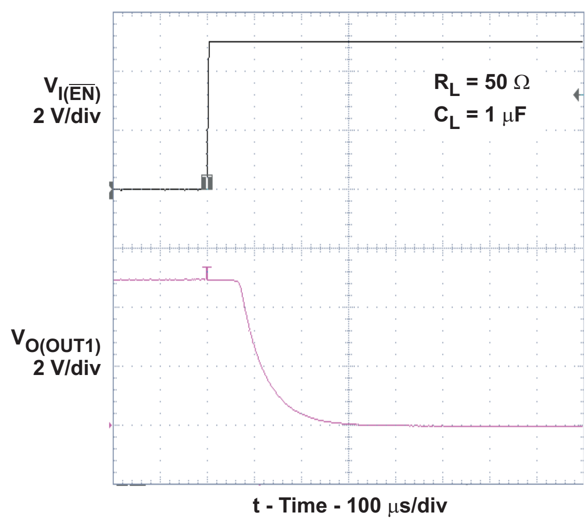


Figure 3. Turnoff Delay and Fall Time With 1-µF Load

PARAMETER MEASUREMENT INFORMATION (continued)

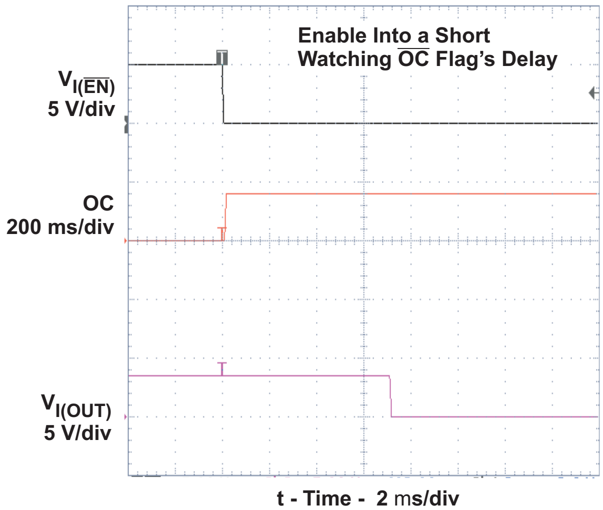


Figure 4. Device Enabled Into a Short

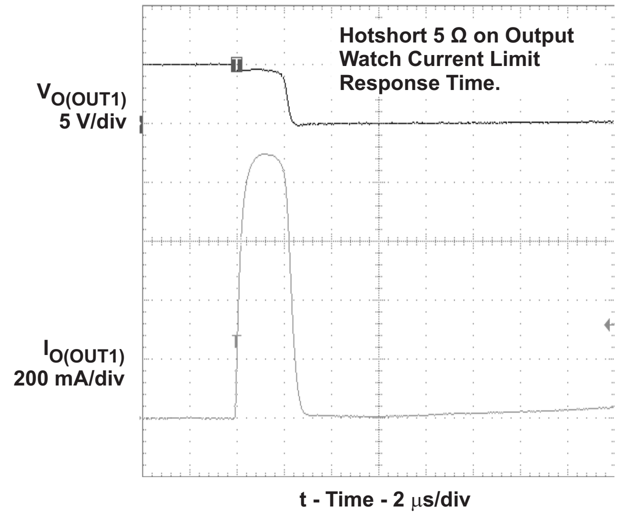


Figure 5. 5-Ω Load Connected to Enabled Device

APPLICATION INFORMATION

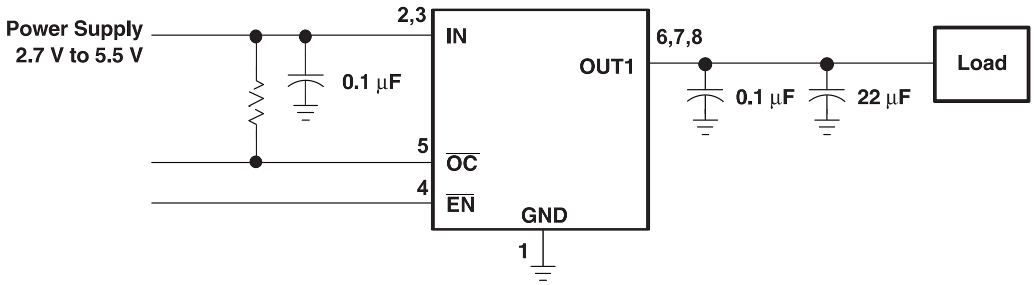


Figure 6. Typical Application

POWER-SUPPLY CONSIDERATIONS

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current–sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before VI(IN) has been applied (see Figure 6). The TPS2049 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, very high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2049 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OC}}$ occurs due to the 10-ms deglitch circuit. The TPS2049 is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OC}}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

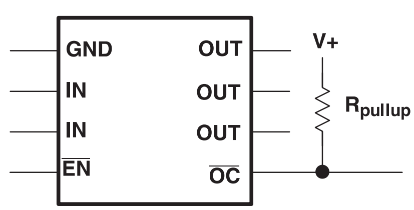


Figure 7. Typical Circuit for the $\overline{\text{OC}}$ Pin

APPLICATION INFORMATION (continued)

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the n-channel MOSFET allows small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\Theta JA} + T_A$$

Where:

T_A = Ambient temperature °C

$R_{\Theta JA}$ = Thermal resistance

P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS2049 implement a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature will rise due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OC}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION (continued)

GENERIC HOT-PLUG APPLICATIONS (see Figure 8)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2049, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2049 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

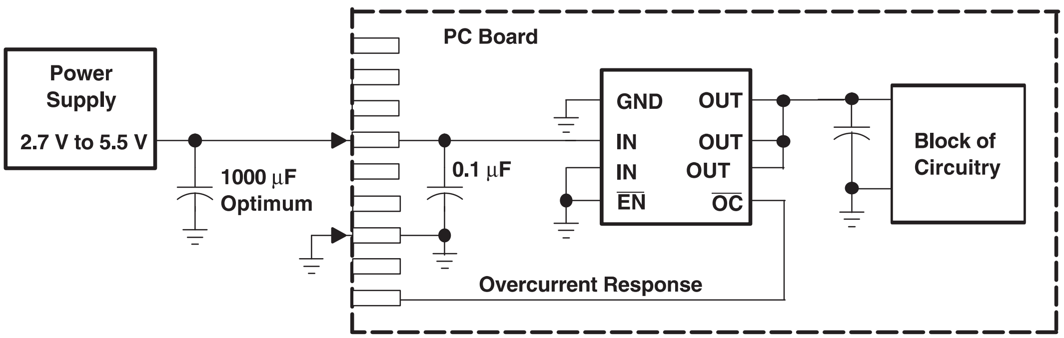


Figure 8. Typical Hot-Plug Implementation

By placing the TPS2049 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

DETAILED DESCRIPTION

POWER SWITCH

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 90 mA.

CHARGE PUMP

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

DRIVER

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

ENABLE ($\overline{EN}$)

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA when a logic high is present on $\overline{EN}$. A logic zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

DETAILED DESCRIPTION (continued)

OVERCURRENT ($\overline{OC}$)

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OC}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OC}$ is asserted instantaneously.

CURRENT SENSE

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

THERMAL SENSE

The TPS2049 implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OC}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

UNDERVOLTAGE LOCKOUT

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2V, a control signal turns off the power switch.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS2049D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2049DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2049DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2049DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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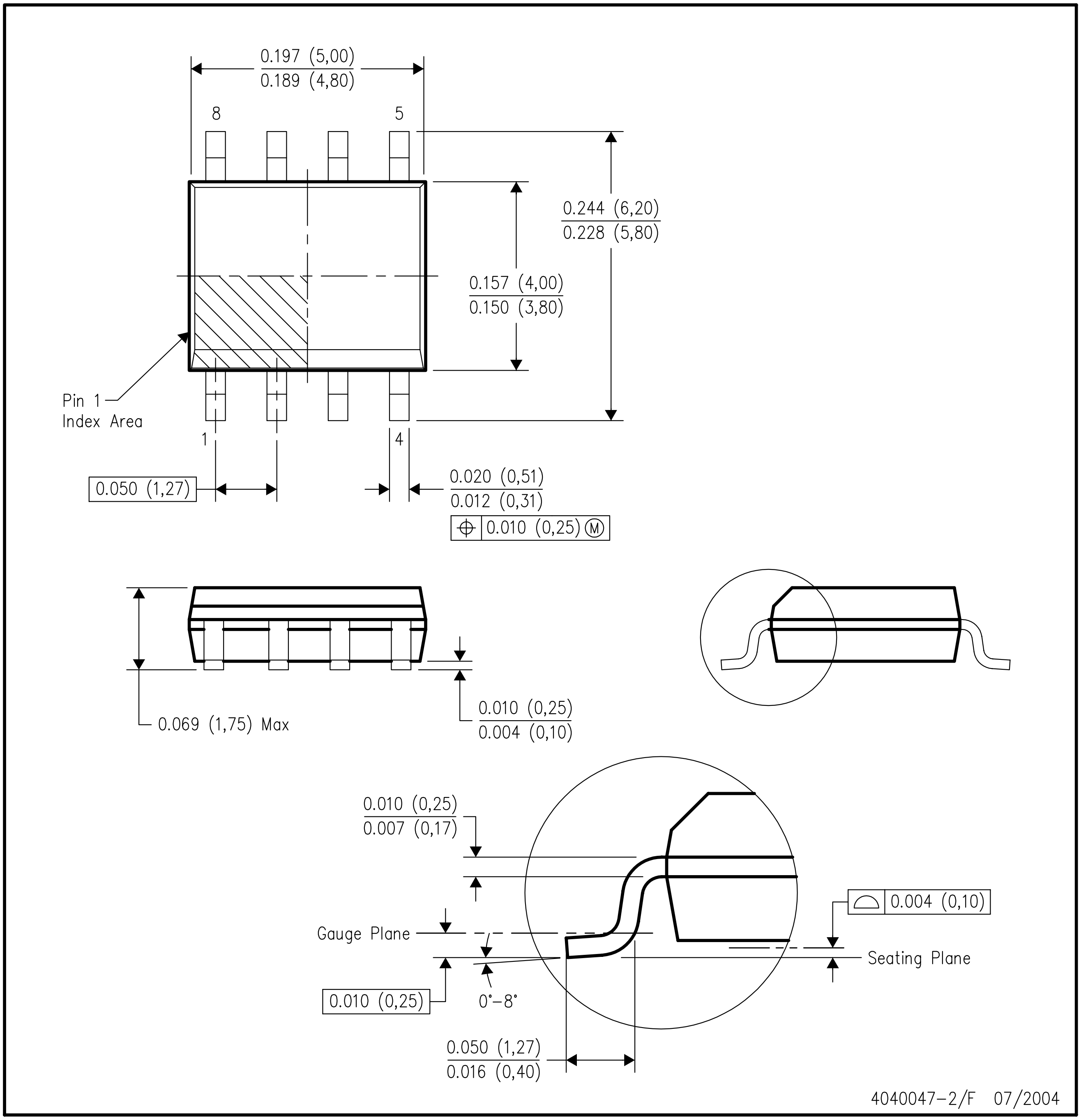
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265