LTC4245

Multiple Supply Hot Swap Controller with I²C Compatible Monitoring

FEATURES

- **Allows Safe Insertion into Live CompactPCI™ or PCI Express™ Backplane**
- **8-Bit ADC Monitors Current and Voltage**
- **I²C™/SMBus Interface**
- **dI/dt Controlled Soft Start**
- Simultaneous or Sequenced Turn-On
- ±20V Absolute Maximum Rating for ±12V Supplies
- No External Gate Capacitor Required
- Dual-Level Circuit Breaker and Current Limit
- Bus Precharge Output
- Power Good Input with Timeout
- Optional Latchoff or Autoretry After Faults
- Alerts Host After Faults
- Integrated LOCAL_PCI_RST# Logic
- 36-Pin SSOP and 38-Pin (5mm × 7mm) QFN Packages

APPLICATIONS

- Live Board Insertion
- CompactPCI, CompactPCI Express, CompactTCA, PCI Express Systems

DESCRIPTION

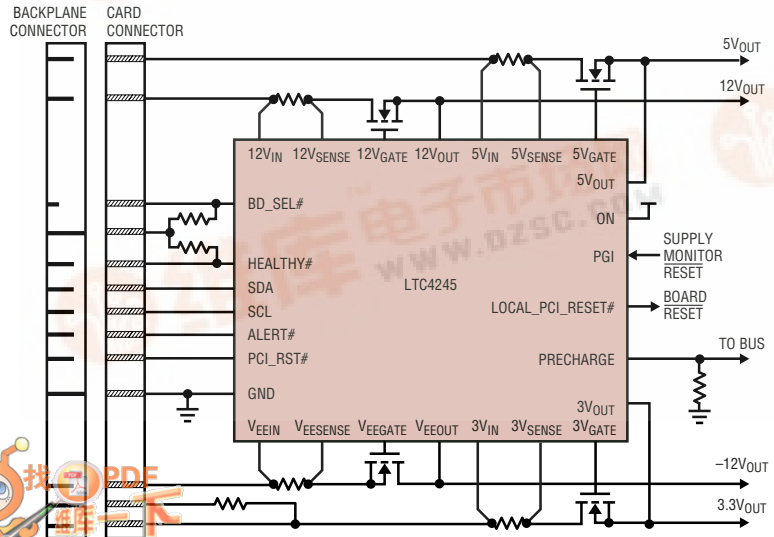
The LTC®4245 Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane in multiple supply systems such as CompactPCI and PCI Express. Using four external N-channel pass transistors, the board supply voltages can be ramped up at an adjustable rate and in any desired sequence. An I²C interface and onboard ADC allow monitoring of board current, voltage and fault status for each supply.

The device features adjustable dI/dt controlled soft start and foldback limited inrush current. A dual-level timed circuit breaker and fast current limit protect each supply against overcurrent faults. A power good input with timeout allows a downstream supply monitor to disconnect the board supplies. The device can be configured to function without a –12V supply or with an extra 3.3V supply instead of a 5V supply.

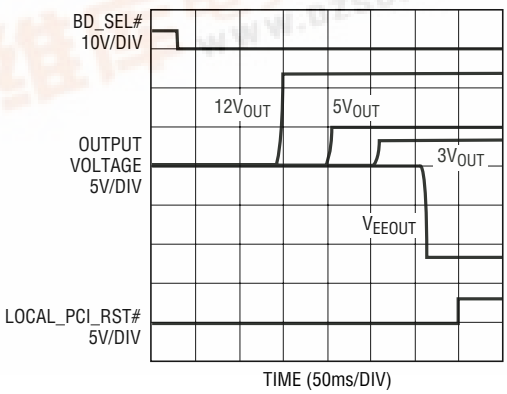
The controller has additional features to interrupt the host when a fault has occurred, notify when output power is good, detect insertion of a load card and power-up in either the on or off state.

TYPICAL APPLICATION

CompactPCI Application



Sequenced Turn-On Waveform



4245 TA01b

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages
- $12V_{IN}$ ..... –0.3V to 20V
- $5V_{IN}$, $3V_{IN}$ ..... –0.3V to 10V
- V_{EEIN} ..... –20V to 0.3V
- $INTV_{CC}$ ..... –0.3V to 6.5V

Input Voltages
- BD_SEL#, ON, PGI ..... –0.3V to 12V
- ADR0-3, CFG, SS, TIMER ..... –0.3V to $INTV_{CC}$ + 0.3V
- PCI_RST#, SCL, SDA ..... –0.3V to 6.5V

Output Voltages
- ALERT#, GPIO1-3, HEALTHY#, LOCAL_PCI_RST# ..... –0.3V to 6.5V

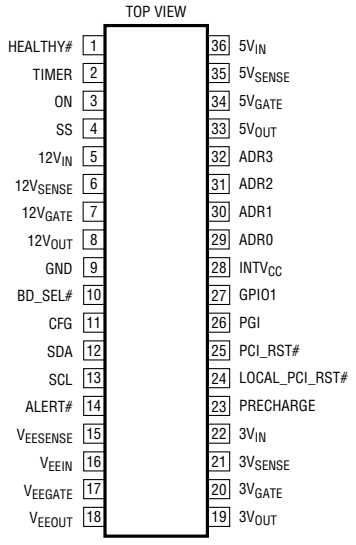
Analog Voltages (n is 5V, 3V)
- $12V_{GATE}$ ..... –0.3V to 25V
- n_{GATE} (Note 3) ..... –0.3V to $12V_{IN}$ + 0.3V or 14V
- $V_{EEGATE} – V_{EEIN}$ (Note 4) ..... –0.3V to 5V
- $12V_{SENSE}$ ..... –0.3V or $12V_{IN}$ – 6V to $12V_{IN}$ + 0.3V
- n_{SENSE} ..... –0.3V to n_{IN} + 0.3V
- $V_{EESENSE}$ ..... V_{EEIN} – 0.3V to 0.3V
- $12V_{OUT} – 12V_{GATE}$ (Note 4) ..... –5V to 0.3V
- $n_{OUT} – n_{GATE}$ (Note 4) ..... –5V to 0.3V
- V_{EEOUT} (Note 5) ..... –20V to 0.3V
- PRECHARGE ..... –0.3V to $3V_{IN}$ + 0.3V

Operating Temperature Range
- LTC4245C ..... 0°C to 70°C
- LTC4245I ..... –40°C to 85°C

Storage Temperature Range
- G Package ..... –65°C to 150°C
- UHF Package ..... –65°C to 125°C

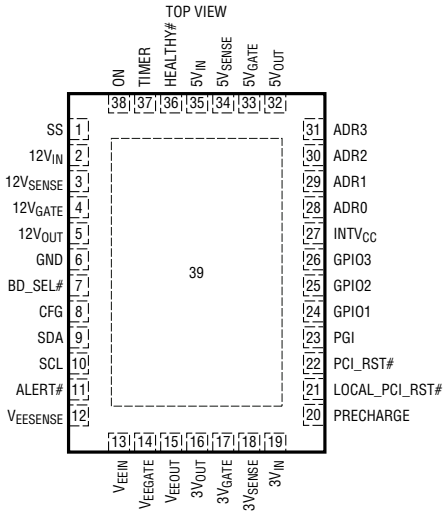
Lead Temperature (Soldering, 10 sec)
- G Package ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) PCB GND CONNECTION OPTIONAL

ORDER PART NUMBER	ORDER PART NUMBER	UHF PART MARKING*
LTC4245CG LTC4245IG	LTC4245CUHF LTC4245IUHF	4245 4245

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{5VIN} = 5V, V_{3VIN} = 3.3V, V_{VEEIN} = –12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{DD}	Input Supply Current	$12V_{IN}$	●		3	5	mA
		$5V_{IN}$	●		0.5	1	mA
		$3V_{IN}$, PRECHARGE Open	●		0.6	1	mA
		V_{EEIN}	●		–0.5	–1	mA
V_{UVL}	Supply Undervoltage Lockout	$12V_{IN}$	●	10.2	10.5	10.8	V
		$5V_{IN}$, V_{CFG} = 0V, Open	●	4.25	4.38	4.5	V
		$5V_{IN}$ When V_{CFG} = V_{CC}, $3V_{IN}$	●	2.7	2.8	2.9	V
		V_{EEIN}, V_{CFG} = 0V	●	–10.2	–10.5	–10.8	V
		V_{CC} Falling	●	3.4	3.8	4.2	V
V_{CC}	Internal Regulator Voltage		●	5	5.5	6	V
Current Limit							
$\Delta V_{SNS(CB)}$	Circuit Breaker Trip Sense Voltage	After Start-Up					
	(V_{12VIN} – $V_{12VSENSE}$)		●	45	50	55	mV
	(V_{5VIN} – $V_{5VSENSE}$)		●	22.5	25	27.5	mV
	(V_{3VIN} – $V_{3VSENSE}$)		●	22.5	25	27.5	mV
	($V_{VEESENSE}$ – V_{VEEIN})		●	40	50	60	mV
$\Delta V_{SNS(ACL)}$	Active Current Limit Sense Voltage	After Start-Up					
	(V_{12VIN} – $V_{12VSENSE}$)		●	130	150	170	mV
	(V_{5VIN} – $V_{5VSENSE}$)		●	60	75	90	mV
	(V_{3VIN} – $V_{3VSENSE}$)		●	60	75	90	mV
	($V_{VEESENSE}$ – V_{VEEIN})		●	130	150	170	mV
$\Delta V_{SNS(FBL)}$, $\Delta V_{SNS(FBH)}$	Foldback Current Limit Sense Voltage	Start-Up, V_{TIMER} = 0V					
	(V_{12VIN} – $V_{12VSENSE}$)	V_{12VOUT} = 0V	●	10	15	20	mV
		V_{12VOUT} = 12V	●	40	50	60	mV
	(V_{5VIN} – $V_{5VSENSE}$)	V_{5VOUT} = 0V	●	4	7.5	11	mV
		V_{5VOUT} = 5V	●	22	25	29	mV
	(V_{3VIN} – $V_{3VSENSE}$)	V_{3VOUT} = 0V	●	4	7.5	11	mV
		V_{3VOUT} = 3.3V	●	22	25	29	mV
	($V_{VEESENSE}$ – V_{VEEIN})	V_{VEEOUT} = 0V	●	11	16	21	mV
		V_{VEEOUT} = –12V	●	40	50	60	mV
Gate Drive							
ΔV_{GATE}	Gate Drive	Gate to Source	●	5	6.2	7.5	V
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, ΔV_{GATE} = 0V	●	–16	–20	–24	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	Gate Drive Off, ΔV_{GATE} = 5V					
	$12V_{GATE}$, $5V_{GATE}$, $3V_{GATE}$,	V_{OUT} = V_{IN}	●	0.9	1.3	1.7	mA
	V_{EEGATE}	$V_{VEEGATE}$ = –7V	●	1.7	3.5	5.3	mA
$I_{GATE(FST)}$	Gate Fast Pull-Down Current	Fast Turn Off, ΔV_{GATE} = 5V					
	$12V_{GATE}$, $5V_{GATE}$	$V_{12VGATE}$ = 17V, V_{5VGATE} = 10V	●	125	250	375	mA
	$3V_{GATE}$	V_{3VGATE} = 8.3V	●	155	310	465	mA
	V_{EEGATE}	$V_{VEEGATE}$ = –7V	●	32	65	98	mA
Input/Output Pins							
$V_{ON, BD\_SEL\#(TH)}$	ON, BD_SEL# Pin Threshold Voltage	V_{ON} Rising, $V_{BD\_SEL\#}$ Rising	●	1.21	1.235	1.26	V
$\Delta V_{ON, BD\_SEL\#(HYST)}$	ON, BD_SEL# Pin Hysteresis		●	70	120	170	mV
$I_{BD\_SEL\#(UP)}$	BD_SEL# Pull-Up Current	$V_{BD\_SEL\#}$ = 0V	●	–7	–10	–16	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{5VIN} = 5V, V_{3VIN} = 3.3V, V_{VEEIN} = –12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{PB(TH)}$	Power Bad Threshold Voltage	$12V_{OUT}$ $5V_{OUT}$, V_{CFG} = 0V, Open $5V_{OUT}$ When V_{CFG} = V_{CC}, $3V_{OUT}$ V_{EEOUT}, V_{CFG} = 0V	● ● ● ●	10.8 4.5 2.8 –10.8	11.1 4.63 2.9 –11.1	11.4 4.75 3.0 –11.4	V V V V
$V_{IN(TH)}$	Logic Input Threshold	PGI, PCI_RST#, GPIO*n* SDA, SCL	● ●	0.8 1.6	1.0 1.8	1.2 2.0	V V
I_{IN}	Pin Input Current	ON, PGI, PCI_RST#, V = 1.2V SDA, SCL, ALERT#, GPIO*n*, HEALTHY#, LOCAL_PCI_RST#, V = 6V	●		0	±1	µA
V_{OL}	Output Low Voltage	SDA, ALERT#, I = 5mA; GPIO*n*, HEALTHY#, LOCAL_PCI_RST#, I = 3mA	●		0.2	0.4	V
$V_{TRI(H)}$	ADR2, ADR3, CFG Input High Threshold		●	V_{CC} –0.8	V_{CC} –0.4	V_{CC} –0.2	V
$V_{TRI(L)}$	ADR*n*, CFG Input Low Threshold		●	0.2	0.4	0.8	V
$I_{TRI(IN,HL)}$	ADR2, ADR3, CFG High, Low Input Current	V = 0V, V_{CC}	●			±80	µA
$I_{TRI(IN,Z)}$	ADR2, ADR3, CFG High Z Input Current	V = 0.8V, V_{CC} –0.8V	●	±10			µA
$I_{ADR01(IN)}$	ADR0, ADR1 Input Current	V_{ADR0}, V_{ADR1} = 0V, V_{CC}	●	–30		1	µA
I_{SENSE}	Sense Pin Input Current $12V_{SENSE}$, $5V_{SENSE}$, $3V_{SENSE}$ $V_{EESENSE}$	After Start-Up V_{SENSE} = V_{IN} $V_{VEESENSE}$ = –12V	 ● ●		 0.3 –30	 1 –45	 µA µA
$I_{OUT(ON)}$	OUT Pin Input Current	V_{12VOUT} = 12V, V_{ON} = 2V V_{5VOUT} = 5V, V_{ON} = 2V V_{3VOUT} = 3.3V, V_{ON} = 2V V_{VEEOUT} = –12V, V_{ON} = 2V	● ● ● ●		200 275 75 –200	280 390 105 –280	µA µA µA µA
$R_{OUT(DIS)}$	OUT Pin Discharge Resistance	V_{12VOUT} = 6V, V_{ON} = 0V V_{5VOUT} = 3V, V_{ON} = 0V V_{3VOUT} = 2V, V_{ON} = 0V V_{VEEOUT} = –6V, V_{ON} = 0V	● ● ● ●	650 125 130 1300	1000 180 190 1800	1800 325 340 3200	Ω Ω Ω Ω
$I_{VEEOUT(UP)}$	V_{EEOUT} Pull-Up Current	V_{VEEOUT} = 0V	●		–36	–54	µA
V_{PXG}	PRECHARGE Voltage	$I_{PRECHARGE}$ = Open, –70mA (Note 6)	●	0.95	1	1.05	V
Timer, Soft-Start							
$V_{TIMER(H)}$	TIMER Pin High Threshold	V_{TIMER} Rising	●	2.5	2.56	2.62	V
$V_{TIMER(L)}$	TIMER Pin Low Threshold	V_{TIMER} Falling	●	0.1	0.23	0.4	V
I_{TIMER}	TIMER Pin Pull-Up Current	During Start-Up, V_{TIMER} = 0V During PGI Timeout, V_{TIMER} = 0V During Auto-Retry, V_{TIMER} = 0V	● ● ●	–80 –8 –1.5	–100 –10 –2	–120 –12 –2.5	µA µA µA
$K_{TMRATIO}$	TIMER Pin Current Ratio	($I_{TIMER(RTRY)}/I_{TIMER(START)}$)	●	1.6	2	2.7	%
K_{TMCAP}	Start-Up Time per TIMER Capacitance	(($V_{TIMER(H)}$ – $V_{TIMER(L)}$)/$I_{TIMER(START)}$)	●	20	23.3	26	ms/µF
I_{SS}	SS Pin Pull-Up Current	Fast Ramp, V_{SS} = 0V Slow Ramp, V_{SS} = 2V	● ●	–16 –1.5	–20 –2	–24 –2.5	µA µA
$R_{TS(DIS)}$	TIMER, SS Discharge Resistance	V_{TIMER} = 1.2V, V_{SS} = 1.2V	●		225	400	Ω
G_{SS}	Gain from SS Pin to Foldback Current Limit ($\Delta V_{SNS(FB)}/\Delta V_{SS}$)	$12V_{IN}$, V_{EEIN} $5V_{IN}$, $3V_{IN}$			46 23		mV/V mV/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{5VIN} = 5V, V_{3VIN} = 3.3V, V_{VEEIN} = –12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC							
RES	Resolution (No Missing Codes)	(Note 7)	●	8			Bits
V_{FS}	Full-Scale Voltage (V_{FS} = 255LSB)						
	$12V_{IN}$, $12V_{OUT}$		●	13.744	14.025	14.306	V
	$12V_{IN} – 12V_{SENSE}$, $V_{EESENSE} – V_{EEIN}$	(Note 6)	●	62.47	63.75	65.03	mV
	$5V_{IN}$, $5V_{OUT}$	V_{CFG} = 0V, Open	●	5.5	5.61	5.72	V
		V_{CFG} = V_{CC}	●	3.75	3.825	3.9	V
	$5V_{IN} – 5V_{SENSE}$, $3V_{IN} – 3V_{SENSE}$		●	31.24	31.875	32.51	mV
	$3V_{IN}$, $3V_{OUT}$		●	3.75	3.825	3.9	V
	V_{EEIN}, V_{EEOUT}		●	–13.744	–14.025	–14.306	V
	GPIO		●	2.5	2.55	2.6	V
INL	Integral Nonlinearity	ΔV_{SENSE} (Note 8)	●		±0.5	±2	LSB
		Other 9 Channels	●		±0.2	±1.25	LSB
OE	Offset Error	ΔV_{SENSE} (Note 6)	●		±0.5	±1.5	LSB
		V_{EEIN}, V_{EEOUT}	●		±0.5	±1.25	LSB
		Other 7 Channels	●		±0.3	±1	LSB
FSE	Full-Scale Error		●			±5	LSB
TUE	Total Unadjusted Error		●			±5	LSB
t_{ADC}	Conversion Time	All 13 Channels Once			665		ms
		ΔV_{SENSE}, V_{EEIN}, V_{EEOUT}			70		ms
		Other 7 Channels			35		ms
Delays							
t_D	Turn-On Delay		●	60	100	150	ms
$t_{PLH(GATE)}$	Input High (ON) to Gates High Delay	SS Open	●		15	30	µs
$t_{PHL(GATE)}$	Input High (BD_SEL#), Input Low (ON) to Gates Low Propagation Delay	C_{GATE} = 1pF	●		0.3	1	µs
$t_{PHL(UVL)}$	Supply Low to Gates Low Delay	$12V_{IN}$, $5V_{IN}$, $3V_{IN}$, C_{GATE} = 1pF	●	2.1	3.5	4.9	µs
		V_{EEIN}, $C_{VEEGATE}$ = 1pF	●	3.3	5.5	7.7	µs
t_{CB}	Circuit Breaker Filter Delay Time		●	16	22	28	µs
t_{ACL}	Active Current Limit Delay	$\Delta V_{12VSENSE}$ = 300mV, $C_{12VGATE}$ = 10nF	●		0.9	2.3	µs
		$\Delta V_{5VSENSE}$ = 150mV, C_{5VGATE} = 10nF	●		0.85	2.1	µs
		$\Delta V_{3VSENSE}$ = 150mV, C_{3VGATE} = 10nF	●		0.7	1.8	µs
		$\Delta V_{VEESENSE}$ = 300mV, $C_{VEEGATE}$ = 10nF	●		2	5	µs
$t_{PHL(PGI)}$	PGI Low to Gates Low	C_{GATE} = 1pF	●	12	20	28	µs
$t_{PHL(RST)}$	Output Low to LOCAL_PCI_RST# Low	$12V_{OUT}$, $5V_{OUT}$, $3V_{OUT}$, $V_{PCI\_RST\#}$ = 2V	●	9	15	21	µs
		V_{EEOUT}, $V_{PCI\_RST\#}$ = 2V	●	10.2	17	23.8	µs
$t_{P(RST)}$	PCI_RST# to LOCAL_PCI_RST# Delay		●		60	200	ns
I^2C Interface Timing (Note 7)							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency	Operates with $f_{SCL} \le f_{SCL(MAX)}$		400			kHz
$t_{BUF(MIN)}$	Min. Bus Free Time Between Stop/Start				0.12	1.3	µs
$t_{SU,\ STA(MIN)}$	Minimum Repeated Start Set-Up Time				10	600	ns
$t_{HD,\ STA(MIN)}$	Min. Hold Time After (Repeated) Start				140	600	ns
$t_{SU,\ STO(MIN)}$	Minimum Stop Condition Set-Up Time				10	600	ns

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{SU, DAT(MIN)}$	Minimum Data Set-Up Time Input				0	100	ns
$t_{HD, DATI(MIN)}$	Minimum Data Hold Time Input				–100	0	ns
$t_{HD, DATO(MIN)}$	Minimum Data Hold Time Output			300	500	900	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width			50	110	250	ns
C_X	SCL, SDA Input Capacitance				5	10	pF
t_{of}	Data Output Fall Time	(Note 9)		20 + 0.1C_b		250	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: The $5V_{GATE}$ and $3V_{GATE}$ pins should not be driven beyond the lower of $12V_{IN}$ + 0.3V and 14V.

Note 4: An internal clamp limits the GATE pins to a minimum of 5V above V_{OUT} (V_{EEIN} for V_{EEGATE}). Driving this pin to voltages beyond the clamp may damage the device.

Note 5: The device pulls up the V_{EEOUT} pin to 0.6V when pin is in open state.

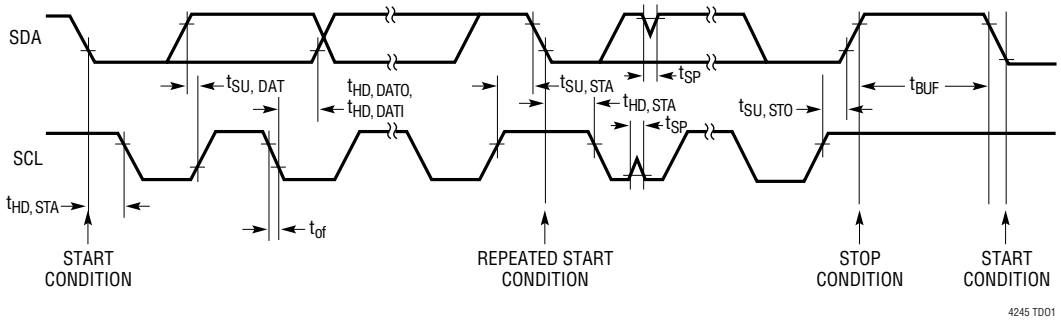
Note 6: UHF package specification limits are identical to G package limits and guaranteed by design and by correlation to wafer test measurements.

Note 7: Guaranteed by design and not subject to test.

Note 8: Integral Nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size and the single shot measurement. Typical specifications are measured from 1/4, 1/2, 3/4 areas of the quantization band.

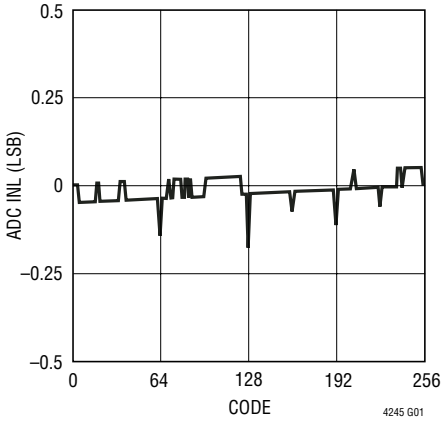
Note 9: C_b = total capacitance of one bus line in pF.

TIMING DIAGRAM

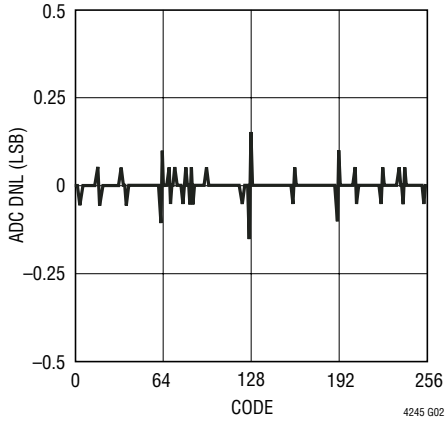


TYPICAL PERFORMANCE CHARACTERISTICS

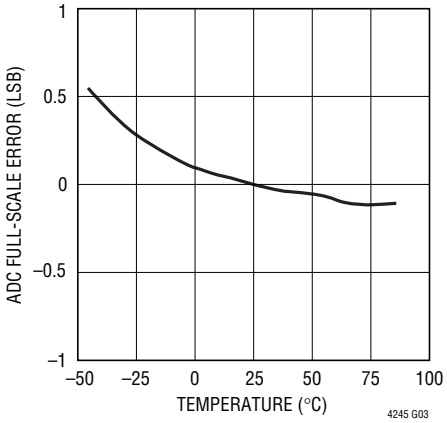
ADC INL vs Code (GPIO1 Pin)



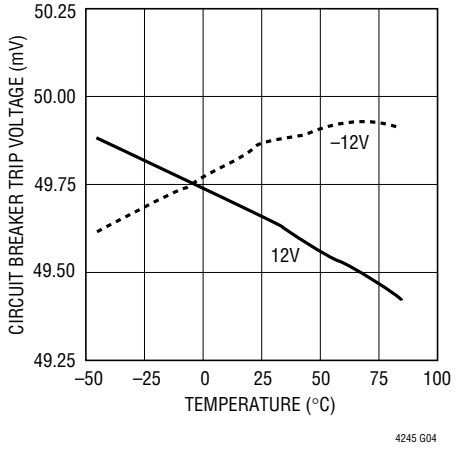
ADC DNL vs Code (GPIO1 Pin)



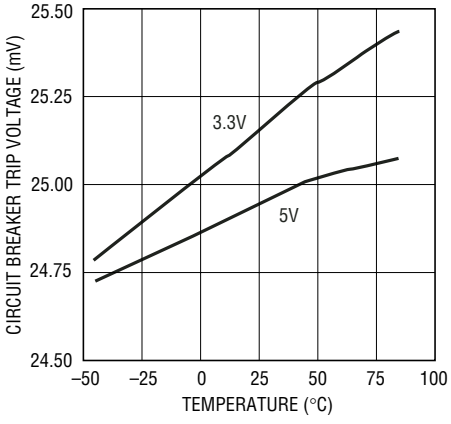
ADC Full-Scale Error vs Temperature (GPIO1 Pin)



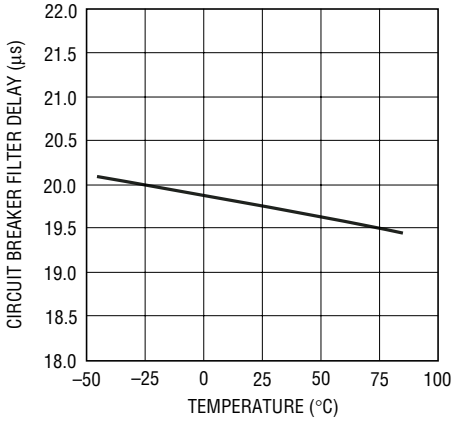
12V and –12V Circuit Breaker Trip Voltage vs Temperature



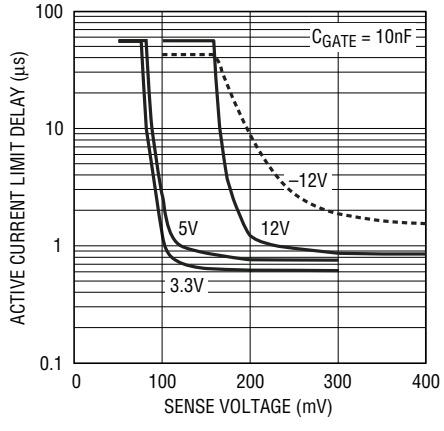
5V and 3.3V Circuit Breaker Trip Voltage vs Temperature



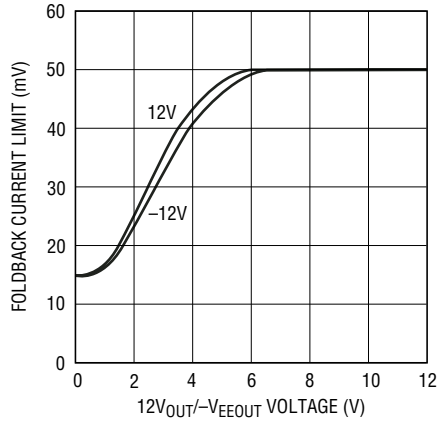
Circuit Breaker Filter Delay vs Temperature



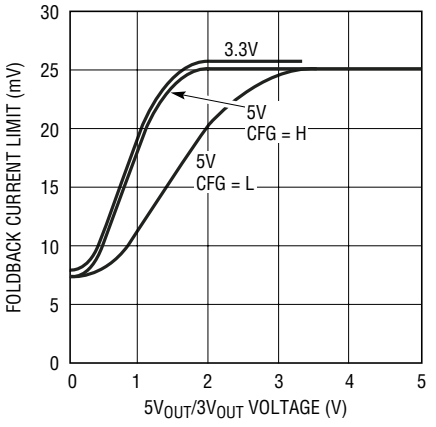
Active Current Limit Delay vs Sense Voltage



12V and –12V Foldback Current Limit vs Output Voltage

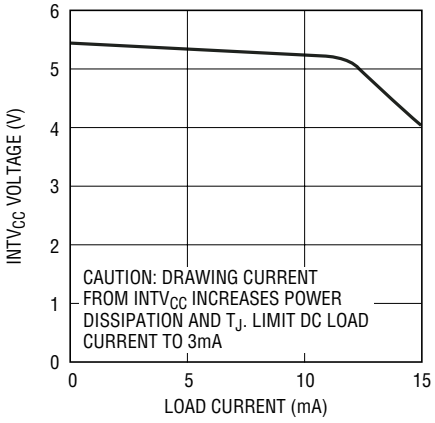


5V and 3.3V Foldback Current Limit vs Output Voltage

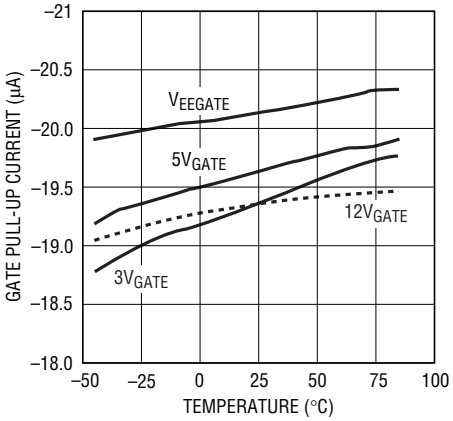


TYPICAL PERFORMANCE CHARACTERISTICS

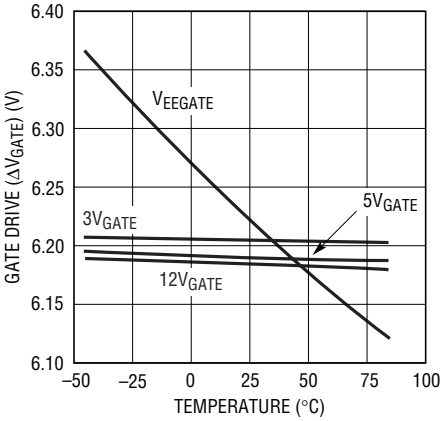
$INTV_{CC}$ Voltage vs Load Current



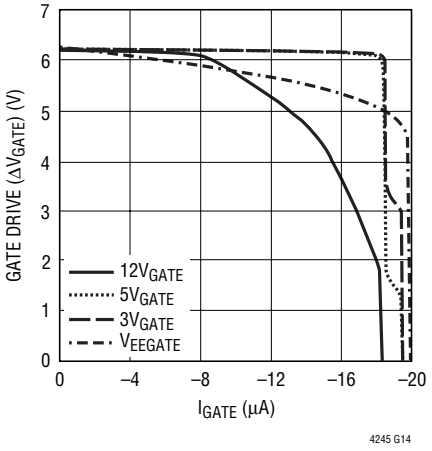
Gate Pull-Up Current vs Temperature



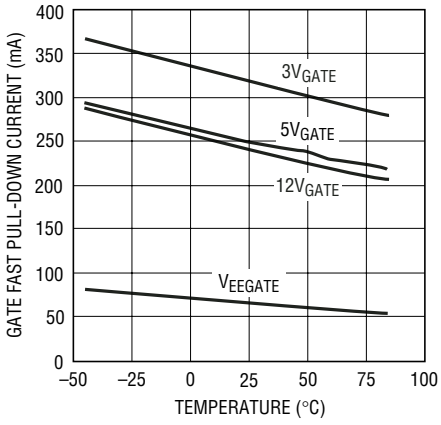
Gate Drive vs Temperature



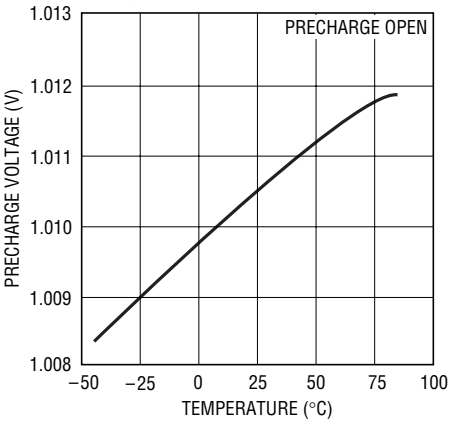
Gate Drive vs I_{GATE}



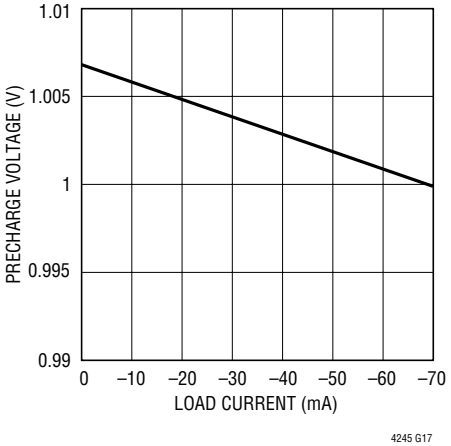
Gate Fast Pull-Down Current vs Temperature



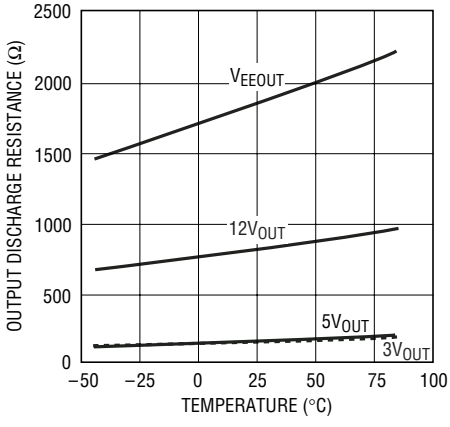
PRECHARGE Voltage vs Temperature



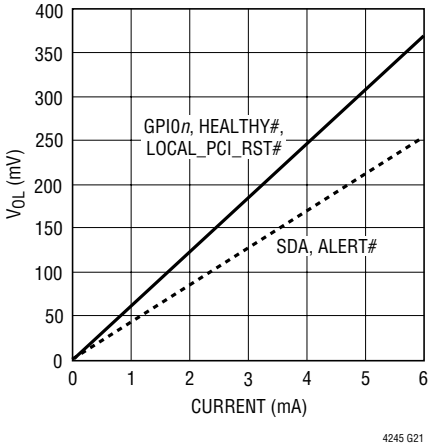
PRECHARGE Voltage vs Load Current



Output Discharge Resistance vs Temperature



V_{OL} vs Current



PIN FUNCTIONS

$12V_{GATE}$: Gate Drive for 12V Supply External N-Channel MOSFET. An internal 20μA current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above $12V_{OUT}$. During turn-off a 1.3mA pull-down current discharges $12V_{GATE}$ to ground. During short-circuit a 250mA pull-down current between $12V_{GATE}$ and $12V_{OUT}$ is activated.

$12V_{IN}$: 12V Supply, Current Sense and ADC Input. The internal low voltage supply V_{CC} is generated from $12V_{IN}$. An undervoltage lockout circuit, with 38mV hysteresis, prevents any external MOSFET from turning on when this pin is below 10.5V.

$12V_{OUT}$: 12V Gate Drive Return; Foldback, ADC and Power Bad Input. Connect this pin to the source of the 12V supply external N-channel MOSFET switch for gate drive return. Power is considered bad if this pin drops below 11.1V. The comparator on this pin has a built-in hysteresis of 40mV. This pin is also an input to the ADC and the current limit foldback circuit. A 1000Ω active pull-down discharges $12V_{OUT}$ to ground when the external MOSFET is turned off.

$12V_{SENSE}$: 12V Supply Current Sense and ADC Input. Connect this pin to the output of the 12V current sense resistor. The current limit circuit controls the $12V_{GATE}$ pin to limit the sense voltage between the $12V_{IN}$ and $12V_{SENSE}$ pins to 50mV or less during start-up and 150mV thereafter. During start-up a foldback feature reduces the current limit to 15mV as the $12V_{OUT}$ pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 50mV for 22μs. To disable current limit, connect this pin to $12V_{IN}$.

$3V_{GATE}$: Gate Drive for 3.3V Supply External N-Channel MOSFET. An internal 20μA current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above $3V_{OUT}$. During turn-off a 1.3mA pull-down current discharges $3V_{GATE}$ to ground. During short-circuit a 310mA pull-down current between $3V_{GATE}$ and $3V_{OUT}$ is activated.

$3V_{IN}$: 3.3V Supply, Current Sense and ADC Input. The 1V precharge circuit draws its power and reference voltage from $3V_{IN}$. An undervoltage lockout circuit, with 10mV hysteresis, prevents any external MOSFET from turning on when this pin is below 2.8V.

$3V_{OUT}$: 3.3V Gate Drive Return; Foldback, ADC and Power Bad Input. Connect this pin to the source of the 3.3V supply external N-channel MOSFET switch for gate drive return. Power is considered bad if this pin drops below 2.9V. The comparator on this pin has a built-in hysteresis of 11mV. This pin is also an input to the ADC and the current limit foldback circuit. A 190Ω active pull-down discharges $3V_{OUT}$ to ground when the external MOSFET is turned off.

$3V_{SENSE}$: 3.3V Supply Current Sense and ADC Input. Connect this pin to the output of the 3.3V current sense resistor. The current limit circuit controls the $3V_{GATE}$ pin to limit the sense voltage between the $3V_{IN}$ and $3V_{SENSE}$ pins to 25mV or less during start-up and 75mV thereafter. During start-up a foldback feature reduces the current limit to 7.5mV as the $3V_{OUT}$ pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 25mV for 22μs. To disable current limit, connect this pin to $3V_{IN}$.

$5V_{GATE}$: Gate Drive for 5V Supply External N-Channel MOSFET. An internal 20μA current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above $5V_{OUT}$. During turn-off a 1.3mA pull-down current discharges $5V_{GATE}$ to ground. During short-circuit a 250mA pull-down current between $5V_{GATE}$ and $5V_{OUT}$ is activated.

$5V_{IN}$: 5V Supply, Current Sense and ADC Input. An undervoltage lockout circuit, with 16mV or 10mV of hysteresis, prevents any external MOSFET from turning on when this pin is below 4.38V or 2.8V depending on the state of the CFG pin.

PIN FUNCTIONS

$5V_{OUT}$: 5V Gate Drive Return; Foldback, ADC and Power Bad Input. Connect this pin to the source of the 5V supply external N-channel MOSFET switch for gate drive return. Power is considered bad if this pin drops below 4.63V or 2.9V depending on the CFG pin. The comparator on this pin has a built-in hysteresis of 17mV or 11mV. This pin is also an input to the ADC and the current limit foldback circuit. A 180Ω active pull-down discharges $5V_{OUT}$ to ground when the external MOSFET is turned off.

$5V_{SENSE}$: 5V Supply Current Sense and ADC Input. Connect this pin to the output of the 5V current sense resistor. The current limit circuit controls the $5V_{GATE}$ pin to limit the sense voltage between the $5V_{IN}$ and $5V_{SENSE}$ pins to 25mV or less during start-up and 75mV thereafter. During start-up a foldback feature reduces the current limit to 7.5mV as the $5V_{OUT}$ pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 25mV for 22μs. To disable current limit, connect this pin to $5V_{IN}$.

ADR0 to ADR3: Serial Bus Address Inputs. ADR0 and ADR1 are two-state inputs; ADR2 and ADR3 are three-state inputs. Tying these pins to ground, open or $INTV_{CC}$ configures one of 32 possible addresses. The addressing scheme is compatible with the CompactPCI geographic addressing for slot identification. See Table 5 in Applications Information.

ALERT#: Fault Alert Output. Open-drain logic output that can be pulled to ground, when a fault occurs, to alert the host controller. A fault alert is enabled by the ALERT register. This device is compatible with SMBus alert protocol. See Applications Information. Tie to ground if unused.

BD_SEL#: Board Present Input. Ground this pin to enable the N-channel MOSFETs to turn on. When this pin is high, the MOSFETs are off. An internal 10μA current source pulls up this pin to $INTV_{CC}$. Transitions on this pin will be recorded in the FAULT2 register. A high-to-low transition activates the logic to read the state of the ON pin and clear faults. See Applications Information.

CFG: Supply Configuration Three-State Input. When this pin is grounded, all four supply inputs must satisfy their undervoltage lockout levels to allow the external MOSFETs to turn on. Floating this pin disables V_{EE} undervoltage lockout and power bad functions, allowing other supplies to turn-on even when –12V supply is absent. Tying this pin to $INTV_{CC}$ not only disables V_{EE}, but also converts the $5V_{IN}$ undervoltage, power bad and ADC levels to 3.3V levels. This allows using an extra 3.3V supply instead of a 5V supply as in a PCI Express application.

EXPOSED PAD (Pin 39, UHF Package): Exposed Pad may be left open or connected to device ground.

GND: Device Ground.

GPIO1 to GPIO3 (GPIO2, GPIO3 on UHF package only): General Purpose Input/Output and ADC Input. Open-drain logic outputs and logic inputs. Any one of the three pins can be multiplexed to the GPIO channel of the internal ADC. GPIO1 has a state change fault associated with it. The GPIO register (Table 13) contains status and control bits for these pins.

HEALTHY#: Board Power Status Output. This pin is pulled low by an open-drain output when all supply outputs are above their power bad thresholds and when all external N-channel MOSFETs are on. When any supply output falls below its power bad threshold voltage, this pin will go high after a 15μs deglitching time.

$INTV_{CC}$: Internal Low Voltage Supply Decoupling Output. Connect a 0.1μF capacitor from this pin to ground. When this pin falls below 3.8V, the internal registers are reset.

LOCAL_PCI_RST#: Reset Output. This pin is pulled low by an open-drain output whenever HEALTHY# is high or when the PCI_RST# input is low. Tie to ground if unused.

ON: On Control Input. A rising edge turns on the external N-channel MOSFETs and a falling edge turns them off. This pin is also used to configure the state of the FET On control bits (and hence the external FETs) in the ON register. For example, if the ON pin is tied high, then one or all (depending on the Sequence control bit) FET On control bits will go high 100ms after power-up. Likewise if the ON pin is tied low then the part will remain off after power-up until the FET On control bits are set high using the I^2C bus. If the Sequence control bit is set, taking ON pin high turns on the supplies in a 12V, 5V, 3.3V, –12V sequence. A high-to-low transition on this pin will clear faults.

PIN FUNCTIONS

PCI_RST#: Reset Input. Pulling this pin low causes LOCAL_PCI_RST# to pull low. When high, LOCAL_PCI_RST# is the logical inverse of HEALTHY#. Tie to $INTV_{CC}$ if unused.

PGI: Power Good Input. Tie this pin to the $\overline{RESET}$ output of an external supply monitor or power good output of a DC/DC converter. When all supplies have been turned on, a timing cycle is started at the end of which the PGI pin is sampled. If it is low, all external MOSFETs are shut off. If the PGI Disable control bit C3 is not set, pulling this pin low for more than 20μs during normal operation will also shut off all MOSFETs. Tie to $INTV_{CC}$ if unused.

PRECHARGE: Bus Precharge Output. This pin can source 70mA at 1V as soon as $3V_{IN}$ is powered-up. Leave it open if unused.

SCL: Serial Bus Clock Input. Data at the SDA pin is shifted in or out on rising edges of SCL. This is a high impedance pin that is generally driven by an open-collector output from a master controller.

SDA: Serial Bus Data Input and Output. This is a high impedance input when address, command or data bits are shifted in. It is an open-drain output when sending data back to the master controller or acknowledging a write operation. An external pull-up resistor or current source is required.

SS: Soft-Start Input. Connect a capacitor between this pin and ground to set the rate of increase of current limit during start-up for dI/dt limited inrush current. When an external MOSFET is turned on, a 20μA pull-up current charges the capacitor. The voltage ramp on the capacitor is converted into an internal current limit increasing linearly with time. Leave it open if dI/dt limited inrush is not required.

TIMER: Timer Input. A capacitor between this pin and ground sets the duration of the start-up, PGI and auto-retry timing cycles to be 23.3ms/μF, 233ms/μF and 1.17s/μF respectively. A timing cycle consists of TIMER being charged to 2.56V with an internal pull-up current source and then being reset by a switch to ground. The timing cycle ends when TIMER falls below 0.23V. The start-up, PGI and auto-retry timing cycles use 100μA, 10μA and 2μA pull-up current sources respectively.

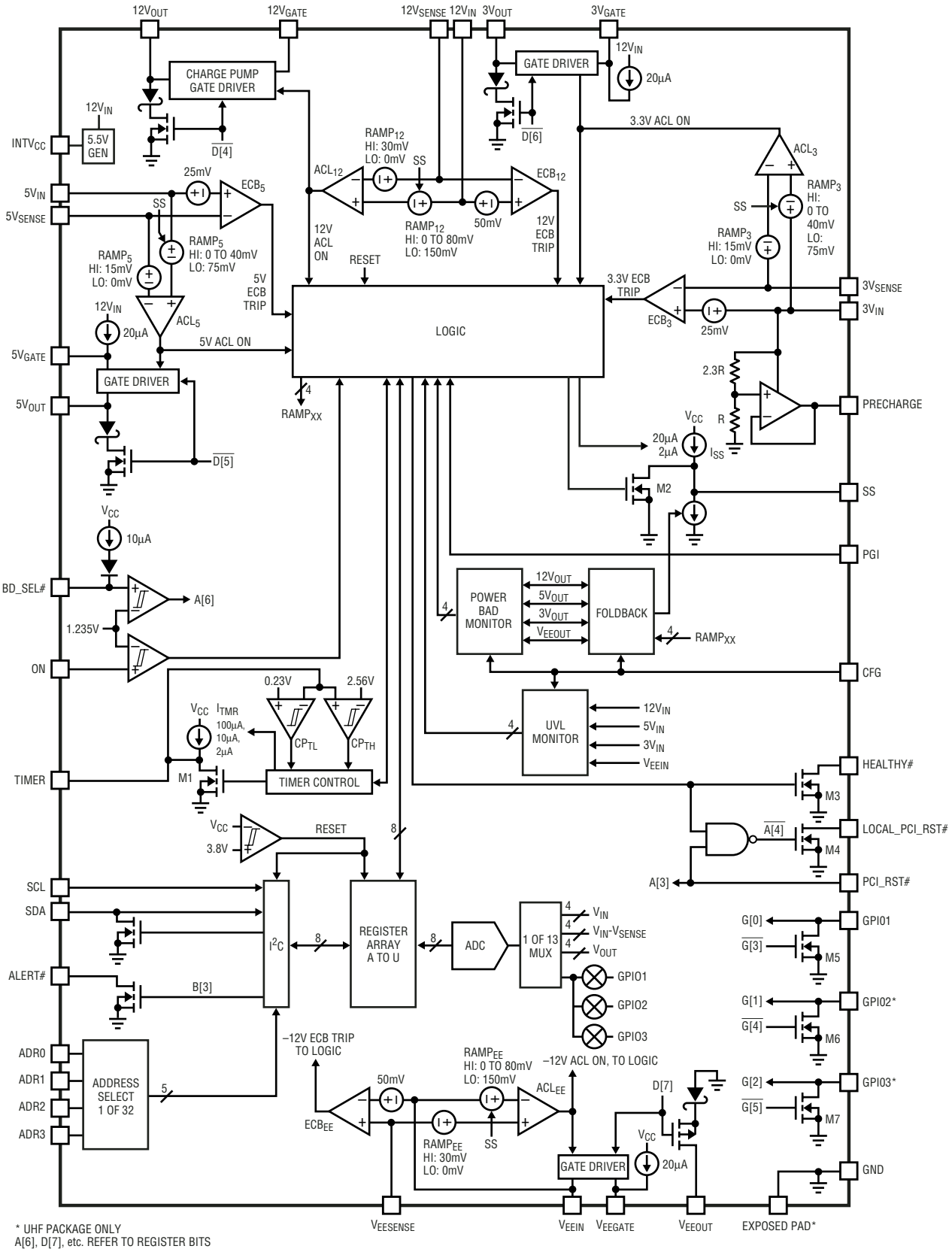
V_{EEGATE}: Gate Drive for –12V Supply External N-Channel MOSFET. An internal 20μA current source charges the gate of the external N-channel MOSFET. An internal clamp limits the gate voltage to 6.2V above V_{EEIN}. During turn-off, a 3.5mA pull-down current discharges V_{EEGATE} to V_{EEIN}. During short-circuit a 65mA pull-down current between V_{EEGATE} and V_{EEIN} is activated. If a –12V supply is not available, connect V_{EEGATE} to ground and use the CFG pin appropriately.

V_{EEIN}: –12V Supply, Current Sense and ADC Input. An undervoltage lockout circuit, with 38mV hysteresis, prevents any external MOSFET from turning on when this pin is above –10.5V. The V_{EEIN} undervoltage lockout can be disabled by using the CFG pin. If a –12V supply is not available, connect V_{EEIN} to ground and use the CFG pin appropriately.

V_{EEOUT}: –12V Supply Foldback, ADC and Power Bad Input. Connect this pin to the drain of the –12V supply external N-channel MOSFET switch. Power is considered bad if this pin rises above –11.1V. The comparator on this pin has a built-in hysteresis of 54mV. The V_{EEOUT} power bad function can be disabled by using the CFG pin. This pin is also an input to the ADC and the current limit foldback circuit. A 1800Ω active pull-up discharges V_{EEOUT} to ground when the external MOSFET is turned off. If a –12V supply is not available, connect V_{EEOUT} to ground and use the CFG pin appropriately.

$V_{EESENSE}$: –12V Supply Current Sense and ADC Input. Connect this pin to the output of the –12V current sense resistor. The current limit circuit controls the V_{EEGATE} pin to limit the sense voltage between the $V_{EESENSE}$ and V_{EEIN} pins to 50mV or less during start-up and 150mV thereafter. During start-up a foldback feature lowers the current limit to 16mV as the V_{EEOUT} pin approaches ground. A circuit breaker, enabled after start-up, trips when the sense voltage exceeds 50mV for 22μs. To disable current limit, connect this pin to V_{EEIN}. If a –12V supply is not available, connect $V_{EESENSE}$ to ground and use the CFG pin appropriately.

BLOCK DIAGRAM



* UHF PACKAGE ONLY
A[6], D[7], etc. REFER TO REGISTER BITS

OPERATION

Start-Up

The LTC4245 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane slot. When a supply turn-on command is received, current sources start pulling up the TIMER and SS pins. The 100μA I_{TMR} current and the external TIMER capacitor determine the time a supply can be in current limit during start-up. The gate of a supply's external N-channel MOSFET is servoed by an amplifer (ACL_n) so that the current, as indicated by the sense resistor voltage drop, never exceeds an internal current limit. This current limit rises at a rate determined by I_{SS} and the capacitor at the SS pin. A foldback circuit determines the maximum value of the current limit and reduces it to 30% of the maximum when a supply's output is shorted to ground. When the TIMER pin crosses 2.56V it is reset to ground and the start-up timing cycle ends. If a supply is still in current limit all gates are turned off, an overcurrent fault is logged and the TIMER goes through a cool-down timing cycle using 2μA for I_{TMR}. Otherwise, its circuit breaker (ECB_n) is armed and the current limit is raised to 3 times the circuit breaker threshold. The SS pin is then reset by switch M2.

Any combination of the four supplies can be turned on together or one after another. Whenever a supply is ramping up, its output voltage will affect, through the foldback circuit, where the internal current limit ramp stops. The default configuration turns on all supplies together. If sequence control bit C6 (Table 9) is set, the supplies turn on in a 12V, 5V, 3.3V, –12V sequence. With this bit set, the end of a supply ramp-up triggers the start of the next one in the sequence. The I^2C interface allows independent on and off control for each supply through its On control bit. Turn-off is simultaneous under fault conditions and when using the ON or BD_SEL# pins.

At the end of the last start-up timing cycle, HEALTHY# is pulled low by M3 if all supply outputs are above their power bad thresholds. LOCAL_PCI_RST# which was held low (M4), now follows PCI_RST#. The TIMER pin goes through a PGI timeout cycle using 10μA for I_{TMR}. The PGI pin is sampled at the end of the cycle. If it is low, then all external MOSFETs are shut-off, a PGI fault is logged and TIMER goes through a cool-down cycle using 2μA for I_{TMR}. If PGI is high, the part enters the normal mode of operation.

Normal Operation

During normal operation, the gates of the MOSFETs are clamped about 6.2V above their sources. The 12V gate driver uses a charge pump, the 5V and 3.3V gate drive is derived from $12V_{IN}$ and the –12V gate drive from $INTV_{CC}$. Each supply is continuously monitored for undervoltage, overcurrent and power bad conditions. Overcurrent monitoring consists of an electronic circuit breaker comparator (ECB_n) and an active current limit circuit (ACL_n) set at 3x the ECB threshold. Undervoltage and overcurrent faults cause all MOSFETs to be shut off. A power bad condition causes HEALTHY# to go high impedance and LOCAL_PCI_RST# to pull low, without shutting off the MOSFETs. If the PGI pin is not disabled (register bit C3 not set), then PGI pin going low will also shut off all MOSFETs.

ADC

Included in the LTC4245 is an 8-bit A/D converter. The converter has a 13-input multiplexer to select between input, output and current sense voltage of each supply, and the GPIO channel. The ADC can either cycle through all channels or measure a channel on-demand.

Serial Interface

An I^2C interface is provided to read from or write to the status, control and A/D registers. It allows the host to poll the device and determine if faults have occurred. If the ALERT# line is used as an interrupt, the host can respond to a fault in real time. The LTC4245 I^2C interface slave address is decoded using the ADR0 to ADR3 pins.

Configuration, GPIO and Precharge

The three-state CFG pin can be used to disable the V_{EE} undervoltage lockout, power bad and foldback functions. It can also convert the 5V undervoltage, power bad and ADC levels to 3.3V levels. The GPIO1 to GPIO3 pins can be used as general purpose inputs or outputs (M5 to M7). One of the pins can also be multiplexed to the GPIO channel of the ADC. A 1V reference voltage derived from $3V_{IN}$ is provided at the PRECHARGE pin. This can be used to pre-charge I/O lines on the board so as not to corrupt the backplane bus.

APPLICATIONS INFORMATION

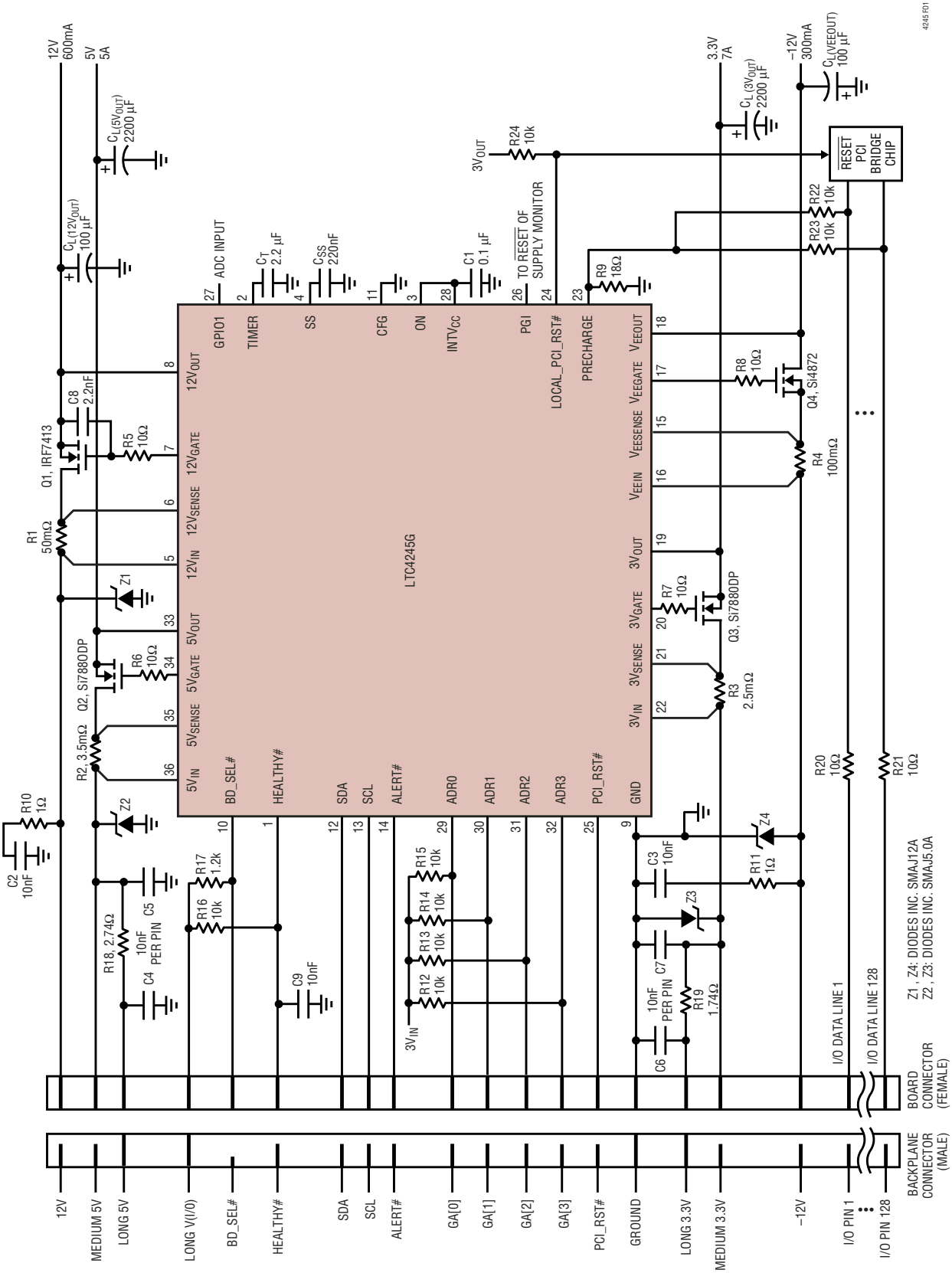


Figure 1. CompactPCI Application

APPLICATIONS INFORMATION

The typical LTC4245 application is in a high availability system where boards using multiple supplies are hot plugged. The device enables the system to periodically monitor board power consumption and fault status over the I^2C interface. Boards in CompactPCI and PCI Express systems typically utilize three to four supplies. Figure 1 shows the LTC4245 being used in a CompactPCI application.

The following sections describe the turn on, turn off and fault response behavior of the LTC4245. The ADC and I^2C interface are discussed next. External component selection is discussed in detail in the Design Example section.

CPCI Connection Pin Sequence

The staggered lengths of the CPCI male connector pins on the backplane ensures that all power supplies are physically connected to the LTC4245 before back-end power is allowed to ramp up (BD_SEL# asserted low). The long pins, which include 5V, 3.3V, V(I/O) and GND, mate first. The short BD_SEL# pin mates last. At least one long 3.3V power pin must be connected to the LTC4245 in order for the PRECHARGE pin voltage to be available before the CPCI bus pins mate.

The following is a typical hot plug sequence.

1. ESD clips make contact.
2. Long power and ground pins make contact and Early Power is established. The 1V precharge voltage becomes valid at this stage. Power is also applied to the pull-up resistors connected to the HEALTHY# and BD_SEL# signals. LOCAL_PCI_RST# is held in reset. All power switches are held off at this stage of insertion.
3. Medium length pins make contact. The 12V and –12V connector pins make contact at this stage. The internal low voltage supply of the LTC4245 ($INTV_{CC}$) powers up from the 12V supply. An internal 10μA pull-up from $INTV_{CC}$ to BD_SEL# turns on. Other connector pins that mate are HEALTHY#, PCI_RST# and the bus I/O pins (which are precharged to 1V).
4. Short pins make contact. If the BD_SEL# signal is grounded on the backplane, the plug-in board power-up cycle may begin immediately. If the ON pin is tied high then turn-on is automatic, else the LTC4245 waits for a serial bus turn-on command. System backplanes that do not ground the BD_SEL# signal will instead have circuitry that detects when BD_SEL# makes contact with the plug-in board. The system logic can then control the power up process by pulling BD_SEL# low. The precharge potential may be optionally disconnected from the CPCI bus signals at this stage.

Turn-On

The back-end power planes are isolated from the input power planes by external N-channel pass transistors Q1 through Q4. Sense resistors R1 to R4 provide current fault detection. Resistors R5 to R8 prevent high frequency oscillations in MOSFETs Q1 to Q4 respectively.

The following conditions must be satisfied for a duration of 100ms before the external switches can be turned on.

1. All input supplies and the internally generated supply, $INTV_{CC}$, must exceed their undervoltage lockout thresholds. The V_{EE} undervoltage lockout can be disabled by not tying the CFG pin low.
2. No undervoltage, overcurrent or PGI fault bits must be set unless the corresponding auto-retry is enabled. When $12V_{IN}$ powers up for the first time, $INTV_{CC}$ rises above its undervoltage threshold which generates a 60μs to 120μs internal power-on-reset pulse. During reset, the fault registers are cleared and the control bits are initialized. If $INTV_{CC}$ is already up, then the I^2C interface can be used to clear the fault bits or set the auto-retry bits.
3. The BD_SEL# pin must be pulled low.

When these initial conditions are satisfied, the ON pin is checked. If it is high, the four FET On control bits (D0 to D3) are set either simultaneously (the default state) or in a 12V, 5V, 3.3V, –12V sequence (register bit C6 set). If ON is low, the external switches turn on when the ON pin is brought high or if a serial bus turn-on command is received. Figure 2 shows all supplies turning on after BD_SEL# goes low.

APPLICATIONS INFORMATION

When a switch is to be turned on, an internal 100μA current source is connected to the TIMER pin and a 20μA current to SS pin. The gate of each ramping supply's pass transistor is servoed by an internal amplifier, so the supply current never exceeds an internal current limit. This internal current limit starts off with a negative value, which makes the amplifier pull the gate low. The voltage ramp on the SS pin is converted to a current limit rising linearly with time. The amplifier releases the gate as the current limit crosses zero. An internal current source starts charging up the gate. When the gate voltage reaches the MOSFET threshold voltage, the switch begins to turn on. The amplifier once again starts modulating the gate pull-up current so that the sense resistor voltage drop follows the internally set current limit. The rate of rise of the inrush current is given by:

$$\frac{dI_{INRUSH}}{dt} = \frac{G_{SS}}{R_{SENSE}} \bullet \frac{dV_{SS}}{dt} \quad (1)$$

$$\frac{dV_{SS}}{dt} = \frac{I_{SS}}{C_{SS}} \quad (2)$$

G_{SS} is the ratio of the change in current limit to the change in SS pin voltage. The rising current limit will stop at a level depending on the foldback circuit. The foldback circuit monitors the outputs of all supplies which are ramping. In the worst case, a supply output could be shorted to ground. In this case the foldback circuit reduces the current limit to 30% of the maximum as shown in the Typical Performance Curves. To set an inrush current lower than the foldback level, a series R-C network can be connected between the gate pin and ground (V_{EEOUT} for –12V supply) (Figure 3). This allows charging the output load beyond the time dictated by the TIMER capacitor. When the rising internal current limit exceeds the dV/dt set inrush current, the current limit amplifier goes open loop. If any ramping supply's amplifier is open loop the SS pin current drops to 2μA from 20μA, thus slowing the current limit rise. This would affect the other supplies ramp-up in case of simultaneous turn-on. A 100kΩ resistance ensures that the capacitor charge is decoupled during a fast gate turn-off. The capacitor value is determined by:

$$C_{GATE} = \frac{I_{GATE(UP)}}{I_{INRUSH}} \bullet C_{LOAD} \quad (3)$$

Meanwhile the TIMER pin ramps up to 2.56V, when it is reset to ground. Current limit faults on the ramping supplies are ignored during this time period. The start-up timing cycle ends when the TIMER pin falls below 0.23V. The SS pin is reset, the circuit breaker for the supply is armed and its current limit raised to 3x the circuit breaker threshold. In a sequenced turn-on the part will start another TIMER and SS cycle to ramp up the next supply. If supplies are being turned on through the serial bus, it will wait for the next turn-on command.

Once all supplies have been turned on and all their outputs are within tolerance, HEALTHY# will pull low and LOCAL_PCI_RST#, which was low, will now follow PCI_RST#. The TIMER pin is now pulled up by a 10μA current source while SS pin remains in reset. When TIMER reaches 2.56V, it is reset to ground. As it crosses 0.23V the PGI pin is sampled. If it is low then all switches are turned off.

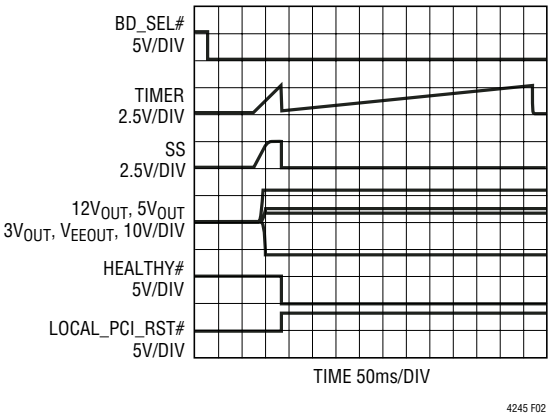


Figure 2. Normal Turn-On Waveform

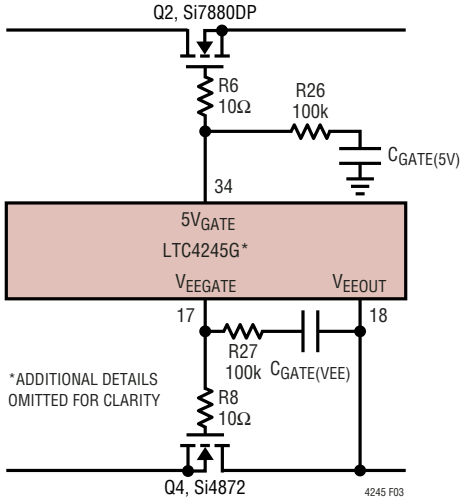


Figure 3. C_{GATE} for dV/dt Limited Inrush Current

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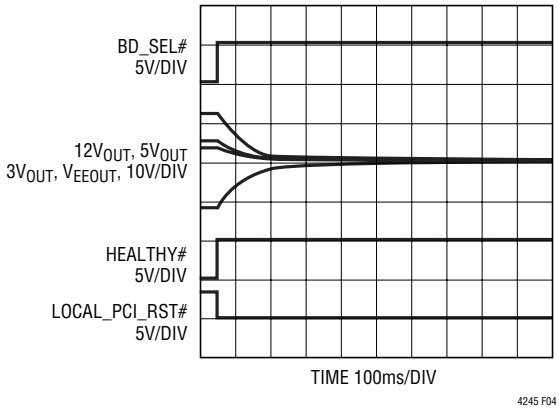

Figure 4. Normal Turn-Off Waveform

Turn-Off

The switches can be turned off by a variety of conditions.

1. ON pin going low or BD_SEL# going high turns off all switches.
2. Individual switches can be turned off by resetting the particular FET On control bit (D0 to D3) through the serial bus.
3. A variety of fault conditions will turn off all switches together. These include supply undervoltage, overcurrent circuit breaker and PGI faults.
4. Writing a logic one into the undervoltage, overcurrent or PGI fault bits will turn off all switches, if the corresponding autoretry is not enabled.

Normally the 12V, 5V and 3.3V switches are turned off with a 1.3mA current pulling down the gate to ground. V_{EEGATE} is pulled through a resistive switch to V_{EEIN}. All supply outputs are also discharged to ground through internal switches. When any MOSFET is shut off, the HEALTHY# signal pulls high and LOCAL_PCI_RST# will be asserted low. Figure 4 shows all supplies being turned off by BD_SEL# going high.

ON Register and Sequencing

The LTC4245 features an ON register (Table 10) consisting of four On control bits (D0 to D3) and four On status bits (D4 to D7). D0 to D3 provide independent on/off control for each supply through the I^2C bus. Bits D4 to D7 report the on status of each supply. Even though a supply may be commanded to turn-on by setting its On control bit, it may remain off (On status bit low) because the conditions to turn on, as listed in the Turn-On section, may not be present.

The sequence control bit, C6, determines whether the four supply MOSFETs turn-on together or in a fixed sequence. The default state is no sequencing. In this case taking the ON pin high sets all the four On control bits. If the start-up conditions are satisfied, all switches will turn on under the control of a single TIMER and SS cycle. Due to different input voltage offsets in the current limit amplifier of each supply, the gate turn-on of all MOSFETs will not occur at the same moment but will happen in random order depending on amplifier offset and soft-start ramp rate. The gate turn-ons will be truly simultaneous only if SS pin is left open.

If bit C6 is set, then the ON pin going high sets only the 12V On control bit, D0. The 12V back-end supply ramps up. The end of the TIMER and SS cycle sets the 5V On control bit, D1, starting the ramp of the 5V supply output. The end of the 5V timing cycle sets bit D2 and the end of the 3.3V ramp sets bit D3. In this way, the four On control

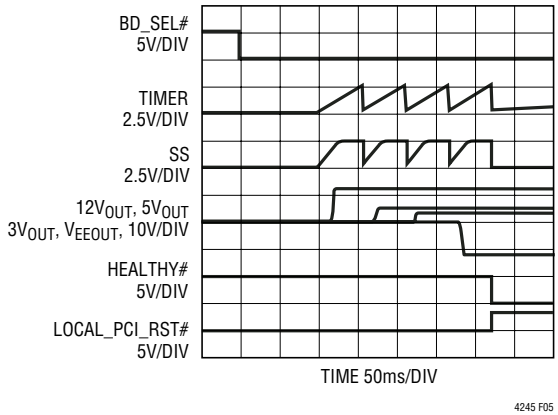

Figure 5. Sequential Turn-On Waveform

bits get set one after another, leading to a 12V, 5V, 3.3V, –12V start-up sequence. Figure 5 illustrates this. If C6 is set and any of the start-up conditions goes bad, all switches turn-off, and all On control bits except D0 are reset. This ensures that the part goes through a sequenced turn-on during auto-retry. D1 to D3 are also reset when BD_SEL# goes low with C6 set.

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When the sequence bit C6 is set, setting the On control bit of a supply, through the I^2C interface, starts the supply turn-on sequence from that supply onwards. For example, setting bit D1 will turn-on 5V, 3.3V, –12V supplies, in that order. A logic one can then be written to bit D0 to ramp the 12V supply. At the end of this ramp-up, bit D1 is set. But since 5V is already powered-up, the sequence stops there.

The I^2C interface provides the most flexibility in turning supplies on and off. With bit C6 cleared, any supply or supplies can be turned on by setting their On control bits. The On control bits cannot be set when any supply is ramping (therefore using TIMER and SS pins). The SS busy bit, A1, indicates this blanking period. The On control bits can be reset though, even when a supply is ramping. Two or more On control bits may be set at the same time to ramp multiple supplies in the same timing cycle. When all supplies are turned on the LTC4245 goes through the PGI timing cycle.

Supply Voltage Configuration

The CFG pin enables the LTC4245 to be used in non-CPCI applications. It is a three-state input pin. In a CPCI application with all four supplies, the CFG pin is tied to ground.

Floating the CFG pin disables the V_{EE} undervoltage lockout (UVLO), start-up foldback and power bad functions. It also makes the ±12V turn-ons coincident by using the 12V FET On control bit, D0, to control the –12V supply MOSFET. This allows the three positive supplies to power-up and HEALTHY# to assert, even when a negative supply is either unavailable or does not meet the required thresholds. If unused the V_{EEIN}, $V_{EESENSE}$, V_{EEGATE} and V_{EEOUT} pins should be tied to ground. Since the circuit breaker and active current limit circuits are not disabled, a lower negative supply could be hot plugged. It would turn on whenever the 12V supply turns on. Care should be taken that the supply does not collapse under overcurrent conditions. At low supplies, the ECB and ACL circuits stop functioning. With the UVLO already disabled, the LTC4245 may not detect a fault condition on the V_{EE} supply. Large currents, limited only by MOSFET and sense resistances, could flow, potentially damaging the board traces and connector pins.

If the CFG pin is tied high, the 5V supply thresholds change to 3.3V levels, while keeping the floating state functionality. The 5V supply UVLO, power bad thresholds and foldback profile become similar to those of the 3.3V supply. The $5V_{IN}$ and $5V_{OUT}$ inputs to the ADC use the same LSB and full-scale as the $3V_{IN}$ and $3V_{OUT}$ pins. This allows the use of an extra 3.3V supply instead of a 5V supply as in a PCI Express application.

Overcurrent Fault

The LTC4245 has different current limiting behavior during start-up, when supply ramps up under TIMER and SS control, and normal operation. As such it can generate an overcurrent fault during both phases of operation. Both set the faulting supply's overcurrent fault bit (bits E4 to E7) and shut off all external FETs.

During start-up when both TIMER and SS are ramping, the current limit is a function of SS pin voltage and the ramping supplies' output voltages. A supply could power up entirely in current limit depending on the bypass capacitor at the outputs of the ramping supplies. The TIMER pin sets the time duration for current limit during start-up. This time involves the TIMER charging up to 2.56V with a 100µA current source and then resetting to 0.23V with a switch. At the end of the timing cycle if the supply is still in current limit, i.e., the gate of it's external MOSFET is still being actively controlled, an overcurrent fault is declared for that supply and all MOSFETs are shut off (Figure 6). Therefore the maximum time a supply can stay in current limit at start-up is given by:

$$t_{START} = C_T \bullet K_{TMCAP} = C_T \bullet 23.3\ \left[ms/\mu F\right] \quad (4)$$

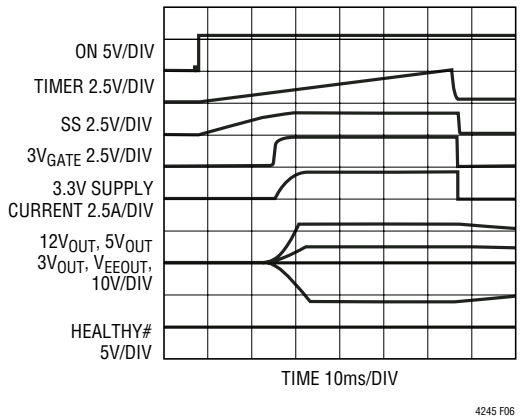

Figure 6. Start-Up Into a Short on 3.3V Output

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After the switches are turned off, the TIMER pin begins charging up with a 2μA pull-up current. When it reaches 2.56V it is reset to ground with a switch. During this cool-down cycle, the overcurrent fault bit cannot be reset. After this cycle, the switches will be allowed to turn on again if the overcurrent fault bit is cleared. However, if the overcurrent autoretry bit, C1, has been set then the switches turn on again automatically after the 100ms turn-on delay (without resetting the overcurrent fault).

After start-up, a supply has dual-level glitch-tolerant protection against overcurrent faults. The sense resistor voltage drop is monitored by an electronic circuit breaker (ECB) and an active current limit (ACL). In the event that a supply's current exceeds the ECB threshold, an internal timer is started. If the supply is still overcurrent after 22μs, the ECB trips and all supplies are turned off (Figure 7). An analog current limit loop prevents the supply current from exceeding 3x the ECB threshold in the event of a short circuit (Figure 8). The 22μs filter delay and the higher ACL threshold prevents unnecessary resets of the board due to minor current surges. The LTC4245 will stay in the latched off state unless bit C1 is set, in which case the switches turn on after a 100ms delay. Note that foldback is not active after start-up.

Undervoltage Fault

An undervoltage fault occurs when any of the input supplies falls below its undervoltage threshold for more than 3.5μs (5.5μs for V_{EEIN}). This turns off all switches immediately and sets the undervoltage present bit A0 and the corresponding undervoltage fault bit (bits E0 to E3). If the supply subsequently rises above the threshold for 100ms, the switches will turn on again unless the undervoltage auto-retry has been disabled by clearing bit C0. When power is first applied to the device, if any supply is below its threshold after $INTV_{CC}$ crosses its undervoltage lockout threshold, an undervoltage fault will be logged in the FAULT1 register.

PGI Fault

The PGI pin can be used to shut off the board's input supplies in case downstream supplies fail to enter regulation in time. It can be tied to the reset output of a monitor IC or the powergood pin of a DC/DC converter.

After all supply outputs have been powered up, a timing cycle is started with a 10μA current pulling up the TIMER pin. When TIMER reaches 2.56V it is reset to ground by a switch. As TIMER falls below 0.23V, the PGI pin is sampled. If it is low, the PGI fault bit F4 is set and all external FETs are shut off. A cool-down timing cycle is started using a 2μA pull-up current on TIMER pin. Bit F4 cannot be reset during this time. After this cycle, the switches will be allowed to turn on again if the PGI fault bit is cleared. However, if the PGI autoretry bit, C4, has been set then the switches turn on again automatically after the 100ms turn-on delay.

By default, the PGI pin is ignored during normal operation. It can be enabled by clearing PGI disable bit C3. Now, if PGI pin goes low for more than 20μs, all FETs will be shut off. If bit C4 is set, the switches will turn on after the 100ms turn-on delay.

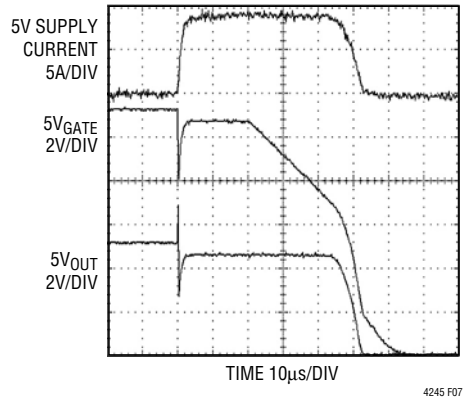

Figure 7. Overcurrent Fault on 5V Output

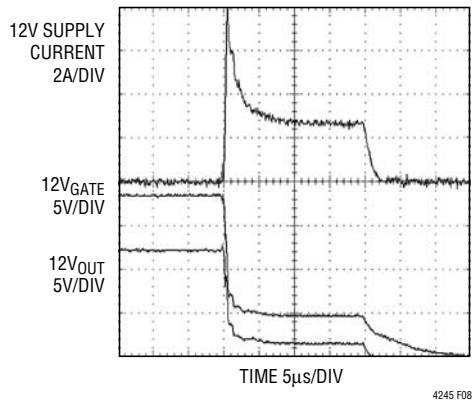

Figure 8. Short-Circuit Fault on 12V Output

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Power Bad Fault

A power bad condition exists when any supply output drops below its power bad threshold for more than 15µs (17µs for V_{EEOUT}). This sets bit A2 in the STATUS register. The HEALTHY# output goes high impedance, and LOCAL_PCI_RST# pin is pulled low. If the gate of the supply's MOSFET is enhanced, a power bad fault is logged in bits F0 to F3 of the FAULT2 register. A circuit will prevent power bad fault bits being set if the external MOSFET gate-to-source voltage is low, eliminating false power bad faults during power-up or power-down. If the supply output subsequently rises back above the threshold, bit A2 will be cleared, HEALTHY# will pull low and LOCAL_PCI_RST# will follow PCI_RST#.

BD_SEL# Change of State

Whenever the BD_SEL# pin toggles, bit F6 is set to indicate a change of state. When the BD_SEL# pin goes high, indicating board removal, all switches turn off immediately. Bit A6 reports the current state of this pin. If the BD_SEL# pin is pulled low, indicating a board insertion, all fault bits except F6 will be cleared. If the sequence bit C6 is set, then On control bits D1 to D3 are also cleared. If the BD_SEL# pin remains low for 100ms the state of the ON pin will be captured in either D0 to D3 or only D0, depending on sequence bit C6. This turns on the switches if ON pin is tied high. There is an internal 10µA pull-up current source on the BD_SEL# pin from $INTV_{CC}$.

If the system shuts down due to a fault, it may be desirable to restart the system simply by removing and reinserting a load card. In cases where the LTC4245 and the switches reside on a backplane or midplane (as in a PCI Express application) and the load resides on a plug-in card, the BD_SEL# pin can be used to detect when the plug-in card is removed (see Figure 9). Once the plug-in card is reinserted the two fault registers are cleared (except for F6). After 100ms the state of ON pin is latched into bits D0 to D3. At this point the system will start up again.

If a connection sense on the plug-in card is driving the BD_SEL# pin, the insertion or removal of the card may cause the pin voltage to bounce. This will result in clearing the fault register when the card is removed. The pin can be debounced using a filter capacitor, $C_{BD\_SEL\#}$, on the BD_SEL# pin as shown in Figure 9. The filter time is given by:

$$t_{FILTER} = C_{BD\_SEL\#} \bullet 123\ [ms/\mu F] \quad (5)$$

FET Short Fault

A FET short fault will be reported if the data converter measures a supply's current sense voltage greater than 7 LSB while the supply's pass transistor is turned off. This condition sets the FET short present bit, A5, and the FET short fault bit F5. Reading the On status bits (D4 to D7) and the ADC current sense voltage data registers (J, M, P, S) can help debug which supply's MOSFET might be potentially shorted. A false FET short fault might be reported if an input supply power-up is delayed by more than 500ms after $INTV_{CC}$ is up.

Fault Alerts

When any of the bits in fault registers E and F are set, an optional bus alert can be generated by setting the appropriate bit in the ALERT register B. This allows only selected faults to generate alerts. At power-up the default state is not to alert on faults. If an alert is enabled, the corresponding fault will cause the ALERT# pin to pull low. See the Alert Response Protocol section for more information.

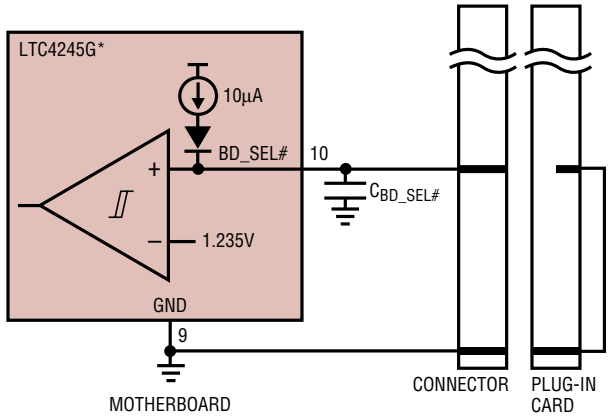

Figure 9. Plug-In Card Insertion/Removal

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Resetting Faults

The two fault registers E and F can be reset in any of the following ways:

1. Writing zeros to the registers using the I^2C bus.
2. Taking the ON pin high to low resets both registers.
3. $INTV_{CC}$ falling below its undervoltage lockout threshold.
4. Bringing BD_SEL# from high to low clears all fault bits except bit F6. Bit F6, which indicates a BD_SEL# change of state, will be set.

Note that faults that are still present cannot be cleared. Overcurrent and PGI faults are continuously set during their cool-down timing cycles and hence cannot be reset for that duration. The fault registers will not be cleared when auto-retrying. When autoretry is disabled the existence of an undervoltage (E0 to E3), overcurrent (E4 to E7) or PGI (F4) fault keeps the switches off. As soon as the fault is cleared, the switches will turn on.

Precharge

The PRECHARGE pin provides a 1V voltage (using a divided down $3V_{IN}$ as the reference) that is used to bias the CPCI bus connector pins during board insertion and extraction. The pin can source 70mA without losing regulation. An external 18Ω resistor from this pin to ground provides the current sink capability. At least one long 3.3V connector pin must be connected to $3V_{IN}$ to provide early power to the precharge circuit.

Resistors are used to connect the 1V bias voltage to the CPCI bus signals. For 5V signaling this resistance must be greater than 10kΩ - 5% (Figure 1). For 3.3V signaling if the leakage current on the I/O line is greater than 2µA, the precharge resistors need to be disconnected during normal operation. Figure 10 shows a circuit that uses a bus switch to accomplish this. The connection is made when the voltage on the BD_SEL# pin is pulled up to 5V, which occurs just after the long pins have made contact. The resistors are disconnected when the short BD_SEL# connector pin makes contact and the BD_SEL# voltage drops below 4.4V thus causing $\overline{OE}$ to be pulled high by

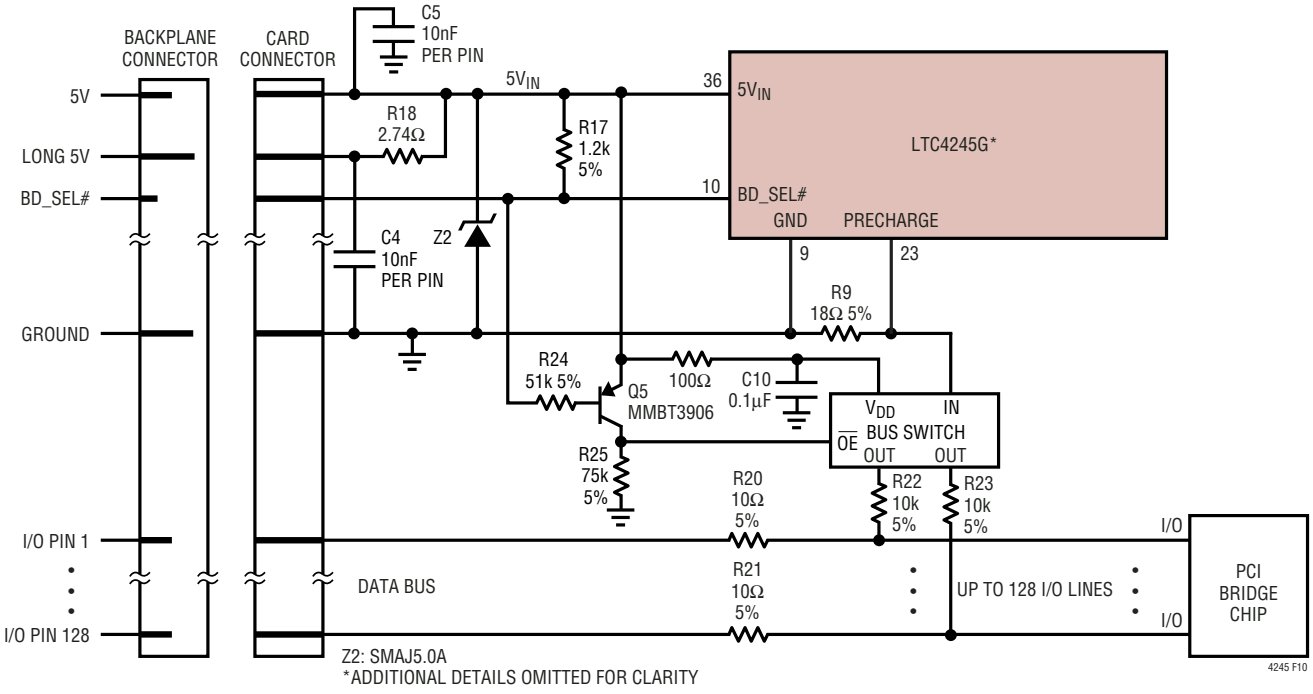

Figure 10. Precharge Bus Switch Application Circuit for 3.3V and Universal Hot Swap Boards

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Q5. The CPCI specification assumes that there is a diode to 3.3V on the circuit that is driving the BD_SEL# pin. If the BD_SEL# pin is being driven high, the actual voltage on the pin will fall to approximately 3.9V from 5V. This is still above the threshold of the LTC4245 BD_SEL# pin, but low enough for Q5 to pull $\overline{OE}$ high. Since the bus switch is powered off an early power plane, a 100Ω resistor should be placed in series with its V_{DD} .

When the plug-in card is removed from the backplane, the BD_SEL# connection is broken first, and the BD_SEL# voltage pulls up to 5V. This causes Q5 to turn off, which re-enables the bus switch, and the precharge resistors are again connected to the PRECHARGE pin for the remainder of the extraction process.

Data Converter

The LTC4245 incorporates an 8-bit data converter that continuously converts thirteen different channels. Twelve of these channels are used for each supply's input, current sense and output voltages. One of the three GPIO pins can be multiplexed to the thirteenth channel using bits G6 and G7. The results from each conversion are stored in registers I through U and are updated once every 665ms. Since the ADC is powered off $INTV_{CC}$, which is derived from $12V_{IN}$, it is not possible to convert $12V_{IN}$ below about 8V as the ADC and serial bus are held in reset.

The ADC can also measure a particular channel on-demand. First the ADC needs to be taken out of it's free-running mode by setting control bit C7. The ADC enters a quiescent state, which is indicated by the ADC busy bit, A7, going to logic zero. Writing the address of a channel to ADCADR register triggers the start of one conversion of that channel's voltage. Bit A7 goes high to indicate ADC activity. It goes low again after the ADC finishes the conversion and writes the result to the channel's data register. The same or different address can be written again to start a new conversion. The quiescent state of the ADC can also be used to read and write from the ADC data registers for software testing purposes. Resetting bit C7 allows the ADC to again start cycling through the thirteen channels starting with the first one.

Digital Interface

The LTC4245 communicates with a bus master using a 2-wire interface compatible with the I^2C bus and the SMBus, an I^2C extension for low power devices.

The LTC4245 is a read-write slave device and supports SMBus Read Byte, Write Byte, Read Word and Write Word commands. The second word in a Read Word command will be identical to the first word. The second word in a Write Word command is ignored. The data formats for these commands are shown in Figures 12 to 15.

START and STOP Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

I^2C Device Addressing

Thirty-two distinct bus addresses are configurable using the two-state ADR0, ADR1 pins and the three-state ADR2, ADR3 pins. Table 5 shows the correspondence between pin states and addresses. Note that address bits B7 and B6 are internally configured to (01)b. The first 16 addresses are compatible with the geographic addressing scheme used in CompactPCI to encode physical slot addresses. In addition, the LTC4245 will respond to two special addresses. Address (0010 111)b is a mass write address used to write to all LTC4245, regardless of their individual address settings. The mass write can be masked by setting register bit C5 to zero. Address (0001 100)b is the SMBus Alert Response Address. If the LTC4245 is pulling low on the ALERT# pin, it will acknowledge this address using the SMBus Alert Response Protocol.

Acknowledge

The acknowledge signal is used for handshaking between the transmitter and the receiver to indicate that the last byte of data was received. The transmitter always releases the

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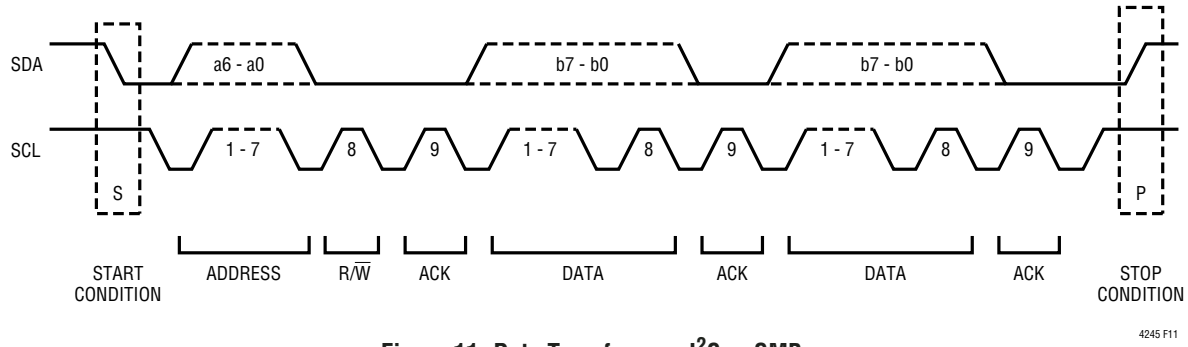

Figure 11. Data Transfer over I²C or SMBus

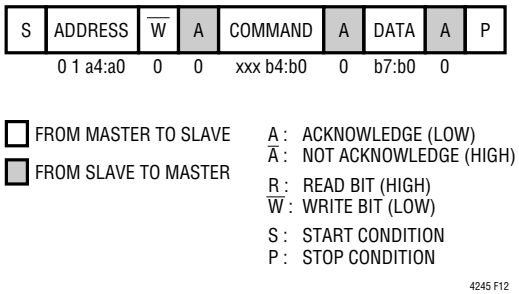

Figure 12. LTC4245 Serial Bus SDA Write Byte Protocol

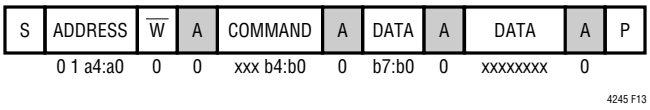

Figure 13. LTC4245 Serial Bus SDA Write Word Protocol

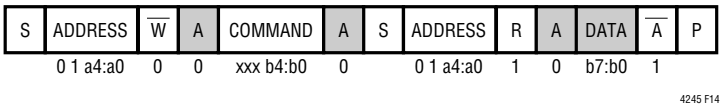

Figure 14. LTC4245 Serial Bus SDA Read Byte Protocol

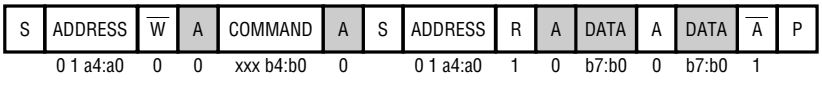

Figure 15. LTC4245 Serial Bus SDA Read Word Protocol

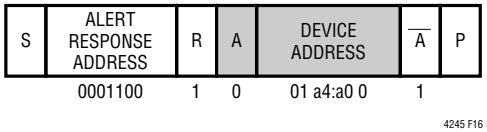

Figure 16. LTC4245 Serial Bus SDA Alert Response Protocol

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SDA line during the acknowledge clock pulse. When the slave is the receiver, it must pull down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA HIGH, then the master can abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master must pull down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received, the master will leave the SDA line HIGH (not acknowledge) and issue a STOP condition to terminate the transmission.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the R/$\overline{W}$ bit set to zero. The addressed LTC4245 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTC4245 acknowledges this and then latches the lower five bits of the command byte into its internal Register Address Pointer. The master then delivers the data byte and the LTC4245 acknowledges once more and latches the data into its internal register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a Write Word command, the second data byte will be acknowledged by the LTC4245 but ignored.

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the R/$\overline{W}$ bit set to zero. The addressed LTC4245 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to read. The LTC4245 acknowledges this and then latches the lower five bits of the command byte into its internal Register Address Pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/$\overline{W}$ bit now set to one. The LTC4245 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a Read Word command, the LTC4245 will repeat the requested register as the second data byte.

Note that the Register Address Pointer is not cleared at the end of the transaction. Thus the Receive Byte protocol can be used to repeatedly read a specific register.

Alert Response Protocol

The LTC4245 implements the SMBus Alert Response Protocol as shown in Figure 16. If enabled to do so through the ALERT register B, the LTC4245 will respond to faults by pulling the ALERT# pin low. Multiple LTC4245s can share a common ALERT# line and the protocol allows a master to determine which LTC4245s are pulling the line low. The master begins by sending a START bit followed by the special Alert Response Address (0001 100)b with the R/$\overline{W}$ bit set to one. Any LTC4245 that is pulling its ALERT# pin low will acknowledge and begin sending back its individual slave address.

An arbitration scheme ensures that the LTC4245 with the lowest address will have priority; all others will abort their response. The successful responder will then release its ALERT# pin while any others will continue to hold their ALERT# pins low. Polling may also be used to search for any LTC4245 that have detected faults. Any LTC4245 pulling its ALERT# pin low will have bit B3 in the ALERT register set. Writing a zero to this bit will release the ALERT# pin.

The ALERT# signal will not be pulled low again until the FAULT1 or FAULT2 register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate alerts until the associated fault register bit has been cleared. Also, a fault on one supply will not generate an alert if a fault bit of the same kind (undervoltage, overcurrent, power bad) is set for any other supply.

General Purpose Input/Outputs (GPIOs)

The G36 package of the LTC4245 has one GPIO (GPIO1) pin while the UHF package has three (GPIO1 to GPIO3). Bits G0 to G2 in the GPIO register (Table 13) indicate whether a pin is above or below the 1V threshold voltage. Bits G3 to G5 control whether the open-drain output on a GPIO pin pulls low or is high impedance. This can be used to drive external pull-up resistors or LEDs. Register bits G6 and G7 control which one of the three pins is multiplexed to the GPIO channel of the ADC. Whenever the GPIO1 pin

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toggles, bit F7 is set to indicate a change of state. If the GPIO1 alert bit B7 is enabled, this feature can be used to alert the host system to a change in state of the board's ejector handles.

Compensating the Active Current Loop

The four active current limit circuits of the LTC4245 are compensated internally and therefore do not require any RC network on the gate pins. The internal compensation should work for most pass transistors. If the gate capacitance is very small then the best method to compensate the loop is to add a 1nF to 5nF capacitor between the gate and source of the external MOSFET.

Supply Collapse During Transients

The LTC4245 is designed to ride through supply transients caused by load steps. If there is a shorted load and the parasitic inductance back to the supply is significant, there is a chance that the supply could collapse before the active current limit circuit brings down the gate of the external MOSFET. In this case the undervoltage lockout circuit, which has a 3.5µs (5.5µs for V_{EEIN}) filter time, turns off the pass transistors.

Input Overvoltage Transient Protection

Hot-plugging a board into a backplane generates inrush currents from the backplane power supplies due to the charging of the plug-in board capacitance. To reduce this transient current to a safe level, the CPCI Hot Swap specification restricts the amount of unswitched capacitance used on the input side of the plug-in board. Each medium or long power pin connected to the CPCI female connector on the plug-in board is required to have a 10nF ceramic bypass capacitor to ground. Bulk capacitors are allowed on the switched output side of the LTC4245. Some bulk capacitance is allowed on the Early Power planes, but only because a current limiting resistor is assumed to decouple the connector pin from the bulk capacitance (e.g., see 100Ω to Bus Switch V_{DD} in Figure 10).

Disallowing bulk capacitors on the input power pins tends to create a resonant circuit formed by the inductance of the backplane power supply trace and the parasitic capacitance of the plug-in board (mainly due to the large power MOSFET). Upon board insertion, the ringing of this circuit can exhibit a peak overshoot of 2.5 times the steady-state voltage (>30V for $12V_{IN}$).

There are two methods for abating the effects of these high voltage transients: using voltage limiters to clip the transient to a safe level and snubber networks. Snubber networks are series RC networks whose time constants are experimentally determined based on the board's parasitic resonance circuits. As a starting point, the capacitors in these networks are chosen to be 10× to 100× the power MOSFET's C_{OSS} under bias. The series resistor is a value determined experimentally that ranges from 1Ω to 50Ω, depending on the parasitic resonance circuit. Note that in all LTC4245 circuit schematics, both transient voltage limiters and snubber networks have been added to the $12V_{IN}$ and V_{EEIN} supply rails and should always be used. Snubber networks are not necessary on the $3V_{IN}$ or the $5V_{IN}$ supply lines since their absolute maximum ratings are 10V. Transient voltage limiters, however, are recommended as these devices provide large-scale transient protection for the LTC4245 in the event of abrupt changes in supply current. All protection networks should be mounted very close to the LTC4245's supply pins using short lead lengths to minimize the trace resistance and inductance. A recommended layout of the 5V and 12V transient protection devices around the LTC4245 is shown in Figure 18.

Design Example

As a design example, consider a Hot Swap application with the following power supply requirements:

Table 1. Example Power Supply Requirements

VOLTAGE SUPPLY	MAXIMUM LOAD CURRENT	MAXIMUM INRUSH dI/dt	LOAD CAPACITANCE
12V	600mA	150mA/ms	100µF
5V	5A	1.5A/ms	2200µF
3.3V	7A	1.5A/ms	2200µF
–12V	300mA	150mA/ms	100µF

1. Select the appropriate values of R_{SENSE} for the supplies. Calculating the value of R_{SENSE} is based on $I_{LOAD(MAX)}$ and the lower limit for the circuit breaker threshold voltage, $\Delta V_{SNS(CB)(MIN)}$. If a 1% tolerance is assumed for the sense resistors, then the following values of resistances should suffice:

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Table 2. Sense Resistance Values

SUPPLY	R_{SENSE}(1%)	$I_{TRIP(MIN)}$	$I_{TRIP(MAX)}$
12V	50mΩ	891mA	1.1A
5V	3.5mΩ	6.4A	7.9A
3.3V	2.5mΩ	8.9A	11.1A
–12V	100mΩ	396mA	606mA

If necessary, two resistors with the same tolerance can be connected in parallel to yield the 3.5mΩ and 2.5mΩ values.

2. Select the SS capacitor for limiting the rate of rise of inrush current. Equations 1 and 2 lead to the following design equation:

$$C_{SS(MIN)} \geq \frac{G_{SS} \bullet I_{SS(MAX)}}{R_{SENSE(MIN)} \bullet (dI/dt)_{(MAX)}} \quad (6)$$

Applying Equation 6 to the 12V supply, with G_{SS} of 46mV/V, $I_{SS(MAX)}$ of 24µA, $R_{SENSE(MIN)}$ of 49.5mΩ, and $(dI/dt)_{(MAX)}$ of 150mA/ms yields a $C_{SS(MIN)}$ greater than 149nF. This capacitance value satisfies the dI/dt requirements of the other supplies too. Hence, a 220nF (±10%) capacitor is chosen for C_{SS}.

3. To determine the TIMER capacitance, the time required to completely power-up all supply outputs simultaneously needs to be calculated. There are three parts to this time: time for the internal current limit to cross zero (t_1), time for the gate to slew to the MOSFET threshold voltage (t_2) and the time for the current flow to charge up the load capacitors (t_3) (see Figure 17).

t_1: The time for the internal current limit to rise above zero is simply:

$$t_1 = 4 \bullet \frac{I_{FBL(MIN)}}{(dI/dt)_{(MIN)}} \quad (7)$$

t_2: The maximum time for the gate of the external MOSFET to rise to the threshold voltage depends on $I_{GATE(UP)(MIN)}$ and the gate charge required to turn on the external MOSFET. A typical value for this time is 1ms. This can be verified after the MOSFETs are selected. Since the current limit ramp is almost stopped while any MOSFET is turning on, t_2 is 4 times 1ms or 4ms, since in the worst case none of the four MOSFET turn-ons overlaps in time.

t_3: Under simultaneous power-up each output voltage affects the inrush current profile. To simplify calculations, the inrush current profile shown in Figure 17 is chosen. All the current is assumed to charge the load capacitor, i.e., there is no load current. There are four parts to t_3 as shown. Equations 8 to 11 are used to determine t_{31} to t_{34}:

$$t_{31} = \frac{I_{FBL(MIN)}}{(dI/dt)_{(MIN)}} \quad (8)$$

$$t_{32} = \frac{C_L \bullet V_{FB}}{I_{FBL(MIN)}} - 0.5 \bullet t_{31} \quad (9)$$

$$t_{33} = \min\left(\frac{I_{FBH(MIN)} - I_{FBL(MIN)}}{(dI/dt)_{(MIN)}}, \sqrt{\frac{2 \bullet C_L \bullet (V_{OUT} - V_{FB})}{(dI/dt)_{(MIN)}} + t_{31}^2} - t_{31}\right) \quad (10)$$

$$t_{34} = \max\left(0, \frac{C_L \bullet (V_{OUT} - V_{FB}) - 0.5 \bullet t_{33} \bullet (I_{FBL(MIN)} + I_{FBH(MIN)})}{I_{FBH(MIN)}}\right) \quad (11)$$

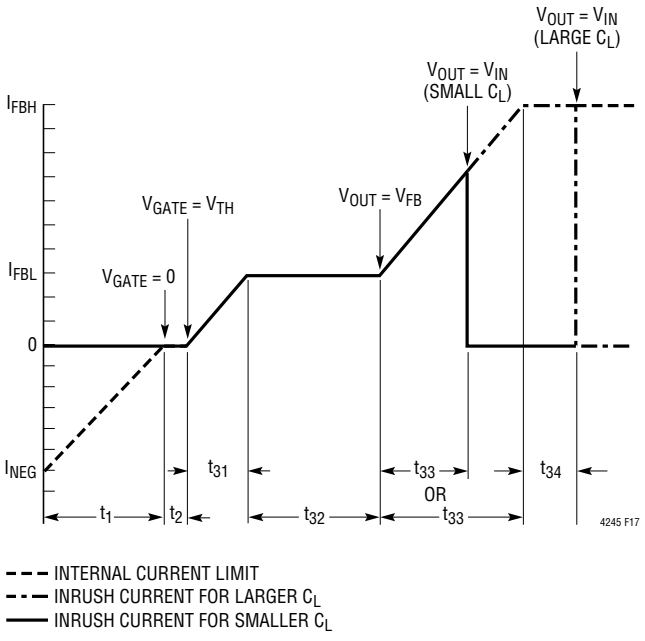

Figure 17. Inrush Current Profile for Design Example

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The inputs to the above equations are pre-calculated in Table 3.

Table 3. t_3 Calculation Inputs

SUPPLY	V_{OUT}	V_{FB}	$(dI/dt)_{(MIN)}$	$I_{FBL(MIN)}$	$I_{FBH(MIN)}$
12V	12V	6V	60mA/ms	198mA	792mA
5V	5V	3V	430mA/ms	1.13A	6.22A
3.3V	3.3V	2V	602mA/ms	1.58A	8.71A
–12V	12V	6V	30mA/ms	109mA	396mA

Equations 8 to 11, when applied to the four supplies yields:

Table 4. t_3 Calculation Results

SUPPLY	t_{31}	t_{32}	t_{33}	t_{34}	TOTAL(t_3)
12V	3.3ms	1.4ms	2.3ms	0	7ms
5V	2.6ms	4.5ms	2.6ms	0	9.7ms
3.3V	2.6ms	1.5ms	1.4ms	0	5.5ms
–12V	3.6ms	3.7ms	3.7ms	0	11ms

Therefore the TIMER capacitance value is constrained by the –12V supply inrush current. The total time ($t_1 + t_2 + t_3$) is approximately 30ms. Equation 4 gives the capacitor value to be:

$$C_{T(MIN)} \geq 30ms / K_{TMCAP(MIN)} = 1.5\mu F \quad (12)$$

So a value of 2.2μF (±10%) should suffice.

4. The next step is to select MOSFETs for the four supplies. The IRF7413 is selected for 12V, Si7880DP for 5V and 3.3V, and Si4872 for –12V Supply. The Si7880DP's on resistance is less than 4.25mΩ for V_{GS} = 4.5V and a junction temperature of 25°C.

Since the maximum load current requirement for the 3.3V supply is 7A, the steady-state power the MOSFET may be required to dissipate is 208mW. The Si7880DP has a maximum junction-to-ambient thermal resistance of 65°C/W. If a maximum ambient temperature of 50°C is assumed, this yields a junction temperature of 63.5°C. According to the Si7880DP's Normalized On-Resistance vs Junction Temperature curve, the device's on-resistance can be expected to increase by about 15% over its room temperature value. Recalculation of the steady-state values of R_{ON} and junction temperature yields approximately 4.9mΩ and 67°C, respectively. The I • R drop across the 3.3V sense resistor and series MOSFET at maximum load current under these conditions will be less than 52mV.

The energy dissipated in the MOSFET during power-up is the same as that stored into the load capacitor. The average power dissipated in the MOSFET is:

$$P_{ON} = \frac{C_L \bullet V_{OUT}^2}{2 \bullet t_3} \quad (13)$$

The 12V MOSFET's single-pulse $\theta_{JA(MAX)}$, as read from its Transient Thermal Impedance Graph, is 3°C/W for a time, t_3, of 7ms. P_{ON} is calculated to be 1W and therefore the 12V MOSFET temperature rise during power-up is 3°C. The other supplies show a smaller rise in MOSFET temperature than this value.

When a supply powers-up into a short-circuit at the output, the supply current rises linearly to the lower foldback level and stays there till the timer expires and the MOSFETs are shut-off. To simplify calculations it will be assumed that the MOSFET conducts the lower foldback current from the moment it turns on. This time (t_{SC}) is the actual time the MOSFET is conducting current minus a correction for the assumption, which is half of the time required for the current to rise from zero to the lower foldback level. Therefore:

$$t_{SC(MAX)} = C_{T(MAX)} \bullet K_{TMCAP(MAX)} - \frac{(1.5 \bullet \Delta V_{SNS(FBL)(MAX)}) \bullet C_{SS(MIN)}}{G_{SS} \bullet I_{SS(MAX)}} \quad (14)$$

The $1.5 \bullet \Delta V_{SNS(FBL)(MAX)}$ term is due to the correction factor and the time spent in ramping the starting negative current limit to zero. $t_{SC(MAX)}$ turns out to be about 58ms for all four supplies. The maximum power dissipated in the MOSFET is given by:

$$P_{SC(MAX)} = I_{FBL(MAX)} \bullet V_{OUT} \quad (15)$$

$P_{SC(MAX)}$ for the 5V supply is 3.2A • 5V, or 16W. $\theta_{JA(MAX)}$ for the 5V MOSFET is 3.25°C/W. Therefore the MOSFET temperature rise during power-up into a $5V_{OUT}$ short-circuit is 52°C. Similar calculations show that the other supplies experience a smaller MOSFET temperature rise. The $\theta_{JA(MAX)}$ value is read from the MOSFET datasheet's Transient Thermal Impedance Graph for a duty cycle of 0.02, which is the case when the LTC4245 is configured for auto-retry on overcurrent faults.

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PCB Layout Considerations

For proper operation of the LTC4245's circuit breaker, Kelvin connection to the sense resistors is strongly recommended. The PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout for the 5V sense resistor and the power MOSFET around the LTC4245 is illustrated in Figure 18. In Hot Swap applications where load currents can be 10A, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper foil is approximately 0.5mΩ/□, track resistances and voltage drops add up quickly in high current applications. Thus, to keep PCB track resistance, voltage drop and temperature rise to a minimum, the suggested trace width in these applications for 1oz copper foil is 0.03" for each ampere of DC current.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PCB. For 1oz copper foil plating, a general rule is 1A of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

It is also important to put C1, the bypass capacitor for the $INTV_{CC}$ pin as close as possible between $INTV_{CC}$ and GND. The surge suppressors, Z1 and Z2, are placed between the supply inputs and ground using wide traces.

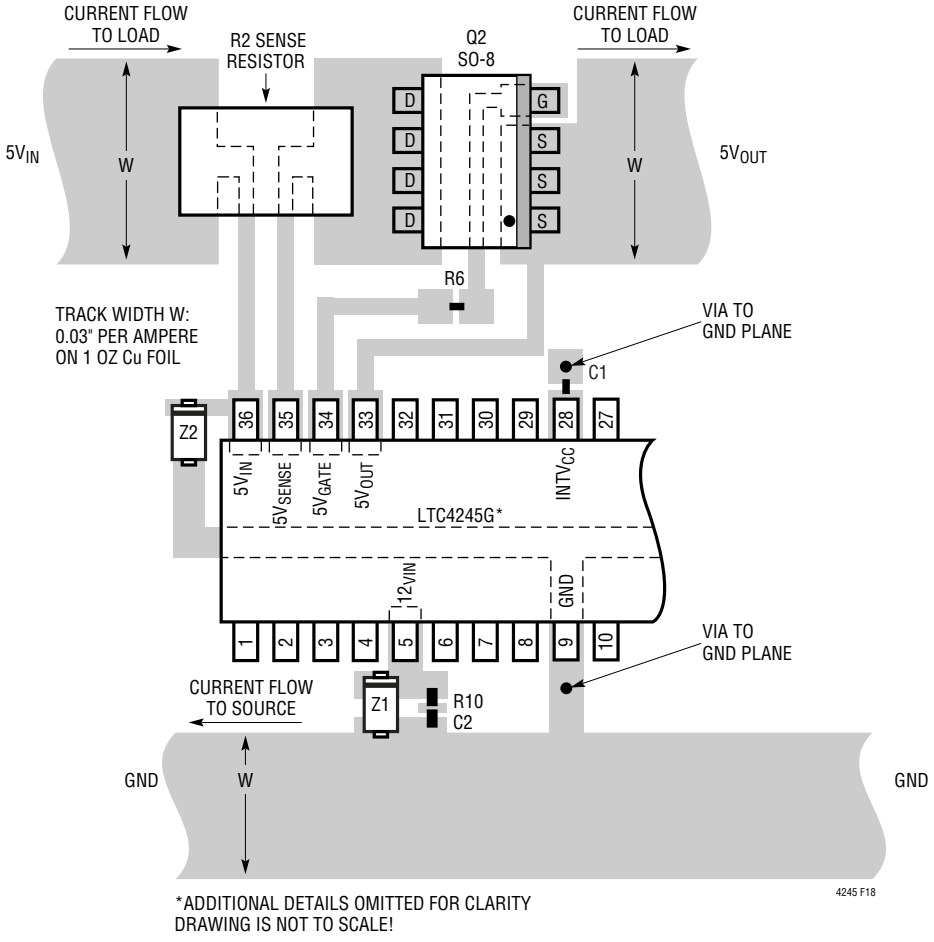

Figure 18. Recommended Layout for R2, Q2, R6, Z2, C1, Z1, R10 and C2

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Table 5. LTC4245 I²C Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTC4245 ADDRESS PINS*			
	H	6	5	4	3	2	1	0	R/$\overline{W}$	ADR3	ADR2	ADR1	ADR0
Mass Write	2E	0	0	1	0	1	1	1	0	X	X	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X	X	X
0	40	0	1	0	0	0	0	0	X	L	L	L	L
1	42	0	1	0	0	0	0	1	X	L	L	L	NC
2	44	0	1	0	0	0	1	0	X	L	L	NC	L
3	46	0	1	0	0	0	1	1	X	L	L	NC	NC
4	48	0	1	0	0	1	0	0	X	L	NC	L	L
5	4A	0	1	0	0	1	0	1	X	L	NC	L	NC
6	4C	0	1	0	0	1	1	0	X	L	NC	NC	L
7	4E	0	1	0	0	1	1	1	X	L	NC	NC	NC
8	50	0	1	0	1	0	0	0	X	NC	L	L	L
9	52	0	1	0	1	0	0	1	X	NC	L	L	NC
10	54	0	1	0	1	0	1	0	X	NC	L	NC	L
11	56	0	1	0	1	0	1	1	X	NC	L	NC	NC
12	58	0	1	0	1	1	0	0	X	NC	NC	L	L
13	5A	0	1	0	1	1	0	1	X	NC	NC	L	NC
14	5C	0	1	0	1	1	1	0	X	NC	NC	NC	L
15	5E	0	1	0	1	1	1	1	X	NC	NC	NC	NC
16	60	0	1	1	0	0	0	0	X	L	H	L	L
17	62	0	1	1	0	0	0	1	X	L	H	L	NC
18	64	0	1	1	0	0	1	0	X	L	H	NC	L
19	66	0	1	1	0	0	1	1	X	L	H	NC	NC
20	68	0	1	1	0	1	0	0	X	NC/H	H	L	L
21	6A	0	1	1	0	1	0	1	X	NC/H	H	L	NC
22	6C	0	1	1	0	1	1	0	X	NC/H	H	NC	L
23	6E	0	1	1	0	1	1	1	X	NC/H	H	NC	NC
24	70	0	1	1	1	0	0	0	X	H	L	L	L
25	72	0	1	1	1	0	0	1	X	H	L	L	NC
26	74	0	1	1	1	0	1	0	X	H	L	NC	L
27	76	0	1	1	1	0	1	1	X	H	L	NC	NC
28	78	0	1	1	1	1	0	0	X	H	NC	L	L
29	7A	0	1	1	1	1	0	1	X	H	NC	L	NC
30	7C	0	1	1	1	1	1	0	X	H	NC	NC	L
31	7E	0	1	1	1	1	1	1	X	H	NC	NC	NC

* L = Low, H = High, NC = Not Connected, X = Don't Care

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Table 6. LTC4245 Register Address and Contents

REGISTER ADDRESS*		REGISTER NAME	READ/WRITE	DESCRIPTION
DECIMAL	HEX			
0, 8	00h, 08h	STATUS (A)	R	System Status Information
1, 9	01h, 09h	ALERT (B)	R/W	Controls Which Faults Cause ALERT# Pin to be Pulled Low
2, 10	02h, 0Ah	CONTROL (C)	R/W	Controls Part Behavior Such As Auto-Retry, Sequencing, etc.
3, 11	03h, 0Bh	ON (D)	D3:D0 R/W**, D7:D4 R	Sets State and Reports Status of Switches
4, 12	04h, 0Ch	FAULT1 (E)	R/W	Fault Log for Undervoltage and Overcurrent
5, 13	05h, 0Dh	FAULT2 (F)	R/W	Fault Log for Power Bad, PGI, FET Short, BD_SEL#, GPIO1
6, 14	06h, 0Eh	GPIO (G)	G2:G0 R, G7:G3 R/W	Sets State and Reports Status of GPIO1 to GPIO3 pins, Control Which Pin is Multiplexed to the GPIO Channel of ADC
7, 15	07h, 0Fh	ADCADR (H)	R/W	4-Bit ADC Channel Address for On-Demand ADC Measurement
16	10h	12VIN (I)	R/W†	ADC $12V_{IN}$ Voltage Data
17	11h	12VSENSE (J)	R/W†	ADC 12V Current Sense Voltage Data
18	12h	12VOUT (K)	R/W†	ADC $12V_{OUT}$ Voltage Data
19	13h	5VIN (L)	R/W†	ADC $5V_{IN}$ Voltage Data
20	14h	5VSENSE (M)	R/W†	ADC 5V Current Sense Voltage Data
21	15h	5VOUT (N)	R/W†	ADC $5V_{OUT}$ Voltage Data
22	16h	3VIN (O)	R/W†	ADC $3V_{IN}$ Voltage Data
23	17h	3VSENSE (P)	R/W†	ADC 3.3V Current Sense Voltage Data
24	18h	3VOUT (Q)	R/W†	ADC $3V_{OUT}$ Voltage Data
25	19h	VEEIN (R)	R/W†	ADC V_{EEIN} Voltage Data
26	1Ah	VEESENSE (S)	R/W†	ADC –12V Current Sense Voltage Data
27	1Bh	VEEOUT (T)	R/W†	ADC V_{EEOUT} Voltage Data
28 to 31	1Ch to 1Fh	GPIOADC (U)	R/W†	ADC GPIO Voltage Data

All registers are 8-bit wide.

* Register address MSBs b7 – b5 are ignored.

** Cannot set D3:D0 high if bit A1 set.

† Set bit C7 before writing.

Table 7. STATUS Register A (00h)- Read Only

BIT	NAME	OPERATION
A7	ADC Busy	Indicates State of ADC; 1 = ADC Busy Measuring, 0 = ADC Quiescent
A6	BD_SEL# Input	State of the BD_SEL# Pin; 1 =BD_SEL# High, 0 = BD_SEL# Low
A5	FET Short Present	Indicates Potential FET Short on at Least One Supply, if ADC Current Sense Voltage Measurement Exceeds 7 LSB While FET is Off; 1 = FET is Shorted, 0 = FET is Not Shorted
A4	LOCAL_PCI_RST# Output	LOCAL_PCI_RST# Pin Open-Drain Output State; 1 = High Impedance, 0 = Pulls Low
A3	PCI_RST# Input	State of the PCI_RST# Pin; 1 = PCI_RST# High, 0 = PCI_RST# Low
A2	Power Bad	Indicates Power Bad Present on at Least One of the Supply Outputs; 1 = Power Bad, 0 = No Power Bad
A1	SS Busy	Indicates SS Pin is Being Used to Ramp Up a Supply, Affects Writing to D3:D0 Bits 1 = SS Pin Ramping, Cannot Set D3:D0 High, 0 = SS Pin Reset
A0	Undervoltage	Indicates Undervoltage Present on at Least One of the Input Supply; 1 = Undervoltage, 0 = Not Undervoltage

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Table 8. ALERT Register B (01h) – Read/Write

BIT	NAME	OPERATION
B7	GPIO1 State Change Alert	Enables Alert When GPIO1 Changes State; 1 = Enable Alert, 0 = Disable Alert (Default)
B6	BD_SEL# State Change Alert	Enables Alert When BD_SEL# Changes State; 1 = Enable Alert, 0 = Disable Alert (Default)
B5	FET Short Alert	Enables Alert for FET Short Condition; 1 = Enable Alert, 0 = Disable Alert (Default)
B4	PGI Fault Alert	Enables Alert When a PGI Fault Occurs; 1 = Enable Alert, 0 = Disable Alert (Default)
B3	Alert Present	ALERT# Pin Open-Drain Output State; 1 = Pulls Low, 0 = High Impedance (Default)
B2	Power Bad Alert	Enables Alert When Output Power is Bad; 1 = Enable Alert, 0 = Disable Alert (Default)
B1	Overcurrent Alert	Enables Alert for Overcurrent Condition; 1 = Enable Alert, 0 = Disable Alert (Default)
B0	Undervoltage Alert	Enables Alert for Undervoltage Condition; 1 = Enable Alert, 0 = Disable Alert (Default)

Table 9. CONTROL Register C (02h) – Read/Write

BIT	NAME	OPERATION
C7	ADC Free-Run Disable	Disable ADC Free Running Operation to Allow On-Demand Measurement and Writes to ADC Registers; 1 = Halt ADC Free Running, 0 = ADC Free Running (Default)
C6	Sequencing Enable	Enables Supplies to Turn-On in a Set Sequence 1 = Sequencing Enabled, 0 = Sequencing Disabled (Default)
C5	Mass Write Enable	Enables Mass Write Using Address (0010 111)b 1 = Mass Write Enabled (Default), 0 = Mass Write Disabled
C4	PGI Fault Autoretry	Enables Autoretry After a PGI Fault; 1 = Retry Enabled, 0 = Retry Disabled (Default)
C3	PGI Pin Disable	Enables PGI Pin Going Low During Normal Operation to Shut Off Switches 1 = PGI Pin Disabled (Default), 0 = PGI Pin Enabled
C2	Reserved	Not Used
C1	Overcurrent Autoretry	Enables Autoretry After an Overcurrent Fault; 1 = Retry Enabled, 0 = Retry Disabled (Default)
C0	Undervoltage Autoretry	Enables Autoretry After an Undervoltage Fault; 1 = Retry Enabled (Default), 0 = Retry Disabled

Table 10. ON Register D (03h) – Read/Write

BIT	NAME	OPERATION
D7	–12V FET On Status	Indicates State of –12V FET. Read Only Bit; 1 = FET On, 0 = FET Off
D6	3.3V FET On Status	Indicates State of 3.3V FET. Read Only Bit; 1 = FET On, 0 = FET Off
D5	5V FET On Status	Indicates State of 5V FET. Read Only Bit; 1 = FET On, 0 = FET Off
D4	12V FET On Status	Indicates State of 12V FET. Read Only Bit; 1 = FET On, 0 = FET Off
D3	–12V FET On Control	Turns –12V FET On and Off. Not used if CFG Pin is Not Low. Cannot Write 1 if Bit A1 Set 1 = Turn FET On, 0 = Turn FET Off. Defaults to ON Pin State at End of Debounce Delay
D2	3.3V FET On Control	Turns 3.3V FET On and Off. Cannot Write 1 if Bit A1 Set 1 = Turn FET On, 0 = Turn FET Off. Defaults to ON Pin State at End of Debounce Delay
D1	5V FET On Control	Turns 5V FET On and Off. Cannot Write 1 if Bit A1 Set 1 = Turn FET On, 0 = Turn FET Off. Defaults to ON Pin State at End of Debounce Delay
D0	12V FET On Control	Turns 12V FET On and Off. Also Turns –12V FET On and Off if CFG Pin is Not Low. Cannot Write 1 if Bit A1 Set 1 = Turn FET On, 0 = Turn FET Off. Defaults to ON Pin State at End of Debounce Delay

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Table 11. FAULT1 Register E (04h) – Read/Write

BIT	NAME	OPERATION
E7	–12V Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred on –12V Supply 1 = Overcurrent Fault Occurred, 0 = No Overcurrent Faults
E6	3.3V Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred on 3.3V Supply 1 = Overcurrent Fault Occurred, 0 = No Overcurrent Faults
E5	5V Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred on 5V Supply 1 = Overcurrent Fault Occurred, 0 = No Overcurrent Faults
E4	12V Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred on 12V Supply 1 = Overcurrent Fault Occurred, 0 = No Overcurrent Faults
E3	–12V Undervoltage Fault Occurred	Indicates –12V Supply Undervoltage Fault Occurred When V_{EEIN} Went High 1 = V_{EEIN} was High, 0 = No Undervoltage Faults
E2	3.3V Undervoltage Fault Occurred	Indicates 3.3V Supply Undervoltage Fault Occurred When $3V_{IN}$ Went Low 1 = $3V_{IN}$ was Low, 0 = No Undervoltage Faults
E1	5V Undervoltage Fault Occurred	Indicates 5V Supply Undervoltage Fault Occurred When $5V_{IN}$ Went Low 1 = $5V_{IN}$ was Low, 0 = No Undervoltage Faults
E0	12V Undervoltage Fault Occurred	Indicates 12V Supply Undervoltage Fault Occurred When $12V_{IN}$ Went Low 1 = $12V_{IN}$ was Low, 0 = No Undervoltage Faults

Table 12. FAULT2 Register F (05h) – Read/Write

BIT	NAME	OPERATION
F7	GPIO1 Changed State	Indicates that GPIO1 Pin Changed State; 1 = GPIO1 Changed State, 0 = GPIO1 Unchanged
F6	BD_SEL# Changed State	Indicates that BD_SEL# Pin Changed State; 1 = BD_SEL# Changed State, 0 = BD_SEL# Unchanged
F5	FET Short Fault Occurred	Indicates Potential FET Short was Detected on at Least One Supply, When ADC Measured Current Sense Voltage Exceeded 7 LSB While FET was Off; 1 = FET was Shorted, 0 = FET is Good
F4	PGI Fault Occurred	Indicates PGI Fault Occurred; 1 = PGI Fault Occurred, 0 = No PGI faults
F3	–12V Power Bad Fault Occurred	Indicates –12V Power was Bad When V_{EEOUT} Went High 1 = V_{EEOUT} was High, 0 = No Power Bad Faults
F2	3.3V Power Bad Fault Occurred	Indicates 3.3V Power was Bad When $3V_{OUT}$ Went Low 1 = $3V_{OUT}$ was Low, 0 = No Power Bad Faults
F1	5V Power Bad Fault Occurred	Indicates 5V Power was Bad When $5V_{OUT}$ Went Low 1 = $5V_{OUT}$ was Low, 0 = No Power Bad Faults
F0	12V Power Bad Fault Occurred	Indicates 12V Power was Bad When $12V_{OUT}$ Went Low 1 = $12V_{OUT}$ was Low, 0 = No Power Bad Faults

Table 13. GPIO Register G (06h) – Read/Write (GPIO2, GPIO3 Bits Apply Only to the UHF Package)

BIT	NAME	OPERATION		
G7:6	GPIO Select	Control Which GPIO Pin is Multiplexed to the GPIO Channel of ADC		
		G7	**G6**	**GPIO**
		0	0	GPIO1 (Default)
		0	1	GPIO1
		1	0	GPIO2
		1	1	GPIO3
G5	GPIO3 Output	GPIO3 Pin Open-Drain Output State; 1 = High Impedance (Default), 0 = Pulls Low		
G4	GPIO2 Output	GPIO2 Pin Open-Drain Output State; 1 = High Impedance (Default), 0 = Pulls Low		
G3	GPIO1 Output	GPIO1 Pin Open-Drain Output State; 1 = High Impedance (Default), 0 = Pulls Low		
G2	GPIO3 Input	State of the GPIO3 Pin, Read Only Bit; 1 = GPIO3 High, 0 = GPIO3 Low		
G1	GPIO2 Input	State of the GPIO2 Pin, Read Only Bit; 1 = GPIO2 High, 0 = GPIO2 Low		
G0	GPIO1 Input	State of the GPIO1 Pin, Read Only Bit; 1 = GPIO1 High, 0 = GPIO1 Low		

APPLICATIONS INFORMATION

Table 14. ADCADR Register H (07h) – Read/Write

BIT	NAME	OPERATION
H7:4	Reserved	Not Used
H3:0	ADC Channel Address	Selects Which ADC Channel to Measure On-Demand

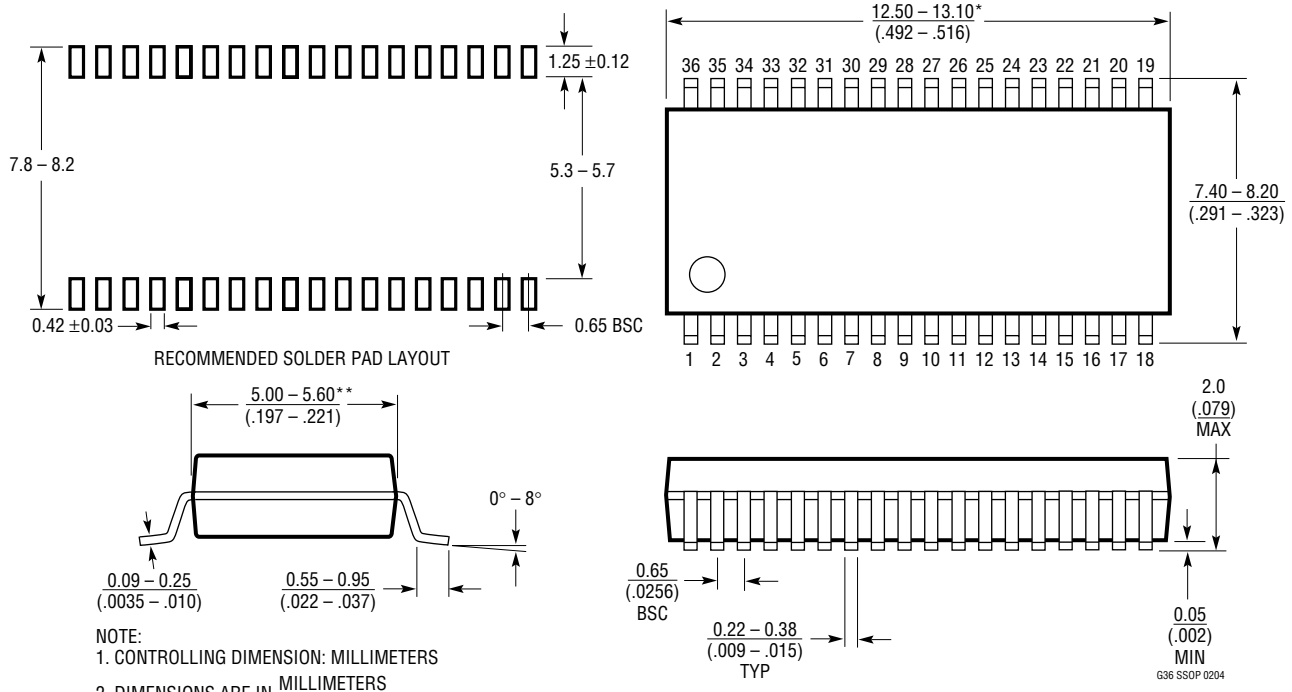
H3	H2	H1	H0	ADC CHANNEL
0	0	0	0	$12V_{IN}$ Voltage (Default)
0	0	0	1	12V Current Sense Voltage
0	0	1	0	$12V_{OUT}$ Voltage
0	0	1	1	$5V_{IN}$ Voltage
0	1	0	0	5V Current Sense Voltage
0	1	0	1	$5V_{OUT}$ Voltage
0	1	1	0	$3V_{IN}$ Voltage
0	1	1	1	3.3V Current Sense Voltage
1	0	0	0	$3V_{OUT}$ Voltage
1	0	0	1	V_{EEIN} Voltage
1	0	1	0	–12V Current Sense Voltage
1	0	1	1	V_{EEOUT} Voltage
1	1	X	X	GPIO Voltage

Table 15. ADC Data Registers I to U (10h to 1Fh) – Read/Write

BIT	NAME	OPERATION
I7:0	$12V_{IN}$ Voltage Data	$12V_{IN}$ Pin Voltage Data. 8-Bit Data with 55mV LSB and 14.025V Full Scale
J7:0	$12V_{SENSE}$ Voltage Data	$12V_{IN}$ to $12V_{SENSE}$ Current Sense Voltage Data. 8-Bit Data with 250µV LSB and 63.75mV Full Scale
K7:0	$12V_{OUT}$ Voltage Data	$12V_{OUT}$ Pin Voltage Data. 8-Bit Data with 55mV LSB and 14.025V Full Scale
L7:0	$5V_{IN}$ Voltage Data	$5V_{IN}$ Pin Voltage Data. 8-Bit Data with 22mV (or 15mV) LSB and 5.61V (or 3.825V) Full Scale
M7:0	$5V_{SENSE}$ Voltage Data	$5V_{IN}$ to $5V_{SENSE}$ Current Sense Voltage Data. 8-Bit Data with 125µV LSB and 31.875mV Full Scale
N7:0	$5V_{OUT}$ Voltage Data	$5V_{OUT}$ Pin Voltage Data. 8-Bit Data with 22mV (or 15mV) LSB and 5.61V (or 3.825V) Full Scale
O7:0	$3V_{IN}$ Voltage Data	$3V_{IN}$ Pin Voltage Data. 8-Bit Data with 15mV LSB and 3.825V Full Scale
P7:0	$3V_{SENSE}$ Voltage Data	$3V_{IN}$ to $3V_{SENSE}$ Current Sense Voltage Data. 8-Bit Data with 125µV LSB and 31.875mV Full Scale
Q7:0	$3V_{OUT}$ Voltage Data	$3V_{OUT}$ Pin Voltage Data. 8-Bit Data with 15mV LSB and 3.825V Full Scale
R7:0	V_{EEIN} Voltage Data	V_{EEIN} Pin Voltage Data. 8-Bit Data with –55mV LSB and –14.025V Full Scale
S7:0	$V_{EESENSE}$ Voltage Data	$V_{EESENSE}$ to V_{EEIN} Current Sense Voltage Data. 8-Bit Data with 250µV LSB and 63.75mV Full Scale
T7:0	V_{EEOUT} Voltage Data	V_{EEOUT} Pin Voltage Data. 8-Bit Data with –55mV LSB and –14.025V Full Scale
U7:0	GPIO Voltage Data	GPIO*n* Pin Voltage Data. 8-Bit Data with 10mV LSB and 2.55V Full Scale

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



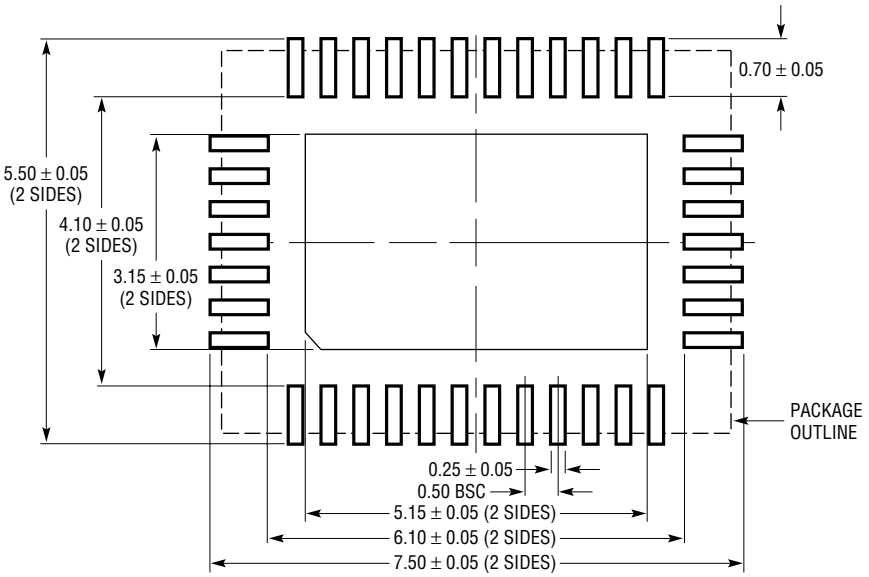
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

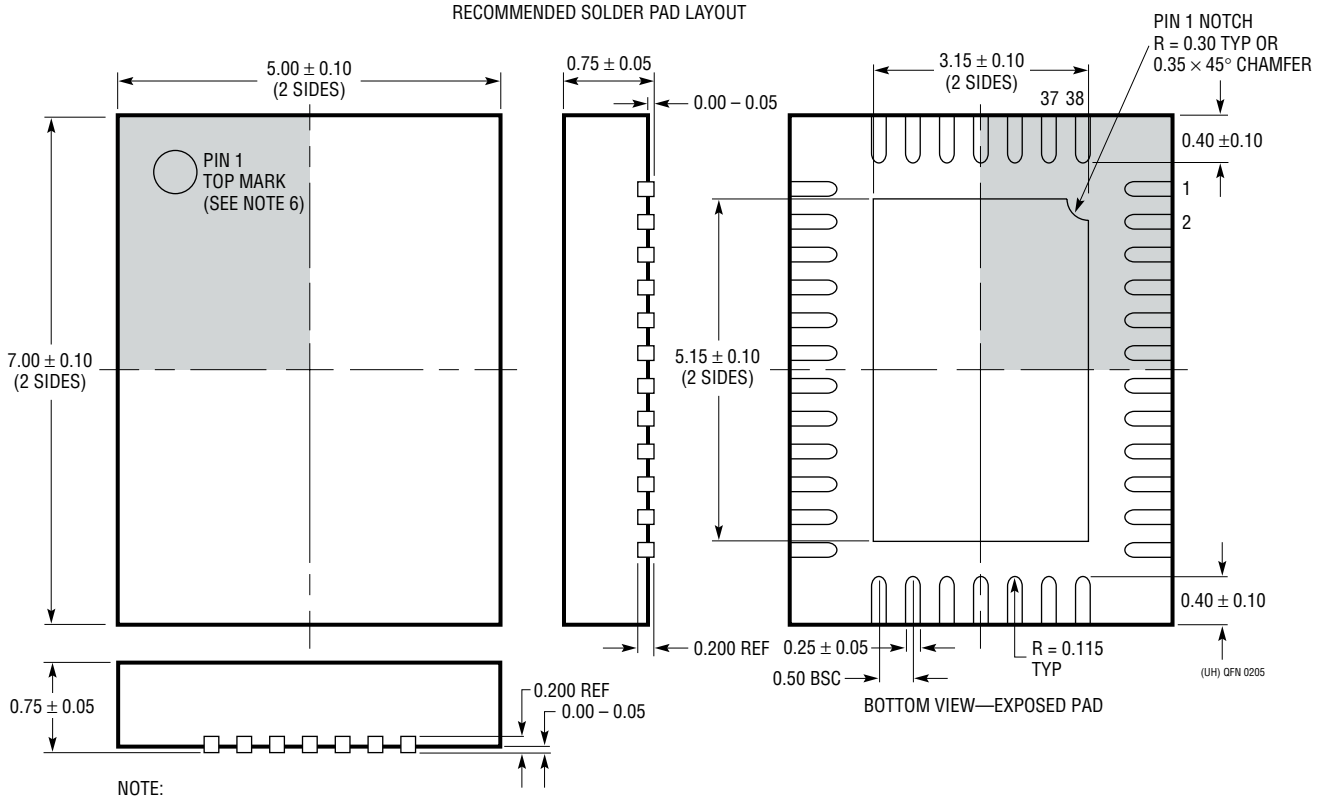
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701)



RECOMMENDED SOLDER PAD LAYOUT

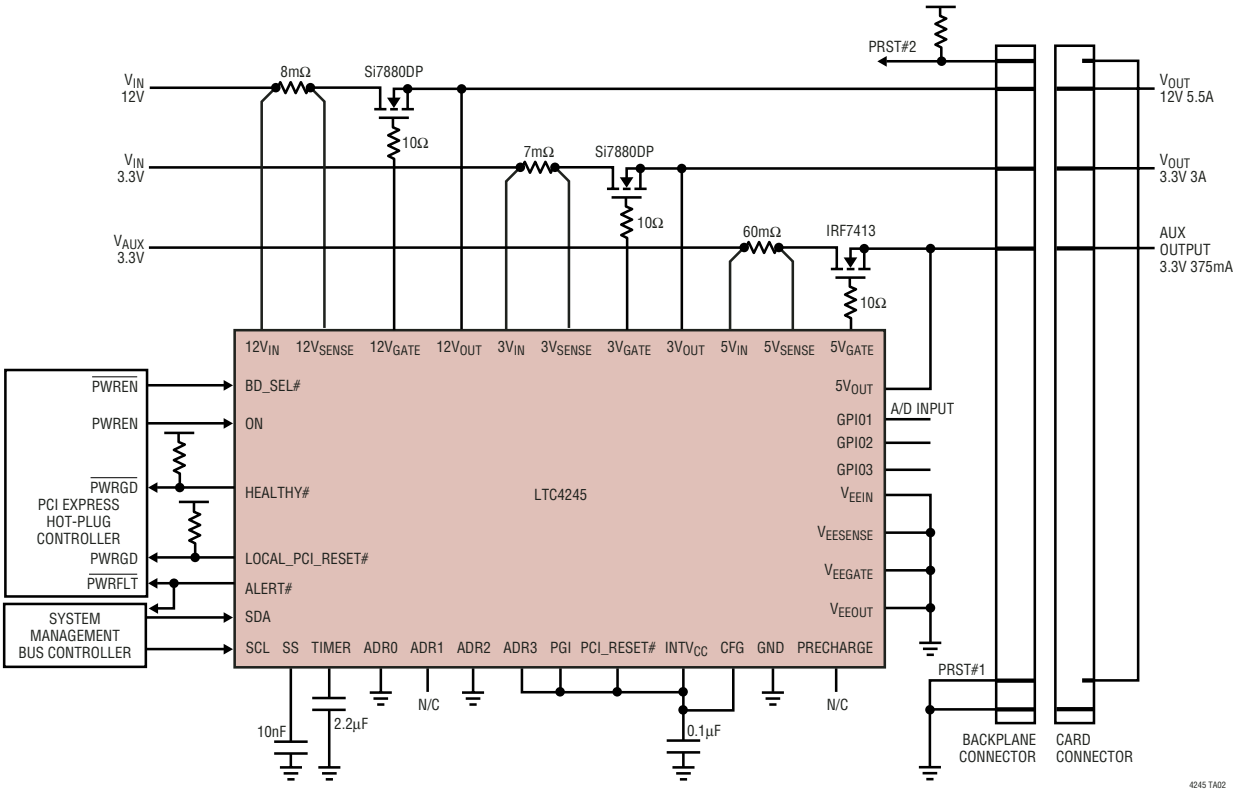


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

PCI Express Backplane Resident Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Hot Swap Controller	Dual Supplies from 3V to 12V, Additional –12V
LT®1641-1/LT1641-2	Positive High Voltage Hot Swap Controllers	9V to 80V, Latch Off/Autoretry, SO-8
LTC1642A	Fault Protected Hot Swap Controller	3V to 16.5V, Overvoltage Protection Up to 33V
LTC1643AL/LTC1643AL-1, LTC1643AH	PCI Bus Hot Swap Controllers	3.3V, 5V, ±12V Supplies for PCI Bus
LTC1645	Dual-Channel Hot Swap Controller/Power Sequencer	Operates from 1.2V to 12V, SO-8
LTC1646	CompactPCI Dual Hot Swap Controller	3.3V, 5V Supplies Only
LTC1647	Dual Hot Swap Controller	Dual ON Pins, 2.7V to 16.5V
LTC4211	Hot Swap Controller with Multifunction Current Control	Single Supply, 2.5V to 16.5V, MSOP
LTC4240	CompactPCI Hot Swap Controller with I²C I/O	3.3V, 5V, ±12V Supplies, Control and Status over I²C
LTC4241	PCI-Bus with 3.3V Auxiliary Hot Swap Controller	3.3V, 5V, ±12V and 3.3VAux Supplies for PCI Bus
LTC4244/LTC4244-1	Rugged CompactPCI Bus Hot Swap Controllers	3.3V, 5V, ±12V, Local Reset Logic and Precharge
LTC4252A	–48V Hot Swap Controller in MSOP	Fast Active Current Limiting with Drain Accelerated Response, Supply from –15V
LTC4260	Positive High Voltage Hot Swap Controller with I²C, ADC	I²C Interface and 8-bit ADC for Board Power Monitoring, 8.5V to 80V
LTC4302-1/LTC4302-2	Addressable 2-Wire Bus Buffers	Provides Capacitive Buffering, SDA and SCL Precharge and Level Shifting, Enabled by 2-Wire Bus Commands

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