NCV7420

LIN Transceiver with 3.3 V or 5 V Voltage Regulator

General Description

The NCV7420 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus. The transceiver is implemented in I3T technology enabling both high−voltage analog circuitry and digital functionality to co−exist on the same chip.

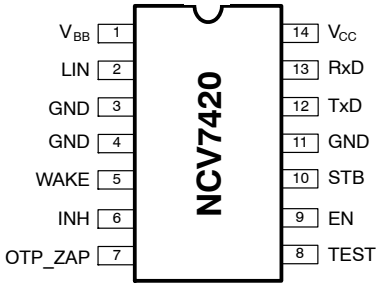
The NCV7420 LIN device is a member of the in−vehicle networking (IVN) transceiver family of ON Semiconductor that integrates a LIN v2.0/2.1 physical transceiver and either a 3.3 V or a 5 V voltage regulator. It is designed to work in harsh automotive environment and is submitted to the TS16949 qualification flow.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU−state machine that recognizes and translates the instructions specific to that function. The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

ON Semiconductor®

http://onsemi.com

PIN CONFIGURATION



SOIC 14
D SUFFIX
CASE 751AP

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

KEY FEATURES

LIN−Bus Transceiver

- LIN compliant to specification revision 2.0 and 2.1 (backward compatible to version 1.3) and J2602
- I3T high voltage technology
- Bus voltage ±45 V
- Transmission rate up to 20 kBaud
- SOIC 14 Green package
- This is a Pb−Free Device

Protection

- Thermal shutdown
- Indefinite short−circuit protection on pins LIN and WAKE towards supply and ground
- Load dump protection (45 V)
- Bus pins protected against transients in an automotive environment
- System ESD protection level for LIN, WAKE and Vbb up to ±12 kV

EMI Compatibility

- Integrated slope control
- Meets most demanding EMS/EME requirements

Voltage Regulator

- Output voltage 5 V / ~50 mA or 3.3 V / ~50 mA
- Wake−up input
- Enable inputs for stand−by and sleep mode
- INH output for auxiliary purposes (switching of an external pull−up or resistive divider towards battery, control of an external voltage regulator etc.)

Modes

- Normal mode: LIN communication in either low (up to 10 kBaud) or normal slope
- Sleep mode: V_{CC} is switched “off” and no communication on LIN bus
- Stand−by mode: V_{CC} is switched “on” but there is no communication on LIN bus
- Wake−up bringing the component from sleep mode into standby mode is possible either by LIN command or digital input signal on WAKE pin. Wake−up from LIN bus can also be detected and flagged when the chip is already in standby mode.

Quality

- Automotive Qualification According to AEC−Q100, Grade 1

Table 1. KEY TECHNICAL CHARACTERISTICS – 3.3 V version

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vbb	Nominal battery operating voltage	5	12	26	V
Vbb	Load dump protection (Note 1)			45	V
Ibb_SLP	Supply current in sleep mode			20	μA
Vcc_out (Note 3)	Regulated Vcc output, Vcc load 1 mA–30 mA	3.23	3.30	3.37	V
	Regulated Vcc output, Vcc load 0 mA–50 mA	3.19	3.30	3.41	V
Iout_max	Maximum Vcc output current (Note 2)	50			mA
V_wake	Operating DC voltage on WAKE pin	0		Vbb	V
	Maximum rating voltage on WAKE pin	−45		45	V
Tj	Junction thermal shutdown temperature	165		195	°C
Tjunc	Operating junction temperature	−40		+150	°C

Table 2. KEY TECHNICAL CHARACTERISTICS – 5 V version

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vbb	Nominal battery operating voltage	6	12	26	V
Vbb	Load dump protection (Note 1)			45	V
Ibb_SLP	Supply current in sleep mode			20	μA
Vcc_out (Note 3)	Regulated Vcc output, Vcc load 1 mA–30 mA	4.9	5.0	5.1	V
	Regulated Vcc output, Vcc load 0 mA–50 mA	4.83	5.0	5.17	V
Iout_max	Maximum Vcc output current (Note 2)	50			mA
V_wake	Operating DC voltage on WAKE pin	0		Vbb	V
	Maximum rating voltage on WAKE pin	−45		45	V
Tj	Junction thermal shutdown temperature	165		195	°C
Tjunc	Operating junction temperature	−40		+150	°C

1. The applied transients shall be in accordance with ISO 7637 part 1, test pulse 5. The device complies with functional class C; class A can be reached depending on the application and external components.
2. Thermal aspects of the entire end–application have to be taken into account in order to avoid thermal shutdown of NCV7420.
3. Vcc voltage must be properly stabilized by external capacitors: capacitor of min. 80 nF with ESR<10 mΩ in parallel with a capacitor of min. 8 μF, ESR<1Ω.

Table 3. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)\_1}$	Thermal resistance junction–to–ambient on JEDEC 1S0P PCB	free air	140	K/W
$R_{th(vj-a)\_4}$	Thermal resistance junction–to–ambient on JEDEC 2S2P PCB	free air	80	K/W

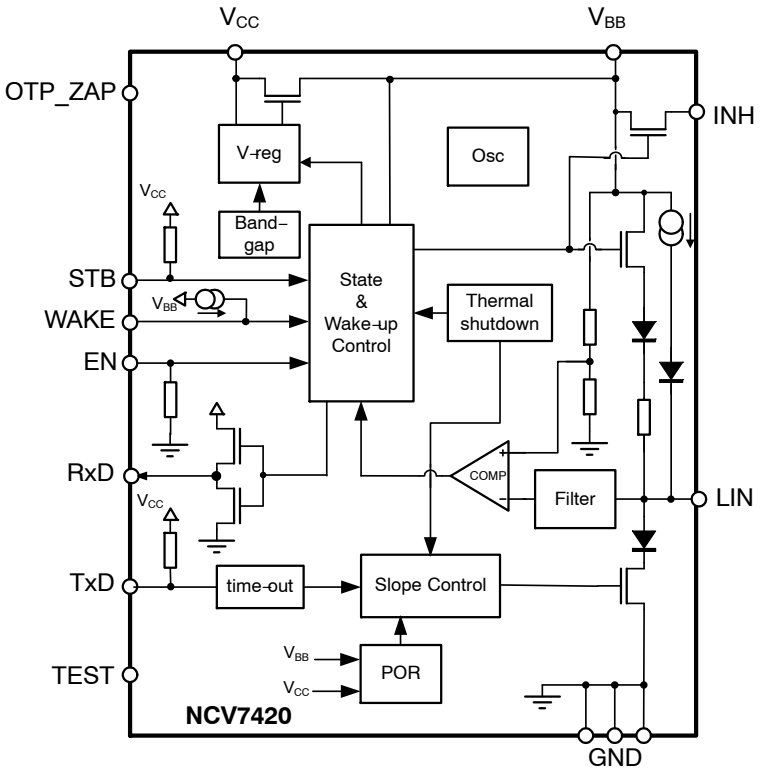


Figure 1. Block Diagram

Typical Application

Application Schematic

The EMC immunity of the Master−mode device can be further enhanced by adding a capacitor between the LIN output and ground. The optimum value of this capacitor is determined by the length and capacitance of the LIN bus, the number and capacitance of Slave devices, the pull−up resistance of all devices (Master & Slave), and the required time constant of the system, respectively.

Vcc voltage must be properly stabilized by external capacitors: capacitor of min. 80 nF (ESR < 10 mΩ) in parallel with a capacitor of min. 8 μF (ESR < 1 Ω).

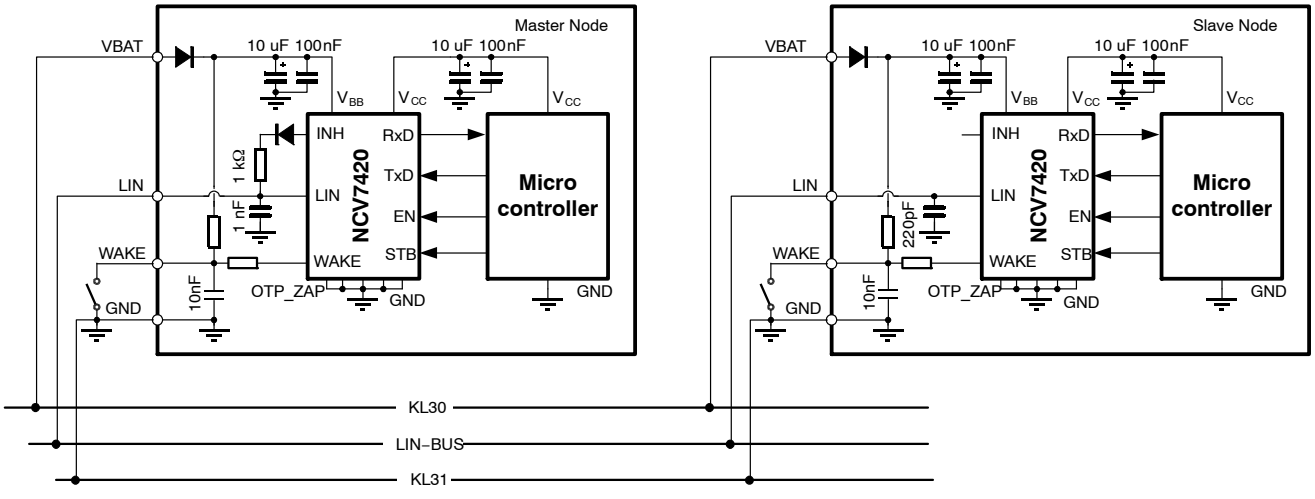


Figure 2. Typical Application Diagram

Table 4. PIN DESCRIPTION

Pin	Name	Description
1	VBB	Battery supply input
2	LIN	LIN bus output/input
3	GND	Ground
4	GND	Ground
5	WAKE	High voltage digital input pin to switch the part from sleep− to standby mode
6	INH	Inhibit output
7	OTP_ZAP	Supply for programming of trimming bits at factory testing, should be grounded in the application
8	TEST	Digital input for factory testing, should be grounded in the application
9	EN	Enable input, transceiver in normal operation mode when high
10	STB	Standby mode control input
11	GND	Ground
12	TxD	Transmit data input, low in dominant state
13	RxD	Receive data output; low in dominant state; push−pull output
14	Vcc	Supply voltage (output)

Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications. The domain is class−A multiplex buses with a single master node and a set of slave nodes.

NCV7420 is designed as a master or slave node for the LIN communication interface with an integrated 3.3 V or 5 V voltage regulator having a current capability up to 50 mA for supplying any external components (microcontroller).

NCV7420 contains the LIN transmitter, LIN receiver, voltage regulator, power−on−reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for the maximum specified transmission speed of 20 kBaud with EMC performance due to reduced slew rate of the LIN output.

The junction temperature is monitored via a thermal shutdown circuit that switches the LIN transmitter and voltage regulator off when temperature exceeds the TSD trigger level.

NCV7420 has four operating states (normal mode, low slope mode, stand−by mode, and sleep mode) that are determined by the input signals EN, WAKE, STB, and TxD.

Operating States

NCV7420 provides four operating states, two modes for normal operation with communication, one stand-by without communication and one low power mode with very low current consumption. See Figure 3.

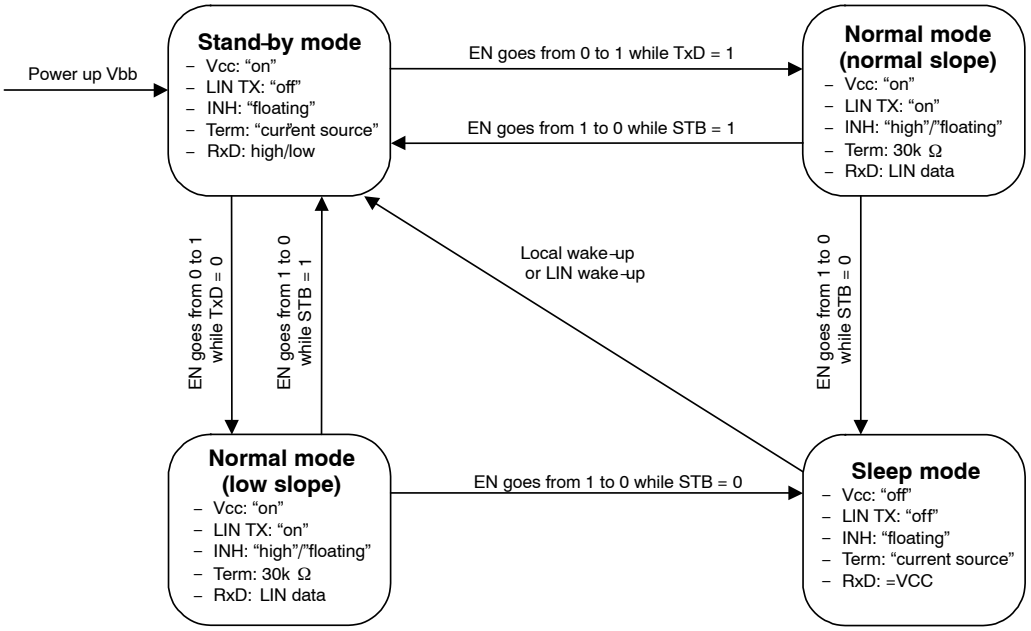


Figure 3. State Diagram

Table 5. MODE SELECTION

Mode	Vcc	RxD	INH	LIN	30 kΩ on LIN	Note
Normal – Slope	ON	Low = Dominant State High = Recessive State	High if STB=High during state transition; Floating otherwise	Normal Slope	ON	(Note 4)
Normal – Low Slope	ON	Low = Dominant State High = Recessive State	High if STB=High during state transition; Floating otherwise	Low Slope	ON	(Note 5)
Stand–by	ON	Low after LIN wakeup, high otherwise	Floating	OFF	OFF	(Note 6)
Sleep	OFF	Clamped to Vcc	Floating	OFF	OFF	

4. The normal slope mode is entered when pin EN goes HIGH while TxD is in HIGH state during EN transition.
5. The low slope mode is entered when pin EN goes HIGH while TxD is in LOW state during EN transition. LIN transmitter gets on only after TxD returns to high after the state transition.
6. The stand–by mode is entered automatically after power–up.

Normal Slope Mode

In normal slope mode the transceiver can transmit and receive data via LIN bus with speed up to 20 kBaud. The transmit data stream of the LIN protocol is present on the TxD pin and converted by the transmitter into a LIN bus signal with controlled slew rate to minimize EMC emission. The receiver consists of the comparator that has a threshold with hysteresis in respect to the supply voltage and an input filter to remove bus noise. The LIN output is pulled HIGH via an internal 30 kΩ pull-up resistor. For master applications it is needed to put an external 1 kΩ resistor with a serial diode between LIN and Vbb (or INH). See Figure 2. The mode selection is done by EN=HIGH when TxD pin is HIGH. If STB pin is high during the standby-to-normal slope mode transition, INH pin is pulled high. Otherwise, it stays floating.

Low Slope Mode

In low slope mode the slew rate of the signal on the LIN bus is reduced (rising and falling edges of the LIN bus signal are longer). This further reduces the EMC emission. As a consequence the maximum speed on the LIN bus is reduced up to 10 kBaud. This mode is suited for applications where the communication speed is not critical. The mode selection is done by EN=HIGH when TxD pin is LOW. In order not to transmit immediately a dominant state on the bus (because TxD=LOW), the LIN transmitter is enabled only after TxD returns to HIGH. If STB pin is high during the standby−to−low slope mode transition, INH pin is pulled high. Otherwise, it stays floating.

Stand−by Mode

The stand−by mode is always entered after power−up of the NCV7420. It can also be entered from normal mode when the EN pin is low and the stand−by pin is high. From sleep mode it can be entered after a local wake−up or LIN wakeup. In stand−by mode the Vcc voltage regulator for supplying external components (e.g. a microcontroller) stays active. Also the LIN receiver stays active to be able to detect a remote wake−up via bus. The LIN transmitter is

disabled and the slave internal termination resistor of 30 kΩ between LIN and Vbb is disconnected in order to minimize current consumption. Only a pull−up current source between Vbb and LIN is active.

Sleep Mode

The Sleep Mode provides extreme low current consumption. This mode is entered when both EN and STB pins are LOW coming from normal mode. The internal termination resistor of 30 kΩ between LIN and Vbb is disconnected and also the Vcc regulator is switched off to minimize current consumption.

Wake−up

NCV7420 has two possibilities to wake−up from sleep or stand−by mode (see Figure 3):

- Local wake−up: enables the transition from sleep mode to stand−by mode
- Remote wake−up via LIN: enables the transition from sleep− to stand−by mode and can be also detected when already in standby mode.

A local wake−up is **only** detected in sleep mode if a transition from LOW to HIGH or from HIGH to LOW is seen on the wake pin.

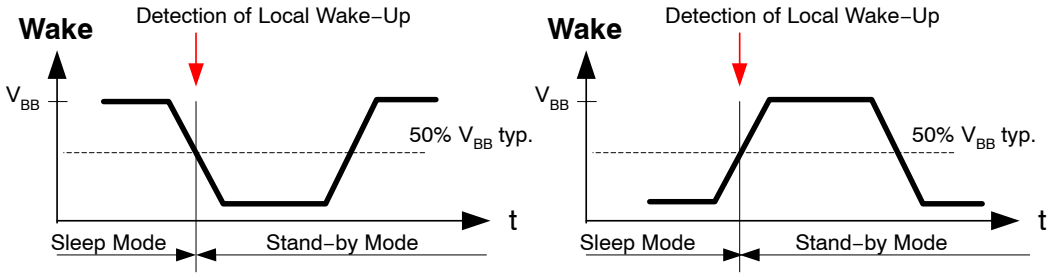


Figure 4. Local Wake−up Signal

A remote wake−up is **only** detected if a combination of (1) a falling edge at the LIN pin (transition from recessive to dominant) is followed by (2) a dominant level maintained for a time period > t_{WAKE} and (3) again a rising edge at pin LIN (transition from dominant to recessive) happens.

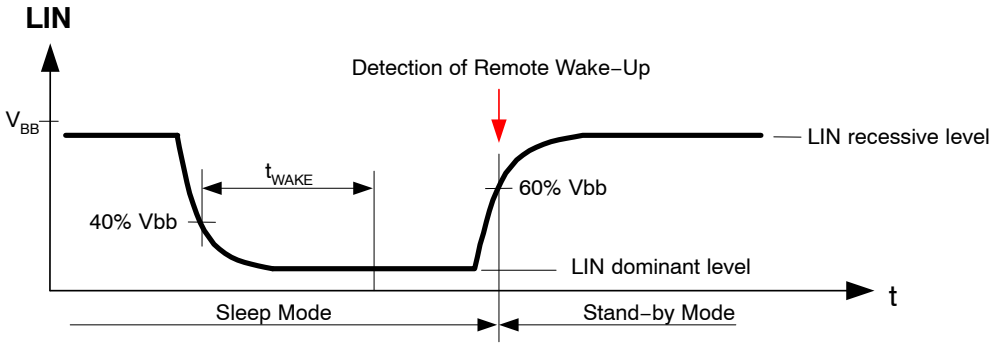


Figure 5. Remote Wake−up Behavior

The wake−up source is distinguished by pin RxD in the stand−by mode:

- RxD remains HIGH after power−up or local wake−up.
- RxD is kept LOW until normal mode is entered after a remote wake−up (LIN).

Electrical Characteristics

Definitions

All voltages are referenced to GND (Pin 13). Positive currents flow into the IC.

Table 6. ABSOLUTE MAXIMUM RATINGS – 3.3 V and 5 V versions

Symbol	Parameter	Min.	Max.	Unit
Vbb	Battery voltage on pin Vbb (Note 7)	−0.3	+45	V
Vcc	DC voltage on pin Vcc	0	+7	V
I_Vcc	Current delivered by the Vcc regulator	50		mA
V_LIN	LIN bus voltage (Note 8)	−45	+45	V
V_INH	DC voltage on inhibit pin	−0.3	Vbb + 0.3	V
V_WAKE	DC voltage on WAKE pin	−45	45	V
V_Dig_in	DC input voltage on pins TxD, RxD, EN, STB	−0.3	Vcc + 0.3	V
Tjunc	Maximum junction temperature	−40	+165	°C
Vesd	Electrostatic discharge voltage on all pins; HBM (Note 9)	−2	+2	kV
	Electrostatic discharge voltage on LIN, INH, WAKE and Vbb towards GND; HBM (Note 9)	−4	+4	kV
	Electrostatic discharge on LIN, WAKE and Vbb; system HBM (Note 10)	−8	+8	kV
	Electrostatic discharge voltage on all pins; CDM (Note 12)	−500	+500	V
Vesd (EMC/ESD improved versions)	Electrostatic discharge voltage on all pins; HBM (Note 9)	−4	+4	kV
	Electrostatic discharge voltage on LIN, INH, WAKE and Vbb towards GND; HBM (Note 9)	−6	+6	kV
	Electrostatic discharge on LIN, WAKE and Vbb; system HBM (Note 11)	−12	+12	kV
	Electrostatic discharge voltage on all pins; CDM (Note 12)	−750	+750	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

7. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, and 5. The device complies with functional class C; class A can be reached depending on the application and external components.
8. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b. The device complies with functional class C; class A can be reached depending on the application and external components.
9. Equivalent to discharging a 100 pF capacitor through a 1500 Ω resistor.
10. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor conform to IEC Standard 1000−4−2. LIN bus filter 220 pF, Vbb blocking capacitor 100 nF, 3k3/10n R/C network on WAKE.
11. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor conform to IEC Standard 1000−4−2. No filter on LIN, Vbb blocking capacitor 100 nF, 3k3/10n R/C network on WAKE.
12. Charged device model according ESD-STM5.3.1.

DC Characteristics – 3.3 V version (V_{BB} = 5 V to 26 V; T_{junc} = −40°C to +150°C; unless otherwise specified.)

Table 7. DC CHARACTERISTICS SUPPLY − Pins VBB and VCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ibb_ON	Supply current	Normal mode; LIN recessive			1	mA
Ibb_STB	Supply current	Stand−by mode, Vbb = 5−18 V, T_{junc} < 105°C			60	μA
Ibb_SLP	Supply current	Sleep mode, Vbb = 5−18 V, T_{junc} < 105°C			20	μA
Vcc_out	Regulator output voltage	Vcc load 1 mA − 30 mA	3.23	3.30	3.37	V
	Regulator output voltage	Vcc load 0 mA − 50 mA	3.19	3.30	3.41	V
Iout_max_abs	Absolute maximum output current	Thermal shutdown must be taken into account			50	mA
Iout_lim	Over−current limitation		50		170	mA

Table 8. DC CHARACTERISTICS LIN TRANSMITTER − Pin LIN

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VLin_dom_LoSup	LIN dominant output voltage	TXD = low; Vbb = 7.3 V			1.2	V
VLin_dom_HiSup	LIN dominant output voltage	TXD = low; Vbb = 18 V			2.0	V
VLin_rec	LIN recessive output voltage	TXD = highH; Ilin = 0 mA	Vbb − Vγ (Note 13)			V
ILIN_lim	Short circuit current limitation	VLin = Vbb_max	40		200	mA
Rslave	Internal pull−up resistance		20	33	47	kΩ
ILIN_off_dom	LIN output current bus in dominant state	Driver off; Vbb = 12 V	−1			mA
ILIN_off_rec	LIN output current bus in recessive state	Driver off; Vbb < 18 V Vbb < VLin < 18 V			1	μA
ILIN_no_GND	Communication not affected	Vbb = GND = 12 V; 0 < VLin < 18 V	−1		1	mA
ILIN_no_Vbb	LIN bus remains operational	Vbb = GND = 0 V; 0 < VLin < 18 V			5	μA

Table 9. DC CHARACTERISTICS LIN RECEIVER − Pin LIN

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Vbus_dom	Bus voltage for dominant state				0.4	Vbb
Vbus_rec	Bus voltage for recessive state		0.6			Vbb
Vrec_dom	Receiver threshold	LIN bus recessive → dominant	0.4		0.6	Vbb
Vrec_rec	Receiver threshold	LIN bus dominant → recessive	0.4		0.6	Vbb
Vrec_cnt	Receiver centre voltage	(Vbus_dom + Vbus_rec) / 2	0.475		0.525	Vbb
Vrec_hys	Receiver hysteresis		0.05		0.175	Vbb

13. Vγ is the forward diode voltage. Typically (over the complete temperature) Vγ = 1 V.
14. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420_3 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.

DC Characteristics – 3.3 V version (V_{BB} = 5 V to 26 V; T_{junc} = −40°C to +150°C; unless otherwise specified.)

Table 10. DC CHARACTERISTICS I/Os

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pin WAKE						
V_wake_th	Threshold voltage		0.35		0.65	Vbb
I_leak	Input leakage current (Note 14)	Vwake = 0 V; Vbb = 18 V	−1	−0.5	1	μA
T_wake_min	Debounce time	Sleep mode; rising and falling edge	8		54	μs
Pins TxD and STB						
Vil	Low level input voltage				0.8	V
Vih	High level input voltage		2.0			V
Rpu	Pull−up resistance to Vcc (Note 14)		50		200	kΩ
Pin INH						
Delta_VH	High level voltage drop	IINH = 15 mA		0.35	0.75	V
I_leak	Leakage current	Sleep mode; VINH = 0 V	−1		1	μA
Pin EN						
Vil	Low level input voltage				0.8	V
Vih	High level input voltage		2.0			V
Rpd	Pull−down resistance to ground (Note 14)		50		200	kΩ
Pin RxD						
Vol	Low level output voltage	Isink = 2 mA			0.65	V
Voh	High level output voltage	Isource = −2 mA	Vcc − 0.65 V			V

Table 11. DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POR						
PORH_Vbb	POR high level Vbb comparator				4.5	V
PORL_Vbb	POR low level Vbb comparator		1.7			V
POR_Vbb_sl	Maximum slope on Vbb to guarantee POR				50	V/ms
PORH_Vcc	POR high level Vcc comparator				3	V
PORL_Vcc	POR low level Vcc comparator		2			V
TSD						
Tj	Junction temperature	For shutdown	165		195	°C
Tj_hyst	Thermal shutdown hysteresis		9		18	°C

13. Vγ is the forward diode voltage. Typically (over the complete temperature) Vγ = 1 V.
14. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420_3 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.

DC Characteristics – 5 V version – (V_{BB} = 6 V to 26 V; T_{junc} = −40°C to +150°C; unless otherwise specified.)

Table 12. DC CHARACTERISTICS SUPPLY – Pins VBB and VCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ibb_ON	Supply current	Normal mode; LIN recessive			1	mA
Ibb_STB	Supply current	Stand−by mode, Vbb = 6–18 V, T_{junc} < 105°C			60	μA
Ibb_SLP	Supply current	Sleep mode, Vbb = 6–18 V, T_{junc} < 105°C			20	μA
Vcc_out	Regulator output voltage	Vcc load 1 mA – 30 mA	4.9	5.0	5.1	V
	Regulator output voltage	Vcc load 0 mA – 50 mA	4.83	5.0	5.17	V
Iout_max_abs	Absolute maximum output current	Thermal shutdown must be taken into account			50	mA
Iout_lim	Over−current limitation		50		170	mA

Table 13. DC CHARACTERISTICS LIN TRANSMITTER – Pin LIN

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VLin_dom_LoSup	LIN dominant output voltage	TXD = low; Vbb = 7.3 V			1.2	V
VLin_dom_HiSup	LIN dominant output voltage	TXD = low; Vbb = 18 V			2.0	V
VLin_rec	LIN recessive output voltage	TXD = highH; Ilin = 0 mA	Vbb – Vγ (Note 15)			V
ILIN_lim	Short circuit current limitation	VLin = Vbb_max	40		200	mA
Rslave	Internal pull−up resistance		20	33	47	kΩ
ILIN_off_dom	LIN output current bus in dominant state	Driver off; Vbb = 12 V	−1			mA
ILIN_off_rec	LIN output current bus in recessive state	Driver off; Vbb < 18 V Vbb < VLin < 18 V			1	μA
ILIN_no_GND	Communication not affected	Vbb = GND = 12 V; 0 < VLin < 18 V	−1		1	mA
ILIN_no_Vbb	LIN bus remains operational	Vbb = GND = 0 V; 0 < VLin < 18 V			5	μA

Table 14. DC CHARACTERISTICS LIN RECEIVER – Pin LIN

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Vbus_dom	Bus voltage for dominant state				0.4	Vbb
Vbus_rec	Bus voltage for recessive state		0.6			Vbb
Vrec_dom	Receiver threshold	LIN bus recessive → dominant	0.4		0.6	Vbb
Vrec_rec	Receiver threshold	LIN bus dominant → recessive	0.4		0.6	Vbb
Vrec_cnt	Receiver center voltage	(Vbus_dom + Vbus_rec) / 2	0.475		0.525	Vbb
Vrec_hys	Receiver hysteresis		0.05		0.175	Vbb

15. Vγ is the forward diode voltage. Typically (over the complete temperature) Vγ = 1 V.
16. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420_5 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.

DC Characteristics – 5 V version – (V_{BB} = 6 V to 26 V; T_{junc} = −40°C to +150°C; unless otherwise specified.)

Table 15. DC CHARACTERISTICS I/OS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Pin WAKE						
V_wake_th	Threshold voltage		0.35		0.65	Vbb
I_leak	Input leakage current (Note 16)	Vwake = 0 V; Vbb = 18 V	−1	−0.5	1	μA
T_wake_min	Debounce time	Sleep mode; rising and falling edge	8		54	μs
Pins TxD and STB						
Vil	Low level input voltage				0.8	V
Vih	High level input voltage		2.0			V
Rpu	Pull−up resistance to Vcc (Note 16)		50		200	kΩ
Pin INH						
Delta_VH	High level voltage drop	IINH = 15 mA		0.35	0.75	V
I_leak	Leakage current	Sleep mode; VINH = 0 V	−1		1	μA
Pin EN						
Vil	Low level input voltage				0.8	V
Vih	High level input voltage		2.0			V
Rpd	Pull−down resistance to ground (Note 16)		50		200	kΩ
Pin RxD						
Vol	Low level output voltage	Isink = 2 mA			0.65	V
Voh	High level output voltage	Isource = −2 mA	Vcc − 0.65 V			V

Table 16. DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POR						
PORH_Vbb	POR high level Vbb comparator				4.5	V
PORL_Vbb	POR low level Vbb comparator		1.7			V
POR_Vbb_sl	Maximum slope on Vbb to guarantee POR				50	V/ms
PORH_Vcc	POR high level Vcc comparator				4.5	V
PORL_Vcc	POR low level Vcc comparator		3			V
TSD						
Tj	Junction temperature	For shutdown	165		195	°C
Tj_hyst	Thermal shutdown hysteresis		9		18	°C

15. Vγ is the forward diode voltage. Typically (over the complete temperature) Vγ = 1 V.
16. By one of the trimming bits, following reconfiguration can be done during chip−level testing in order to fit the NCV7420_5 into different interface: pins TxD and EN will have typ. 10 kΩ pull−down resistor to ground and pin WAKE will have typ. 10 μA pull−up current source.

AC Characteristics – 3.3 V and 5 V versions – (V_{BB} = 7 V to 18 V; T_{junc} = −40°C to +150°C; unless otherwise specified.)

Table 17. AC CHARACTERISTICS LIN TRANSMITTER − Pin LIN

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x T_{Bit})	$TH_{REC(max)}$ = 0.744 x V_{BB} $TH_{DOM(max)}$ = 0.581 x V_{BB} T_{BIT} = 50 μs $V(V_{BB})$ = 7 V to 18 V	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x T_{Bit})	$TH_{REC(min)}$ = 0.422 x V_{BB} $TH_{DOM(min)}$ = 0.284 x V_{BB} T_{BIT} = 50 μs $V(V_{BB})$ = 7.6 V to 18 V	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x T_{Bit})	$TH_{REC(max)}$ = 0.778 x V_{BB} $TH_{DOM(max)}$ = 0.616 x V_{BB} T_{BIT} = 96 μs $V(V_{BB})$ = 7 V to 18 V	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x T_{Bit})	$TH_{REC(min)}$ = 0.389 x V_{BB} $TH_{DOM(min)}$ = 0.251 x V_{BB} T_{BIT} = 96 μs $V(V_{BB})$ = 7.6 V to 18 V	0.5		0.590	
T_fall_norm	LIN falling edge	Normal slope mode; V_{BB} = 12 V; L1, L2 (Note 17)			22.5	μs
T_rise_norm	LIN rising edge	Normal slope mode; V_{BB} = 12 V; L1, L2 (Note 17)			22.5	μs
T_sym_norm	LIN slope symmetry	Normal slope mode; V_{BB} = 12 V; L1, L2 (Note 17)	−4		4	μs
T_fall_norm	LIN falling edge	Normal slope mode; V_{BB} = 12 V; L3 (Note 17)			27	μs
T_rise_norm	LIN rising edge	Normal slope mode; V_{BB} = 12 V; L3 (Note 17)			27	μs
T_sym_norm	LIN slope symmetry	Normal slope mode; V_{BB} = 12 V; L3 (Note 17)	−5		5	μs
T_fall_low	LIN falling edge	Low slope mode (Note 18); V_{BB} = 12 V; L3 (Note 17)			62	μs
T_rise_low	LIN rising edge	Low slope mode (Note 18); V_{BB} = 12 V; L3 (Note 17)			62	μs
T_wake	Dominant time−out for wake−up via LIN bus		30		150	μs
T_dom	TxD dominant time−out	TxD = low	6		20	ms

17. The AC parameters are specified for following RC loads on the LIN bus: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF.
18. Low slope mode is not compliant to the LIN standard.

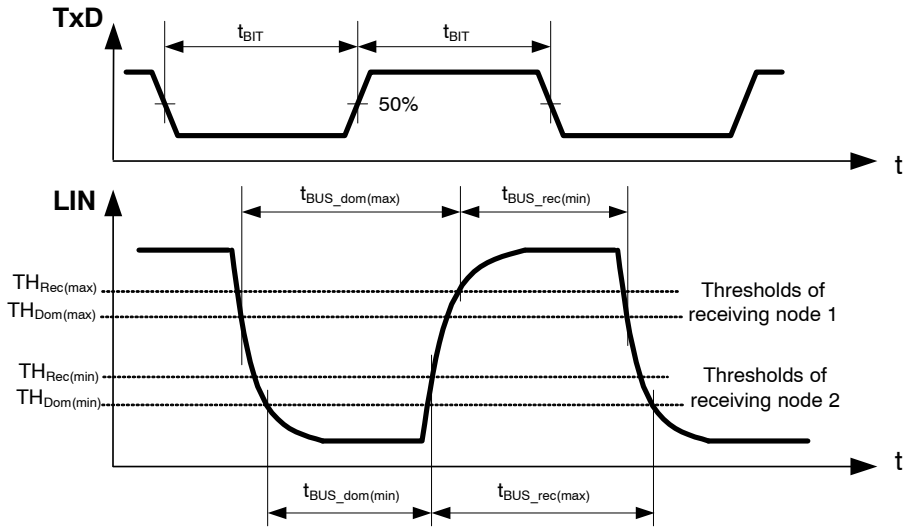


Figure 6. LIN Transmitter Duty Cycle

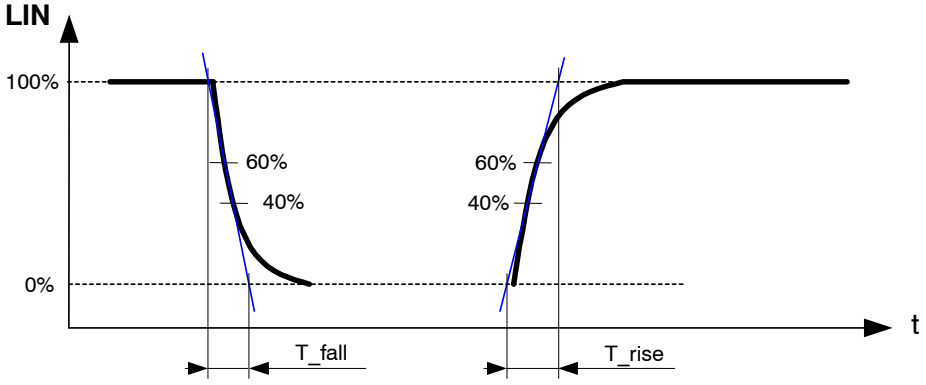


Figure 7. LIN Transmitter Rising and Falling Times

Table 18. AC CHARACTERISTICS LIN RECEIVER

Symbol Pin LIN	Parameter	Conditions	Min.	Typ.	Max.	Unit
Trec_prop_down	Propagation delay of receiver falling edge		0.1		6	µs
Trec_prop_up	Propagation delay of receiver rising edge		0.1		6	µs
Trec_sym	Propagation delay symmetry	Trec_prop_down – Trec_prop_up	−2		2	µs

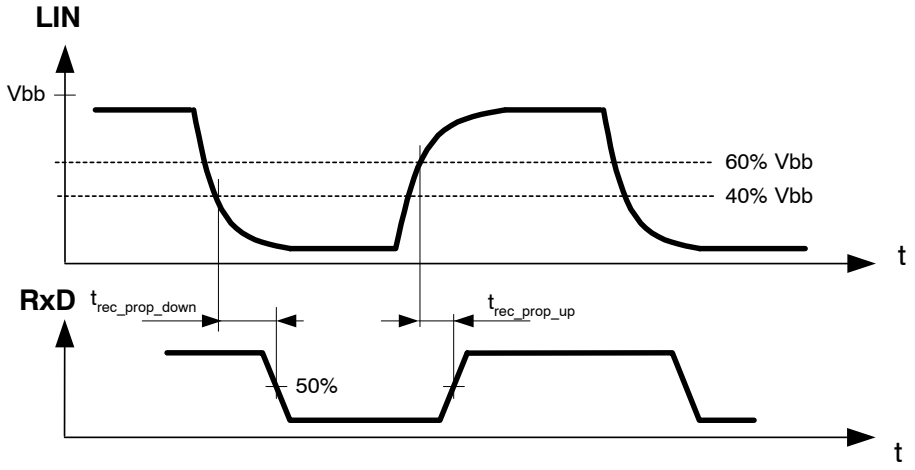


Figure 8. LIN Receiver Timing

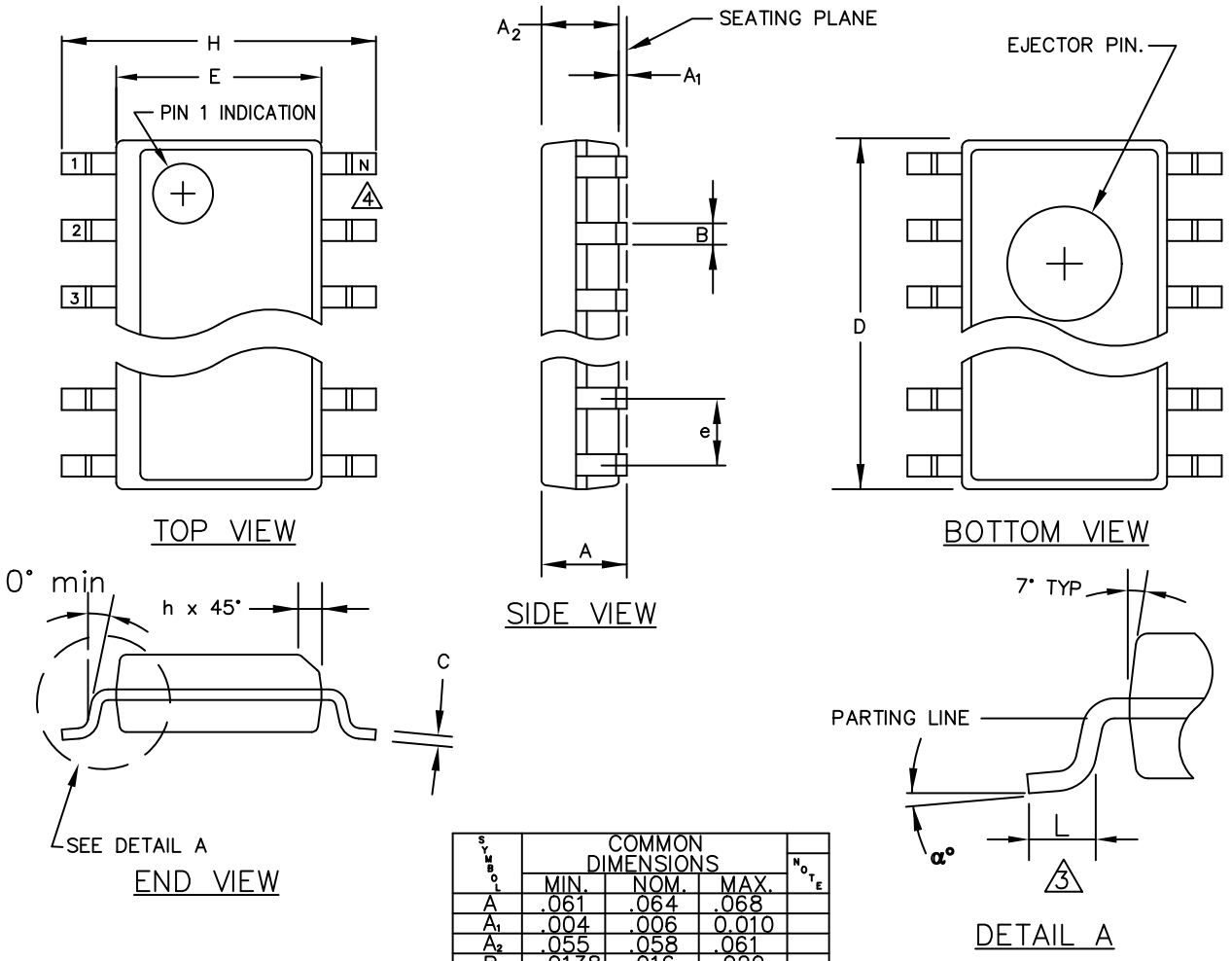
ORDERING INFORMATION

Part Number	Description	Package	Container		Temperature Range
			Shipping†	Qty.	
NCV7420D23G	LIN Transceiver + 3.3 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tube/Rail	55	−40°C to 125°C
NCV7420D23R2G	LIN Transceiver + 3.3 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tape & Reel	3000	−40°C to 125°C
NCV7420D24G	EMC/ESD Improved LIN Transceiver + 3.3 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tube/Rail	55	−40°C to 125°C
NCV7420D24R2G	EMC/ESD Improved LIN Transceiver + 3.3 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tape & Reel	3000	−40°C to 125°C
NCV7420D25G	LIN Transceiver + 5 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tube/Rail	55	−40°C to 125°C
NCV7420D25R2G	LIN Transceiver + 5 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tape & Reel	3000	−40°C to 125°C
NCV7420D26G	EMC/ESD Improved LIN Transceiver + 5 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tube/Rail	55	−40°C to 125°C
NCV7420D26R2G	EMC/ESD Improved LIN Transceiver + 5 V Vreg.	SOIC 150 14 GREEN (JEDEC MS−012)	Tape & Reel	3000	−40°C to 125°C

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOIC 14
CASE 751AP−01
ISSUE A



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	.061	.064	.068	
A_1	.004	.006	0.010	
A_2	.055	.058	.061	
B	.0138	.016	.020	
C	.0075	.008	.0098	
D	SEE VARIATIONS			1
E	.150	.155	.157	
e	.050 BSC			
H	.230	.236	.244	
h	.010	.013	.016	
L	.016	.025	.035	
N	SEE VARIATIONS			2
α°	0°	5°	8°	

VARIATIONS				
	1			2
	D			N
NOTE	MIN.	NOM.	MAX.	
AA	.189	.194	.196	8
AB	.337	.342	.344	14
AC	.386	.391	.393	16

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