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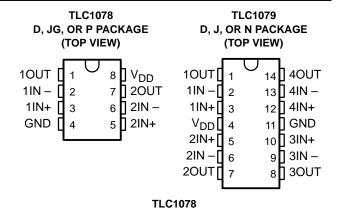
- Power Dissipation as Low as 10 μW Typ Per **Amplifier**
- Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min
- V_{IO} . . . 450 μ V/850 μ V Max in DIP and Small-Outline Package (TLC1078/79)
- Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days
- High-impedance LinCMOS™ Inputs $I_{IB} = 0.6 \text{ pA Typ}$
- High Open-Loop Gain . . . 800 000 Typ
- Output Drive Capability > 20 mA
- Slew Rate . . . 47 V/ms Typ
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative** Rail
- **On-Chip ESD-Protection Circuitry**
- **Small-Outline Package Option Also** Available in Tape and Reel

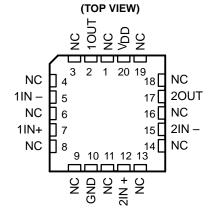
description

The TLC107x operational amplifiers offer ultralow offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-μW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC107xC is an ideal solution for low-voltage battery-operated systems. The 20-mA output drive capability means that the TLC107x can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

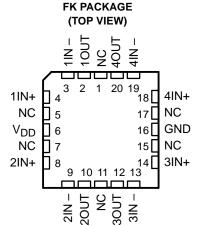
Since this device is functionally compatible as well as pin compatible with the TLC27L2/4 and TLC27L7/9, the TLC107x easily upgrades existing designs that can benefit from its improved performance.





TLC1079

FK PACKAGE



NC - No internal connection



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description (continued)

The TLC107x incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC107x design also inhibits latch-up of the device inputs and outputs even with surge currents as large 100 mA.

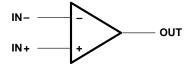
The C-suffix devices are characterized for operation from 0° C to 70° C. The I-suffix devices are characterized for operation from -40° C to 85° C. The M-suffix devices are characterized for operation over the full military temperature range of -55° C to 125° C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

	PACKAGED DEVICES								
TA	SMALL OUTLINET (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	FORM [‡] (Y)		
0°C to 70°C	TLC1078CD TLC1079CD	_	_	_	TLC1079CN	TLC1078CP	TLC1078Y TLC1079Y		
-40°C to 85°C	TLC1078ID TLC1079ID			_	TLC1079IN	TLC1078IP			
-55°C to 125°C	TLC1078MD TLC1079MD	TLC1078MFK TLC1079MFK	TLC1079MJ	TLC1078MJG	TLC1079MN	TLC1078MP	_		

[†] The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1078CDR).

symbol (each amplifier)



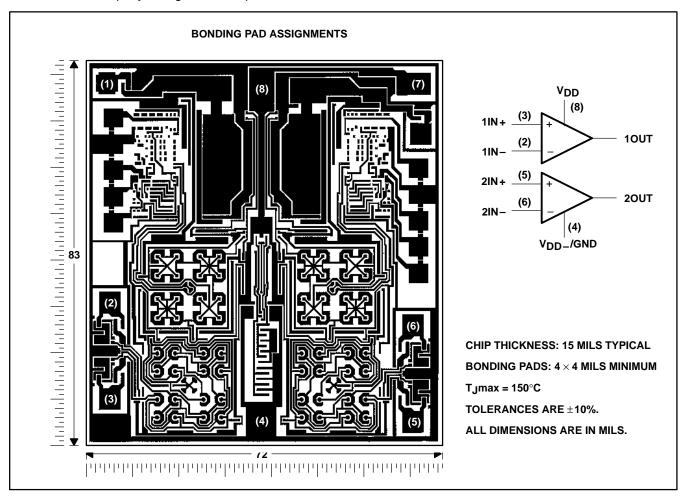


[‡] Chip forms are tested 25°C only.

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TLC1087Y chip information

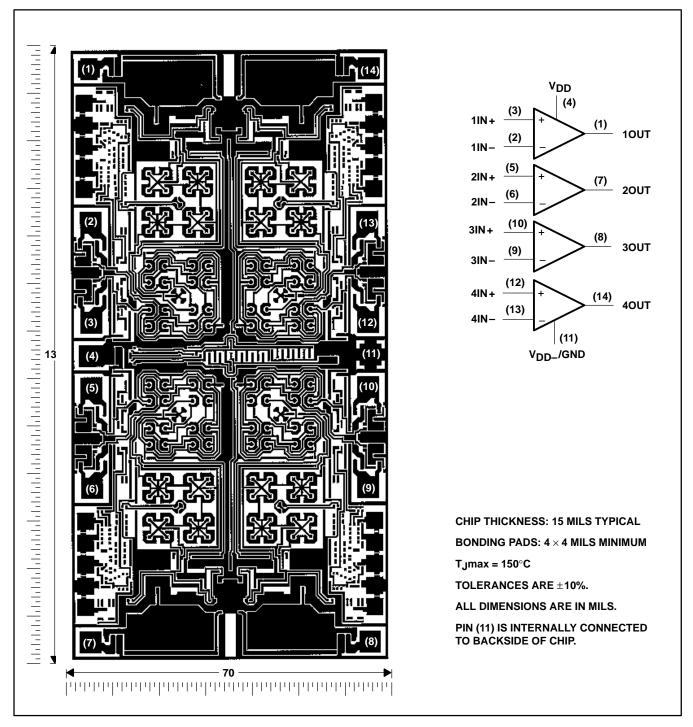
This chip, when properly assembled, displays characteristics similar to the TLC1078C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.



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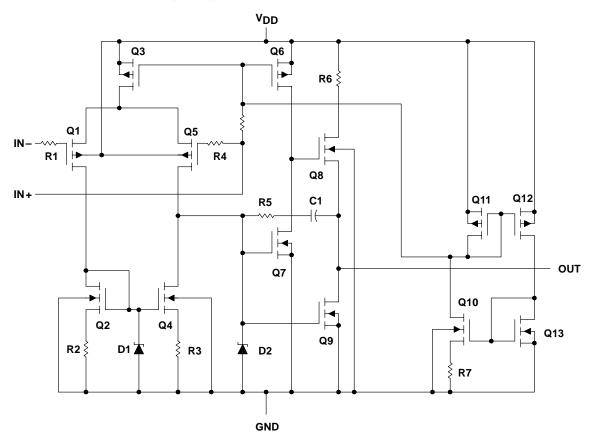
TLC1079Y chip information

This chip, when properly assembled, display characteristics similar to the TLC1079C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.





equivalent schematic (each amplifier)



ACTUAL DEV	ICE COMPONE	NT COUNT								
COMPONENT TLC1078 TLC1079										
Transistors	38	76								
Resistors	16	32								
Diodes	12	24								
Capacitors	2	4								

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{DD} (see Note 1)	18 V
Differential input voltage, V _{ID} (see Note 2)	±V _{DD}
Input voltage range, V _I (any input)	
Input current, I _I (each input)	±5 mA
Output current, I _O (each output)	±30 mA
Total current into V _{DD} (see Note 3)	45 mA
Duration of short-circuit at (or below) T _A = 25°C (see Note 3)	unlimited
Continuous total power dissipation	. see Dissipation Rating Table
Operating free-air temperature range, T _A : C suffix	0°C to 70°C
l suffix	–40°C to 85°C
M suffix	
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	ge 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at IN+ with respect to IN-.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings are not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{A}} \leq 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D-14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

			C SUFFIX		FIX	M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V _{DD}		1.4	16	3	16	4	16	V
Common mode input voltage V/-	V _{DD} = 5 V	-0.2	4	-0.2	4	0	4	V
Common-mode input voltage, V _{IC}	V _{DD} = 10 V	-0.2	9	-0.2	9	0	9	V
Operating free-air temperature, T _A		0	70	-40	85	-55	125	°C



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electrical characteristics at specified free-air temperature

						TLC1	078C			
	PARAMETER	TEST CONDITIONS	T _A †	V	_{DD} = 5	V	٧	_{DD} = 10	٧	UNIT
		OONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	
V	lanut affact valtage	V _O = 1.4 V,	25°C		160	450		180	600	\/
VIO	Input offset voltage	$R_S = 50 \Omega$,	Full range			800			950	μV
αΛΙΟ	Temperature coefficient of input offset voltage	$V_{IC} = 0,$ $R_{I} = 1 \text{ M}\Omega$	25°C to 70°C		1.1			1		μV/°C
1	Input offset surrent (see Note 4)		25°C		0.1	60		0.1	60	π Λ
ΙΟ	Input offset current (see Note 4)	$V_O = V_{DD}/2$	70°C		7	300		7	300	pΑ
l	Input bias current (see Note 4)	$V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	pА
IB	input bias current (see Note 4)		70°C		40	600		50	600	pΑ
V	Common-mode input voltage		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V
VICR	range (see Note 5)		Full range	-0.2 to 3.5			-0.2 to 8.5			٧
			25°C	3.2	4.1		8.2	8.9		
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $R_I = 1 \text{ M}\Omega$	0°C	3.2	4.1		8.2	8.9		V
•			70°C	3.2	4.2		8.2	8.9		
			25°C		0	25		0	25	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 0$	0°C		0	25		0	25	mV
		IOL - V	70°C		0	25		0	25	
		D 4140	25°C	250	525		500	850		
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	0°C	250	680		500	1010		V/mV
	amplification	Gee Note o	70°C	200	380		350	660		
			25°C	70	95		75	97		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	0°C	70	95		75	97		dB
			70°C	70	95		75	97		
			25°C	75	98		75	98		
ksvr	Supply-voltage rejection ratio (ΔVDD/ΔVIO)	V _O = 1.4 V	0°C	75	98		75	98		dB
	עט אין עט אין עט אין אין עט אין		70°C	75	98		75	98		
		$V_O = V_{DD}/2$,	25°C		20	34		29	46	
I_{DD}	Supply current (two amplifiers)	$V_{IC} = V_{DD}/2$	0°C		24	42		36	66	β μΑ
	N	No load	70°C		16	28		22	40	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

- 5. This range also applies to each input individually.
- 6. At $V_{DD} = 5 \text{ V}$. $V_{O} = 0.25 \text{ V}$ to 2 V; at $V_{DD} = 10 \text{ V}$, $V_{O} = 1 \text{ V}$ to 6 V.



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electrical characteristics at specified free-air temperature

						TLC1	079C			
	PARAMETER	TEST CONDITIONS	T _A †	V	_{DD} = 5 \	/	V	_{DD} = 10	٧	UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
\/	lanut effect valence		25°C		190	850		200	1150	\/
VIO	Input offset voltage	$V_O = 1.4 \text{ V}, V_{IC} = 0,$	Full range			1200			1500	μV
αΛΙΟ	Temperature coefficient of input offset voltage	$R_S = 50 \Omega$, $R_I = 1 M\Omega$	25°C to 70°C		1.1			1		μV/°C
l. a	Input offset current		25°C		0.1	60		0.1	60	A
ΙΟ	(see Note 4)	$V_O = V_{DD}/2$,	70°C		7	300		7	300	pΑ
l.s	Input bias current	$V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	pА
ΙΒ	(see Note 4)		70°C		40	600		50	600	pΑ
\/	Common mode input		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V
VICR	voltage range (see Note 5)		Full range	-0.2 to 3.5			-0.2 to 8.5			V
			25°C	3.2	4.1		8.2	8.9		
Vон	High-level output voltage	V_{ID} = 100 mV, R _L = 1 M Ω	0°C	3.2	4.1		8.2	8.9		V
			70°C	3.2	4.2		8.2	8.9		
			25°C		0	25		0	25	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 0$	0°C		0	25		0	25	mV
		IOL = V	70°C		0	25		0	25	
			25°C	250	525		500	850		
A_{VD}	Large-signal differential voltage amplification	$R_L = 1 M\Omega$, See Note 6	0°C	250	700		500	1010		V/mV
	voltage amplification		70°C	200	380		350	660		
			25°C	70	95		75	97		
CMRR	Common mode rejection ratio	V _{IC} = V _{ICR} min	0°C	70	95		75	97		dB
	Tullo		70°C	70	95		75	97		
	0 1 1 1 1	.,	25°C	75	98		75	98		
ksvr	Supply-voltage rejection ratio (∆VDD/∆VIO)	$V_{DD} = 5 \text{ V to } 10 \text{ V},$ $V_{O} = 1.4 \text{ V}$	0°C	75	98		75	98		dB
		VO = 1.4 V	70°C	75	98		75	98		
	Cumply ourront /form	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	25°C		40	68		57	92	
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	0°C		48	84		72	132	μΑ
	ampimers) v		70°C		31	56		44	80	

[†]Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

- 5. This range also applies to each input individually.
- 6. At $V_{DD} = 5 \text{ V}$, $V_{O} = 0.25 \text{ V}$ to 2 V; at $V_{DD} = 10 \text{ V}$, $V_{O} = 1 \text{ V}$ to 6 V.



operating characteristics at specified free-air temperature

							TLC1	078C												
	PARAMETER	TEST CO	TEST CONDITIONS		TEST CONDITIONS		TEST CONDITIONS		TEST CONDITIONS		TEST CONDITIONS		TEST CONDITIONS T _A V _{DD} = 5 V		/	V _{DD} = 10 V			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX										
		5	C _L = 20 pF, See Figure 1	25°C		32			47											
SR	Slew rate at unity gain			0°C		35			51		V/ms									
		VI(PP) = 1 V,		70°C		27		38												
٧n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$	25°C		68			68		nV/√ Hz									
		C _L = 20 pF, See F	C _L = 20 pF,	C _L = 20 pF,	C _L = 20 pF, See Figu				See Figure 2	20 pF, See Figure 2	oF, See Figure 2		25°C		85			110		
В1	Unity-gain bandwidth					See Figure 2	pF, See Figure 2	See Figure 2				0°C		100			125			
				70°C		65			90											
				25°C		34°			38°											
φm	Phase margin at unity gain	C _L = 20 pF, See Figure 2	C _L = 20 pF, See Figure 2	C _L = 20 pF, See Figure 2	C _L = 20 pF, See Figure 2	nity gain $C_L = 20 \text{ pF}$, See Figure	n at unity gain $C_L = 20 \text{ pF}$, See Figure 2	Phase margin at unity gain $C_L = 20 \text{ pF}$, See Figure 2	See Figure 2	See Figure 2	pF, See Figure 2	0°C		36°		-	40°			
				70°C		30°			34°											

operating characteristics at specified free-air temperature

							TLC1	079C									
	PARAMETER	TEST CONDITIONS		TEST CONDITIONS		TEST CONDITIONS TA VDI		DD = 5 \	1	V _{DD} = 10 V			UNIT				
					MIN	TYP	MAX	MIN	TYP	MAX							
			C: - 20 pE	25°C		32			47								
SR	Slew rate at unity gain	$R_L = 1 M\Omega$, $C_L = 20 pF$, $V_{I(PP)} = 1 V$, See Figure 1	0°C		35			51		V/ms							
	I VI(PP)		70°C	27			38										
٧n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$	25°C		68			68		nV/√ Hz						
		C _L = 20 pF, See Figure 2	C _L = 20 pF, S	C _L = 20 pF,			See Figure 2	F, See Figure 2	25°C		85			110			
B ₁	Unity-gain bandwidth				C _L = 20 pF, See Figure 2	$C_L = 20 pF$,			pF, See Figure 2	See Figure 2	pF, See Figure 2	L = 20 pF, See Figure 2	0°C		100		
				70°C		65			90								
				25°C		34°			38°								
φm	Phase margin at unity gain	C _L = 20 pF, See Figure 2	C _L = 20 pF, See Figure 2	C _L = 20 pF, See Figure 2	C _L = 20 pF, See Figure 2	hase margin at unity gain $C_L = 20 \text{ pF}$, See Figure	See Figure 2	See Figure 2	20 pF, See Figure 2	0°C		36°	, and the second		40°		
				70°C		30°			34°								

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electrical characteristics at specified free-air temperature

						TLC	10781			
	PARAMETER	TEST CONDITIONS	τ _Α †	\	_{DD} = 5 \	V	٧	_{DD} = 10	٧	UNIT
		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	
V/	lanut effect voltege		25°C		160	450		180	600	μV
VIO	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	Full range			950			1100	μν
αΛΙΟ	Temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_I = 1 M\Omega$	25°C to 85°C		1.1			1		μV/°C
li o	Input offset current		25°C		0.1	60		0.1	60	рA
ΙΟ	(see Note 4)	$V_O = V_{DD}/2$	85°C		24	1000		26	1000	рA
l	Input bias current (see Note 4)	$V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	π Λ
ΙΒ	input bias current (see Note 4)		85°C		200	2000		220	2000	pΑ
\/	Common-mode input voltage		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V
VICR	range (see Note 5)		Full range	-0.2 to 3.5			-0.2 to 8.5			V
Vон	High-level output voltage		25°C	3.2	4.1		8.2	8.9		
		$V_{ID} = 100 \text{ mV},$ $R_{I} = 1 \text{ M}\Omega$	-40°C	3.2	4.1		8.2	8.9		V
			85°C	3.2	4.2		8.2	8.9		
			25°C		0	25		0	25	
V_{OL}	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OI} = 0$	-40°C		0	25		0	25	mV
		I OL - V	85°C		0	25		0	25	
			25°C	250	525		500	850		
A_{VD}	Large-signal differential voltage amplification	$R_L = 1 M\Omega$, See Note 6	-40°C	250	900		500	1550		V/mV
	апринсацоп	OCC NOIC O	85°C	150	300		250	585		
			25°C	70	95		75	97		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	-40°C	70	95		75	97		dB
			85°C	70	95		75	97		
			25°C	75	98		75	98		
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _O = 1.4 V	-40°C	75	98		75	98		dB
SVK			85°C	75	98		75	98		
		$V_O = V_{DD}/2$,	25°C		20	34		29	46	
I_{DD}	Supply current (two amplifiers)		-40°C		31	54		50	86	μΑ
			85°C		15	26		20	36	

[†]Full range is -40°C to 80°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

- 5. This range also applies to each input individually.
- 6. At $V_{DD} = 5 \text{ V}$, $V_{O} = 0.25 \text{ V}$ to 2 V; at $V_{DD} = 10 \text{ V}$, $V_{O} = 1 \text{ V}$ to 6 V.



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electrical characteristics at specified free-air temperature

						TLC1	10791			
	PARAMETER	TEST CONDITIONS	T _A †	V	_{DD} = 5 \	/	V	_{DD} = 10	V	UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V	Innut offeet voltege		25°C		190	850		200	1150	\/
VIO	Input offset voltage	$V_O = 1.4 \text{ V}, V_{IC} = 0,$	Full range			1350			1650	μV
ανιο	Temperature coefficient of input offset voltage	$R_S = 50 \Omega$, $R_I = 1 M\Omega$	25°C to 85°C		1.1			1		μV/°C
li o	Input offset current		25°C		0.1	60		0.1	60	pА
IIO	(see Note 4)	$V_{O} = V_{DD}/2$,	85°C		24	1000		26	1000	ÞΑ
l.p	Input bias current	$V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	рA
lΒ	(see Note 4)		85°C		200	2000		220	2000	pΑ
\/.o.	Common-mode input voltage range		25°C	-0.2 to 4	-0.3 to 4.2		-0.2 to 9	-0.3 to 9.2		V
VICR	(see Note 5)		Full range	-0.2 to 3.5			-0.2 to 8.5			V
		.,,	25°C	3.2	4.1		8.2	8.9		
∨он	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $R_{I} = 1 \text{ M}\Omega$	-40°C	3.2	4.1		8.2	8.9		V
			85°C	3.2	4.2		8.2	8.9		
		., ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	25°C		0	25		0	25	
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 0$	−40°C		0	25		0	25	mV
		IOL - v	85°C		0	25		0	25	
	Laura d'arab d'ffancadal		25°C	250	525		500	850		
AVD	Large-signal differential voltage amplification	$R_L = 1 M\Omega$, See Note 6	−40°C	250	900		500	1550		V/mV
	voltago amplinoation		85°C	150	330		250	585		
			25°C	70	95		75	97		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	−40°C	70	95		75	97		dB
	rojoonori rano		85°C	70	95		75	97		
	Owner by continuous and another of	V 5.V (- 40.V	25°C	75	98		75	98		
ksvr	Supply-voltage rejection ratio (∆V _{DD} /∆V _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$ $V_{O} = 1.4 \text{ V}$	−40°C	75	98		75	98		dB
	(4400/4410/	VO = 1.4 V	85°C	75	98		75	98		
	Cupply ourrent	V V / 2	25°C		40	68		57	92	-
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	−40°C		62	108		98	172	
	(four amplifiers) V _I	10 100. 2, 110.000	85°C		29	52		40	72	

† Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

- 5. This range also applies to each input individually.
- 6. At $V_{DD} = 5$ V, $V_{O} = 0.25$ V to 2 V; at $V_{DD} = 10$ V, $V_{O} = 1$ V to 6 V.



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operating characteristics at specified free-air temperature

							TLC1	078I															
	PARAMETER	TEST CONDITIONS		TA	V _{DD} = 5 V			V _{DD} = 10 V			UNIT												
					MIN	TYP	MAX	MIN	TYP	MAX													
				25°C		32			47														
SR	Slew rate at unity gain		C _L = 20 pF, See Figure 1			-40°C		39			59		V/ms										
		VI(PP) - 1 V,		85°C		25			34														
٧n	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω	25°C		68		68			nV/√ Hz												
				25°C		85			110														
B ₁	Unity-gain bandwidth	$C_L = 20 \text{ pF},$	$C_L = 20 pF$,	= 20 pF, See Figure 2	See Figure 2	See Figure 2	See Figure 2	See Figure 2	See Figure 2	See Figure 2	See Figure 2	See Figure 2	See Figure 2	-40°C		130			155		kHz		
				85°C		55			80														
				25°C		34°			38°														
φm	Phase margin at unity gain	C _L = 20 pF, See Figure 2	$C_L = 20 \text{ pF}, \text{See Figure 2} -40^{\circ}\text{C}$	See Figure 2	See Figure 2	See Figure 2	F, See Figure 2	F, See Figure 2	, See Figure 2	See Figure 2	See Figure 2	; See Figure 2	, See Figure 2	See Figure 2	, See Figure 2	_ = 20 pF, See Figure 2		38°			40°		
	The state of the s			85°C		28°			32°														

operating characteristics at specified free-air temperature

							TLC1	079I			
	PARAMETER	TEST CO	NDITIONS	TA	٧ _I	DD = 5 \	<i>'</i>	۷۲	D = 10	V	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
				25°C		32			47		
SR	Slew rate at unity gain	$R_L = 1 M\Omega$,	C _L = 20 pF, See Figure 1	−40°C		39			59	MAX	V/ms
		VI(PP) = 1 V,	oce i igule i	85°C	25			34			
٧n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$	25°C		68			68		nV/√ Hz
				25°C		85			110		
В1	Unity-gain bandwidth	$C_L = 20 pF$,	See Figure 2	−40°C		130			155		kHz
				85°C		55			80		
				25°C		34°			38°		
φm	Phase margin at unity gain	C _L = 20 pF,	See Figure 2	−40°C		38°			42°		
				85°C		28°			32°		

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electrical characteristics at specified operating free-air temperature

						TLC1	078M			
	PARAMETER	TEST CONDITIONS	T _A †	V	_{DD} = 5 \	/	V	_{DD} = 10	٧	UNIT
		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	
\/. -	lanut offeet voltege	V _O = 1.4 V,	25°C		160	450		180	600	\/
VIO	Input offset voltage	$V_{IC} = 0$,	Full range			1250			1400	μV
ανιο	Temperature coefficient of input offset voltage	$R_S = 50 \Omega$, $R_L = 1 M\Omega$	25°C to 125°C		1.4			1.4		μV/°C
lia	Input offset current		25°C	0.1 60 0.1		60	pА			
IIO	(see Note 4)	$V_O = V_{DD}/2$,	125°C		1.4	15		1.8	15	nA
1	Input bias current	$V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	pА
IВ	(see Note 4)		125°C		9	35		10	35	nA
\/	Common-mode input		25°C	0 to 4	-0.3 to 4.2		0 to 9	-0.3 to 9.2		V
VICR Voltage range (see Note 5)		Full range	0 to 3.5			0 to 8.5			V	
			25°C	3.2	4.1		8.2	8.9		
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $R_{L} = 1 \text{ M}\Omega$	−55°C	3.2	4.1		8.2	8.8		V
		KL= 1 IVIS2	125°C	3.2	4.2		8.2	9		
			25°C		0	25		0	25	
v_{OL}	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 0$	−55°C		0	25		0	25	mV
		IOL = 0	125°C		0	25		0	25	
			25°C	250	525		500	850		
AVD	Large-signal differential voltage amplification	$R_L=1 M\Omega$, See Note 6	−55°C	250	950		500	1750		V/mV
	voltage amplification	Occ Noic o	125°C	35	200		75	380		
			25°C	70	95		75	97		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	−55°C	70	95		75	97		dB
			125°C	70	85		75	91		
	0 1 1		25°C	75	98		75	98		
ksvr	SVR Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$	V _O = 1.4 V	−55°C	70	98		70	98		dB
	(A • DD/A • IO/		125°C	70	98		70	98		
	•	$V_{O} = V_{DD}/2,$ $V_{IC} = V_{DD}/2,$	25°C		20	34		29	46	
I_{DD}	Supply current (two amplifiers)		−55°C		35	60		56	96	μΑ
	, ,	No load	125°C		14	24		18	30	

[†] Full range is –55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

- 5. This range also applies to each input individually.
- 6. At $V_{DD} = 5$ V, $V_{O} = 0.25$ V to 2 V; at $V_{DD} = 10$ V, $V_{O} = 1$ V to 6 V.



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electrical characteristics at specified free-air temperature

				TLC1079M							
	PARAMETER	TEST CONDITIONS	T _A †	V	_{DD} = 5 \	/	V	_{DD} = 10	٧	UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
\/	lanut effect valence		25°C		190	850		200	1150	/	
VIO	Input offset voltage	$V_O = 1.4 \text{ V}, V_{IC} = 0,$	Full range			1600			1900	μV	
ανιο	Temperature coefficient of input offset voltage	$R_S = 50 \Omega$, $R_I = 1 M\Omega$	25°C to 125°C		1.4			1.4		μV/°C	
1	Input offset current		25°C		0.1	60		0.1	60	pА	
ΙO	(see Note 4)	$V_O = V_{DD}/2$,	125°C		1.4	15		1.8	15	nA	
l	Input bias current	$V_{IC} = V_{DD}/2$	25°C		0.6	60		0.7	60	pА	
ΙΒ	(see Note 4)		125°C		9	35		10	35	nA	
V	Common mode input		25°C	0 to 4	-0.3 to 4.2		0 to 9	-0.3 to 9.2		V	
VICR	voltage range (see Note 5)		Full range	0 to 3.5			0 to 8.5			V	
			25°C	3.2	4.1		8.2	8.9			
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $R_{I} = 1 \text{ M}\Omega$	−55°C	3.2	4.1		8.2	8.9		٧	
			125°C	3.2	4.2		8.2	9			
			25°C		0	25		0	25		
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 0$	−55°C		0	25		0	25	mV	
		OL V	125°C		0	25		0	25		
	Laure d'avail d'étance d'al		25°C	250	525		500	850			
AVD	Large-signal differential voltage amplification	$R_L = 1 M\Omega$, See Note 6	−55°C	250	950		500	1750		V/mV	
	renage ampimeation		125°C	35	200		75	380			
	On any and a section of the section of		25°C	70	95		75	97			
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	−55°C	70	95		75	97		dB	
	ratio		125°C	70	85		75	91			
	0 1 1 1 1	577, 4077	25°C	75	98		75	98			
ksvr	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 5 \text{ V to } 10 \text{ V},$ $V_{O} = 1.4 \text{ V}$	−55°C	70	98		70	98		dB	
			125°C	70	98		70	98			
	Cupply ourront	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	25°C		40	68		57	7 92		
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	−55°C		69	120		111	192	2 μΑ	
	• 1 -7		125°C		27	48		35	60		

[†] Full range is -55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

- 5. This range also applies to each input individually.
 6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics at specified free-air temperature

							TLC1	078M			
	PARAMETER	TEST CO	NDITIONS	TA	V	DD = 5 \	/	٧ _C	D = 10	٧	UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
				25°C		32			47		
SR	Slew rate at unity gain	$R_L = 1 M\Omega,$ $V_{I(PP)} = 1 V,$		−55°C		41			63		-
		VI(PP) = 1 V,	Occ rigure r	125°C		20			27		
٧n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$	25°C		68			68		nV/√ Hz
				25°C		85			110		
В1	Unity-gain bandwidth	C _L = 20 pF,	See Figure 2	−55°C		140			165		kHz
				125°C		45			70		
				25°C		34°			38°		
φm	Phase margin at unity gain	$C_L = 20 pF$,	See Figure 2	−55°C		39°			43°		
				125°C		25°			29°		

operating characteristics at specified free-air temperature

							TLC1	079M				
	PARAMETER	TEST CO	NDITIONS	TA	V	DD = 5 \	1	۷۲	D = 10	٧	UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
				25°C		32			47			
SR	SR Slew rate at unity gain	$R_L = 1 M\Omega$, $V_{VDD} = 1 V$	C _L = 20 pF, See Figure 1	−55°C		41			63		V/ms	
		VI(PP) - 1 V,	Coo i iguio i	125°C		20		27				
٧n	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$	25°C		68			68		nV/√ Hz	
				25°C		85			110			
 D.	Unity-gain bandwidth	C 20 pE	See Figure 2	−55°C		140			165			
B ₁	Offity-gairt baridwidth	$C_L = 20 \text{ pF},$	See Figure 2	125°C		45			70		kHz	
				25°C		34°			38°		KIIZ	
	Phono morain at unity gain	C 20 pE	0 5 0	−55°C		39°			43°			
φm	Phase margin at unity gain	$C_L = 20 \text{ pF},$	See Figure 2	125°C		25°			29°			

PARAMETER MEASUREMENT INFORMATION

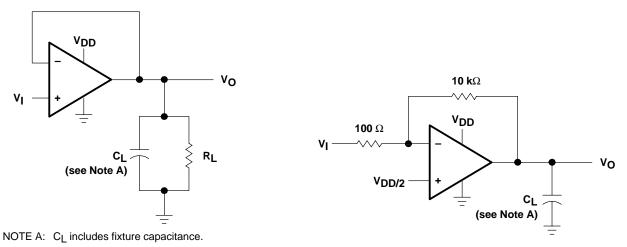


Figure 1. Slew-Rate Test Circuit

Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
ανιο	Temperature coefficient of input offset voltage	Distribution	3 – 6
I _{IB}	Input bias current	vs Free-air temperature	7
lιΟ	Input offset current	vs Free-air temperature	7
VIC	Common-mode input voltage	vs Supply voltage	8
Vон	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	9, 10 11 12
V _{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	13, 14 15 16 17, 18
AVD	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	19 20 21, 22
Vом	Maximum peak output voltage	vs Frequency	23
I _{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
٧n	Equivalent input noise voltage	vs Frequency	29
B ₁	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	30 31
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive load	32 33 34
	Phase shift	vs Frequency	21, 22



DISTRIBUTION OF TLC1078 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

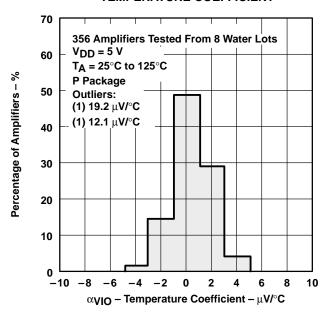


Figure 3

DISTRIBUTION OF TLC1079 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

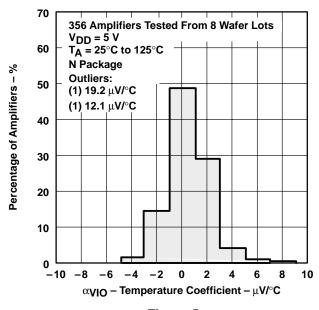


Figure 5

DISTRIBUTION OF TLC1078 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

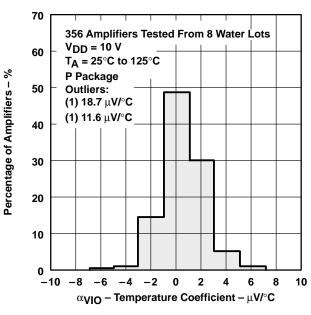


Figure 4

DISTRIBUTION OF TLC1079 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

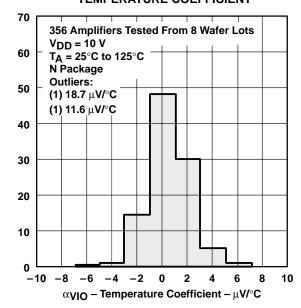
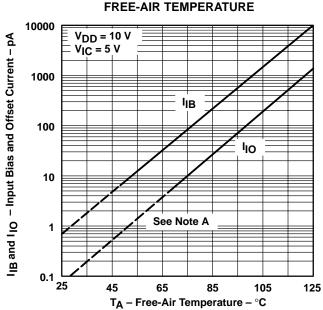


Figure 6

Percentage of Amplifiers – %

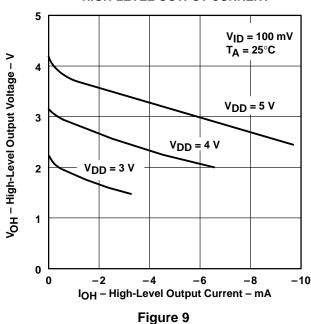
INPUT BIAS AND OFFSET CURRENT† vs



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 7

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT



COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT

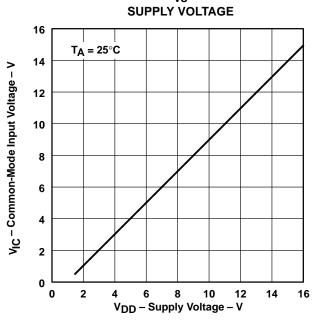
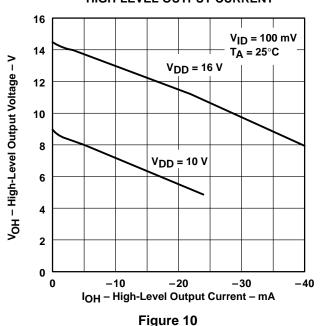


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. † The V_{DD} = 3 V curve does not apply to the TLC107xM.



HIGH-LEVEL OUTPUT VOLTAGE SUPPLY VOLTAGE 16 V_{ID} = 100 mV $R_L = 1 M\Omega$ 14 V_{OH} - High-Level Output Voltage - V **T_A = 25°C** 12 10 8 6 4 2 0 10 12 14 16 V_{DD} - Supply Voltage - V

HIGH-LEVEL OUTPUT VOLTAGE[†]
vs
FREE-AIR TEMPERATURE

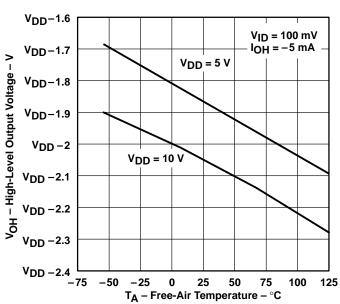
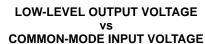


Figure 11 Figure 12



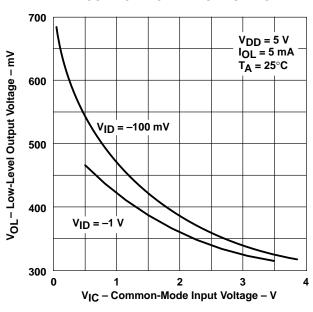


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

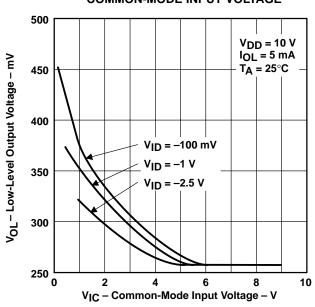


Figure 14

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



LOW-LEVEL OUTPUT VOLTAGE vs **DIFFERENTIAL INPUT VOLTAGE** 800 $V_{IC} = |V_{ID}/2|$ 700 $I_{OL} = 5 \text{ mA}$ V_{OL} - Low-Level Output Voltage - mV $T_A = 25^{\circ}C$ 600 500 $V_{DD} = 5 V$ 400 300 $V_{DD} = 10 V$ 200 100 0 0 -2 -4 -6 -8 -10 V_{ID} - Differential Input Voltage - V

LOW-LEVEL OUTPUT VOLTAGE[†]
vs
FREE-AIR TEMPERATURE

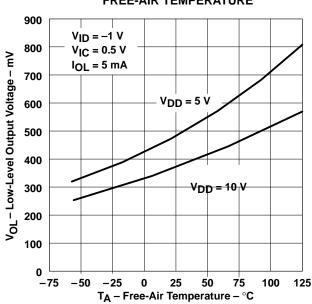
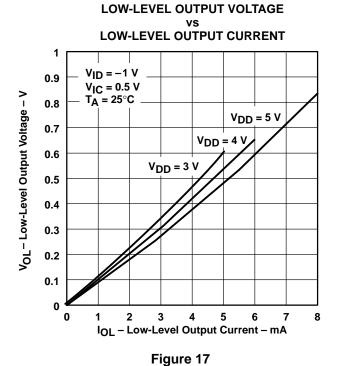


Figure 15

Figure 16



LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

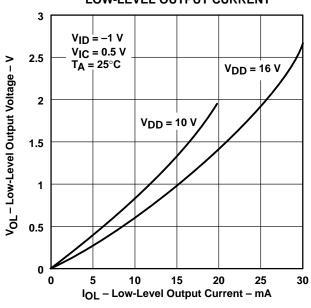
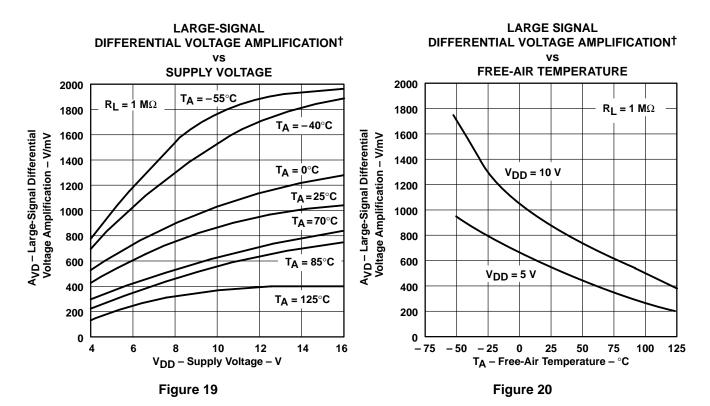


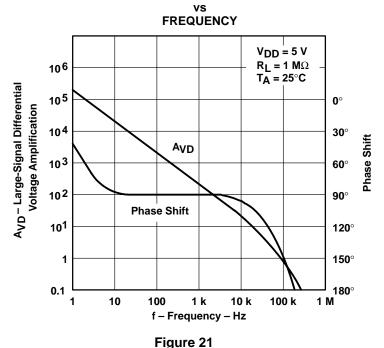
Figure 18

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



LARGE-SIGNAL DIFFERENTIAL VOLTAGE **AMPLIFICATION AND PHASE SHIFT**

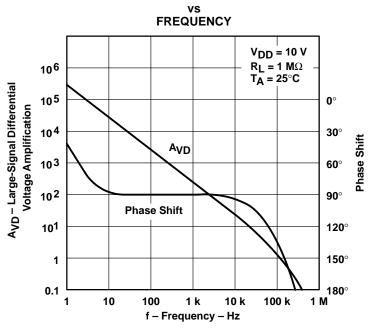
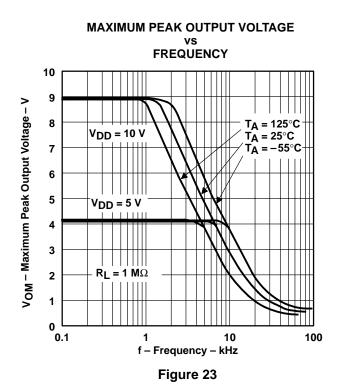
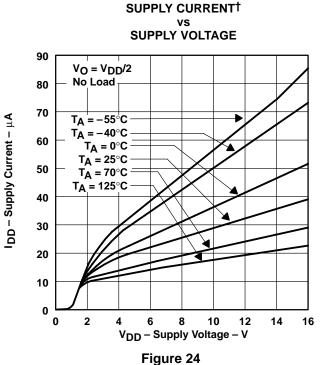


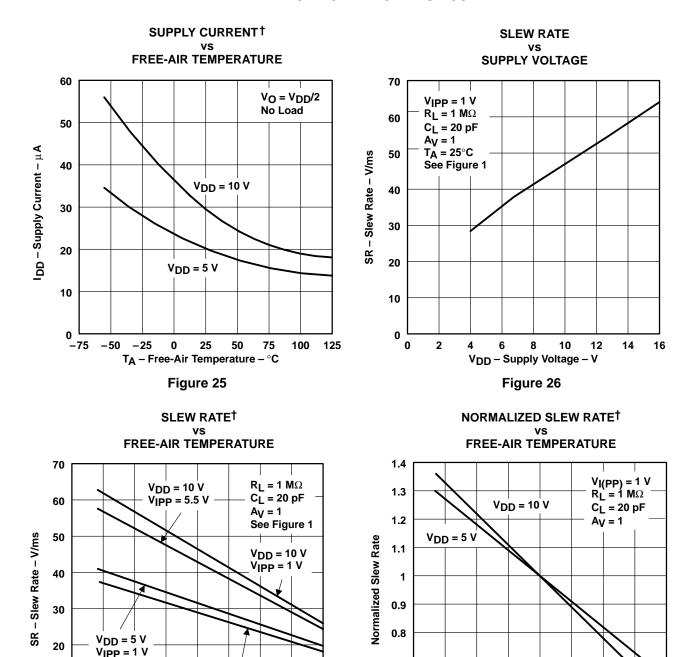
Figure 22





[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

 $V_{DD} = 5 V$

50

 $V_{IPP} = 2.5 V$

75

100

125

10

0

-75

-50

-25

0

25

 T_A – Free-Air Temperature – $^{\circ}$ C

Figure 27



0.7

0.6

0.5

-75 -50

-25

0

25

 T_A – Free-Air Temperature – $^{\circ}$ C

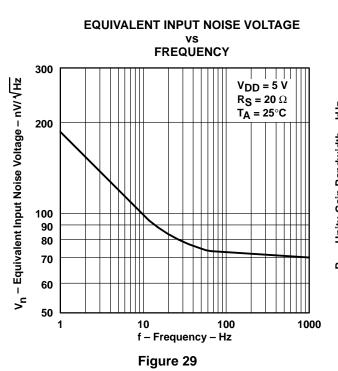
Figure 28

50

75

100

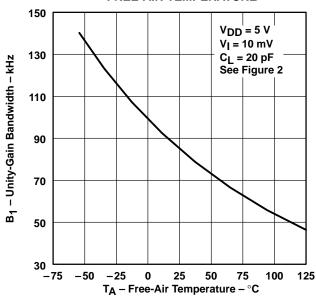
125



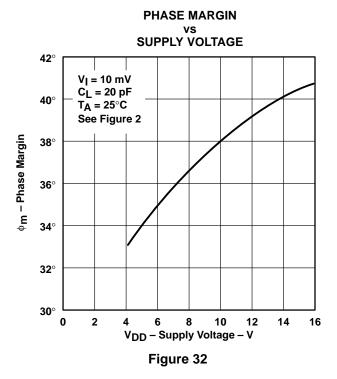
SUPPLY VOLTAGE 140 $V_I = 10 \text{ mV}$ 130 C_L = 20 pF T_A = 25°C B₁ - Unity-Gain Bandwidth - kHz See Figure 2 120 110 100 90 80 70 60 50 0 2 8 10 12 14 16 V_{DD} – Supply Voltage – V Figure 30

UNITY-GAIN BANDWIDTH







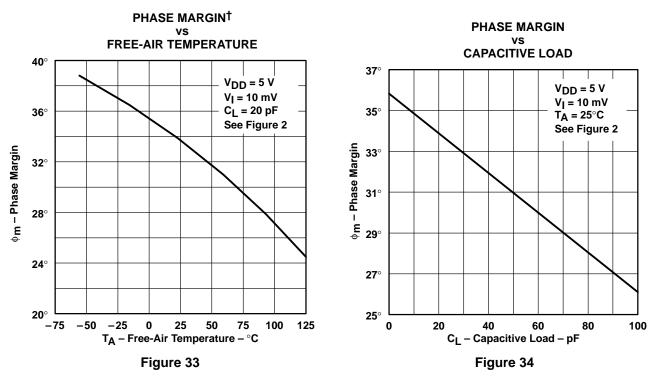


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





11-Mar-2015

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TLC1078CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C	Samples
TLC1078CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C	Samples
TLC1078CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C	Samples
TLC1078CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C	Samples
TLC1078CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC1078CP	Samples
TLC1078CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC1078CP	Samples
TLC1078ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1078I	Samples
TLC1078IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1078I	Samples
TLC1078IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1078I	Samples
TLC1078IDRG4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		Samples
TLC1078IP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC1078IP	Samples
TLC1078IPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLC1078IP	Samples
TLC1078MD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-55 to 125		
TLC1078MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1078M	Samples
TLC1079CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1079C	Samples
TLC1079CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1079C	Samples
TLC1079CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1079C	Samples



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PACKAGE OPTION ADDENDUM

11-Mar-2015

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLC1079CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1079CN	Samples
TLC1079CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1079CN	Samples
TLC1079ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1079I	Samples
TLC1079IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1079I	Samples
TLC1079IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC1079I	Samples
TLC1079IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1079IN	Samples
TLC1079INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC1079IN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

11-Mar-2015

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC1078CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1078IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1078IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1079CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC1079IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

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*All dimensions are nominal

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Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC1078CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC1078IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC1078IDR	SOIC	D	8	2500	367.0	367.0	38.0
TLC1079CDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC1079IDR	SOIC	D	14	2500	367.0	367.0	38.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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