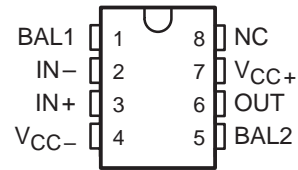


LF411 JFET-INPUT OPERATIONAL AMPLIFIER

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- Low Input Bias Current, 50 pA Typ
- Low Input Noise Current, 0.01 pA/ $\sqrt{\text{Hz}}$ Typ
- Low Supply Current, 2 mA Typ
- High Input impedance, $10^{12} \Omega$ Typ
- Low Total Harmonic Distortion
- Low 1/f Noise Corner, 50 Hz Typ
- Package Options Include Plastic Small-Outline (D) and Standard (P) DIPs

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

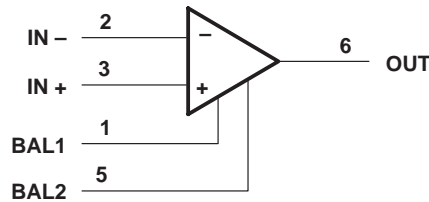
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current, yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C. The LF411I is characterized for operation from –40°C to 85°C.

symbol



AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	2 mV	LF411CD	LF411CP
–40°C to 85°C	2 mV	LF411ID	LF411IP

The D packages are available taped and reeled. Add the suffix R to the device type (i.e., LF411CDR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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LF411

JFET-INPUT OPERATIONAL AMPLIFIER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	-18 V
Differential input voltage, V_{ID}	± 30 V
Input voltage, V_I (see Note 1)	± 15 V
Duration of output short circuit	Unlimited
Continuous total power dissipation	500 mW
Package thermal impedance, θ_{JA} (see Note 2): D package	197°C/W
P package	104°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

	C SUFFIX		I SUFFIX		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC+}	3.5	18	3.5	18	V
Supply voltage, V_{CC-}	-3.5	-18	-3.5	-18	V
Operating free-air temperature, T_A	0	70	-40	-85	°C

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V (unless otherwise specified)

PARAMETER	TEST CONDITIONS	T_A		MIN	TYP	MAX	UNIT
		LF411C	LF411I				
V_{IO} Input offset voltage	$V_{IC} = 0, R_S = 10 \text{ k}\Omega$	25°C	25°C	0.8	2		mV
α_{VIO} Average temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 10 \text{ k}\Omega$			10	20†		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current‡	$V_{IC} = 0$	25°C	25°C	25	100		pA
		70°C	85°C		2		nA
I_{IB} Input bias current‡	$V_{IC} = 0$	25°C	25°C	50	200		pA
		70°C	85°C		4		nA
V_{ICR} Common-mode input voltage range				± 11	-11.5 to 14.5		V
V_{OM} Maximum peak output-voltage swing	$R_L = 10 \text{ k}\Omega$			± 12	± 13.5		V
A_{VD} Large-signal differential voltage	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	25°C	25°C	25	200		V/mV
		0°C to 70°C	-40°C to 85°C	15	200		
r_i Input resistance	$T_J = 25^\circ\text{C}$				10 ¹²		Ω
CMR_R Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$			70	100		dB
K_{SVR} Supply-voltage rejection ratio	See Note 3			70	100		dB
I_{CC} Supply current				2	3.4		mA

† At least 90% of the devices meet this limit for α_{VIO} .

‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 3: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.



LF411 JFET-INPUT OPERATIONAL AMPLIFIER

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operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/ μs
B ₁	Unity-gain bandwidth		2.7	3		MHz
V _n	Equivalent input noise voltage	f = 1 kHz, R _S = 20 Ω		18		nV/ $\sqrt{\text{Hz}}$
I _n	Equivalent input noise current	f = 1 kHz		0.01		pA/ $\sqrt{\text{Hz}}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF411CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C	Samples
LF411CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C	Samples
LF411CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C	Samples
LF411CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LF411C	Samples
LF411CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LF411CP	Samples
LF411CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LF411CP	Samples
LF411ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
LF411IDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
LF411IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF411CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF411CDR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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