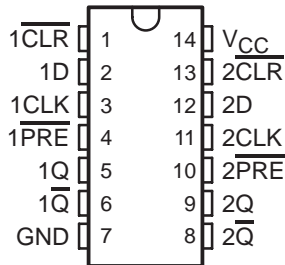


SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

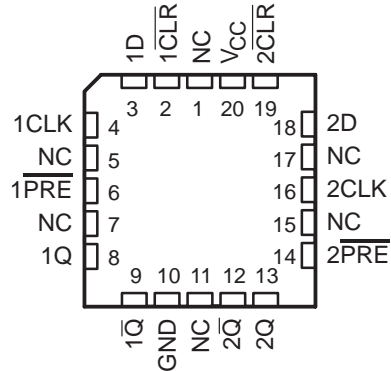
SCAS520H – AUGUST 1995 – REVISED OCTOBER 2003

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 10.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible

SN54ACT74 . . . J OR W PACKAGE
SN74ACT74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'ACT74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube | SN74ACT74N | SN74ACT74N |
| | SOIC – D | Tube | SN74ACT74D | ACT74 |
| | | Tape and reel | SN74ACT74DR | |
| | SOP – NS | Tape and reel | SN74ACT74NSR | ACT74 |
| | SSOP – DB | Tape and reel | SN74ACT74DBR | AD74 |
| TSSOP – PW | Tube | SN74ACT74PW | AD74 | |
| | Tape and reel | SN74ACT74PWR | | |
| -55°C to 125°C | CDIP – J | Tube | SNJ54ACT74J | SNJ54ACT74J |
| | CFP – W | Tube | SNJ54ACT74W | SNJ54ACT74W |
| | LCCC – FK | Tube | SNJ54ACT74FK | SNJ54ACT74FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

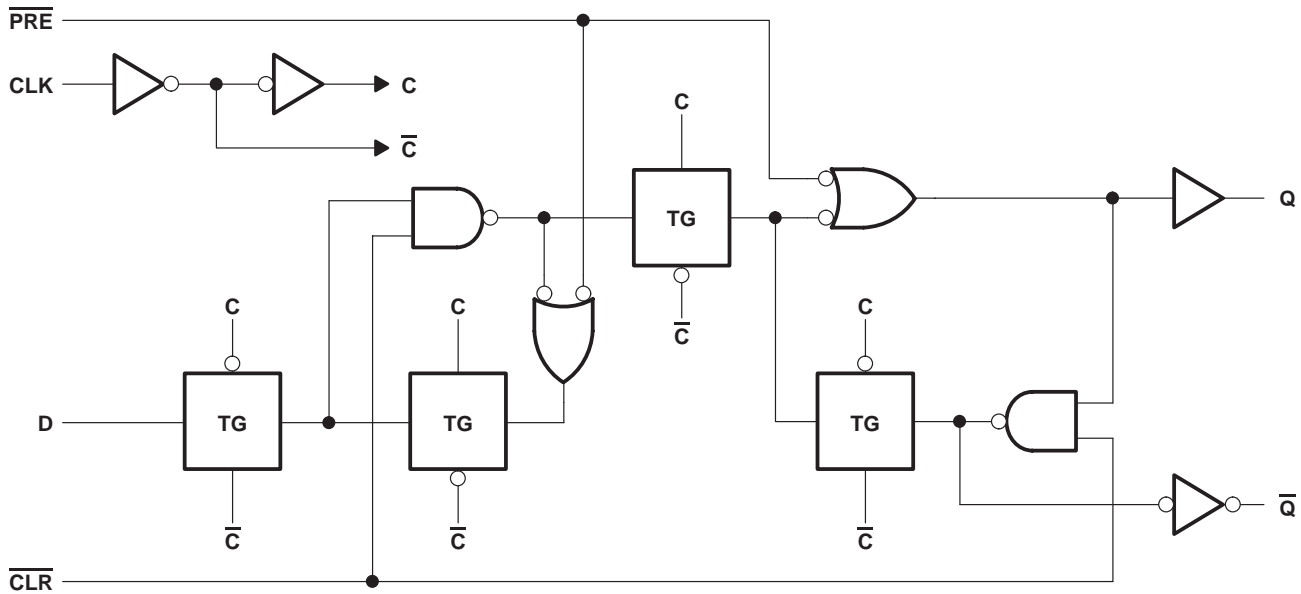
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FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | OUTPUTS | |
|-------------------------|-------------------------|-----|---|----------------|-------------------------|
| $\overline{\text{PRE}}$ | $\overline{\text{CLR}}$ | CLK | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H [†] | H [†] |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | Q ₀ | $\overline{\text{Q}}_0$ |

[†] This configuration is nonstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)



SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±50 mA |
| Continuous current through V_{CC} or GND | ±200 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| DB package | 96°C/W |
| N package | 80°C/W |
| NS package | 76°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | SN54ACT74 | | SN74ACT74 | | UNIT |
|--|-----------|----------|-----------|----------|------|
| | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| V_O Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | –24 | | –24 | mA |
| I_{OL} Low-level output current | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 8 | | 8 | ns/V |
| T_A Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54ACT74 | | SN74ACT74 | | UNIT |
|---------------------------|---|-----------------|-----------------------|------|------|-----------|------|-----------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | 4.49 | | 4.4 | | 4.4 | V | |
| | | 5.5 V | 5.4 | 5.49 | | 5.4 | | 5.4 | | |
| | I _{OH} = -24 mA | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| | I _{OH} = -50 mA† | 5.5 V | | | | 3.86 | | | | |
| I _{OH} = -75 mA† | 5.5 V | | | | | | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | 0.001 | | 0.1 | | 0.1 | | V | |
| | | 5.5 V | 0.001 | | 0.1 | | 0.1 | | | |
| | I _{OL} = 24 mA | 4.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| | | 5.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| | I _{OL} = 50 mA† | 5.5 V | | | | | 1.65 | | | |
| I _{OL} = 75 mA† | 5.5 V | | | | | | 1.65 | | | |
| I _I | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | ±1 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 40 | 20 | μA | |
| ΔI _{CC} ‡ | One input at 3.4 V, Other inputs at GND or V _{CC} | 5.5 V | | | 0.6 | | 1.6 | 1.5 | mA | |
| C _i | V _I = V _{CC} or GND | 5 V | | | 3 | | | | pF | |

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | T _A = 25°C | | SN54ACT74 | | SN74ACT74 | | UNIT |
|--------------------|------------------------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 145 | | 85 | | 125 | | MHz |
| t _w | Pulse duration | PRE or CLR low | 5 | 7 | 6 | | | ns |
| | | CLK | 5 | 7 | 6 | | | |
| t _{su} | Setup time, data before CLK↑ | Data | 3 | 4 | 3.5 | | | ns |
| | | PRE or CLR inactive | 0 | 0.5 | 0 | | | |
| t _h | Hold time, data after CLK↑ | 1 | 1 | 1 | | | ns | |

switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ACT74 | | | | UNIT | |
|------------------|--------------|-------------|-----------------------|-----|-----|-----|------|-----|
| | | | T _A = 25°C | | | MIN | | MAX |
| | | | MIN | TYP | MAX | | | |
| f _{max} | | | 145 | 210 | | 85 | MHz | |
| t _{PLH} | PRE or CLR | Q or Q̄ | 1 | 5.5 | 9.5 | 1 | 11.5 | ns |
| t _{PHL} | | | 1 | 6 | 10 | 1 | 12.5 | |
| t _{PLH} | CLK | Q or Q̄ | 1 | 7.5 | 11 | 1 | 14 | ns |
| t _{PHL} | | | 1 | 6 | 10 | 1 | 12 | |



SN54ACT74, SN74ACT74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ACT74 | | | | | UNIT |
|------------------|--|----------------------------|-----------------------|-----|-----|-----|------|------|
| | | | T _A = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| f _{max} | | | 145 | 210 | | 125 | MHz | |
| t _{PLH} | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ | 3 | 5.5 | 9.5 | 2.5 | 10.5 | ns |
| t _{PHL} | | | 3 | 6 | 10 | 3 | 11.5 | |
| t _{PLH} | CLK | Q or $\overline{\text{Q}}$ | 4 | 7.5 | 11 | 4 | 13 | ns |
| t _{PHL} | | | 3.5 | 6 | 10 | 3 | 11.5 | |

operating characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------------------------|-----|------|
| C _{pd} Power dissipation capacitance | C _L = 50 pF, f = 1 MHz | 45 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| 5962-8752501M2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 8752501M2A SNJ54ACT 74FK | Samples |
| 5962-8752501MCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8752501MC A SNJ54ACT74J | Samples |
| 5962-8752501MDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8752501MD A SNJ54ACT74W | Samples |
| SN74ACT74D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT74 | Samples |
| SN74ACT74DBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74ACT74DBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD74 | Samples |
| SN74ACT74DE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT74 | Samples |
| SN74ACT74DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT74 | Samples |
| SN74ACT74DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT74 | Samples |
| SN74ACT74DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT74 | Samples |
| SN74ACT74DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT74 | Samples |
| SN74ACT74N | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ACT74N | Samples |
| SN74ACT74NE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ACT74N | Samples |
| SN74ACT74NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT74 | Samples |
| SN74ACT74PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD74 | Samples |
| SN74ACT74PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 85 | | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| SN74ACT74PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD74 | Samples |
| SN74ACT74PWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD74 | Samples |
| SN74ACT74PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD74 | Samples |
| SNJ54ACT74FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-8752501M2A SNJ54ACT 74FK | Samples |
| SNJ54ACT74J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8752501MC A SNJ54ACT74J | Samples |
| SNJ54ACT74W | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8752501MD A SNJ54ACT74W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ACT74, SN74ACT74 :

- Catalog: [SN74ACT74](#)

- Enhanced Product: [SN74ACT74-EP](#), [SN74ACT74-EP](#)

- Military: [SN54ACT74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ACT74DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ACT74DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ACT74NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ACT74PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ACT74DBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ACT74DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74ACT74NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ACT74PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - Δ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - Δ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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