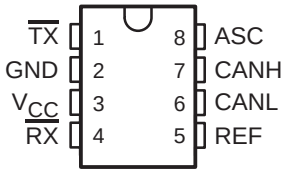
- **SN75LBC031 Meets Standard ISO/DIS 11898 (up to 500 k Baud)**
- **Driver Output Capability at 50 mA**
- **Wide Positive and Negative Input/output Bus Voltage Range**
- **Bus Outputs Short-Circuit-Protected to Battery Voltage and Ground**
- **Thermal Shutdown**
- **Available in Q-Temp Automotive**
  - **HighRel Automotive Applications**
  - **Configuration Control/Print Support**
  - **Qualification to Automotive Standards**

D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL	DESCRIPTION
$\overline{TX}$	Transmitter input
GND	Ground
V_{CC}	Supply voltage
$\overline{RX}$	Receiver output
REF	Reference output
CANL	Low side bus output driver
CANH	High side bus output driver
ASC	Adjustable slope control

FUNCTION TABLE

$\overline{TX}$	CANH	CANL	BUS STATE	$\overline{RX}$
L	H	L	Dominant	L
High or floating	Floating	Floating	Recessive	H

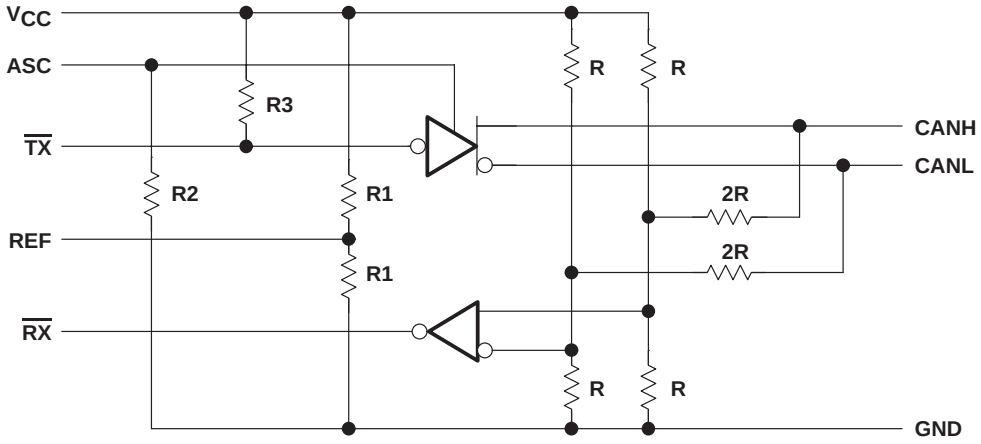
L = low, H = high

description

The SN75LBC031 is a CAN transceiver used as an interface between a CAN controller and the physical bus for high speed applications of up to 500 kBaud. The device provides transmit capability to the differential bus and differential receive capability to the controller. The transmitter outputs (CANH and CANL), feature internal transition regulation to provide controlled symmetry resulting in low EMI emissions. Both transmitter outputs are fully protected against battery short circuits and electrical transients that can occur on the bus lines. In the event of excessive device power dissipation the output drivers are disabled by the thermal shutdown circuitry at a junction temperature of approximately 160°C. The inclusion of an internal pullup resistor on the transmitter input ensures a defined output during power up and protocol controller reset. For normal operation at 500 kBaud the ASC terminal is open or tied to GND. For slower speed operation at 125 kBaud the bus output transition times can be increased to reduce EMI by connecting the ASC terminal to V_{CC}. The receiver includes an integrated filter that suppresses the signal into pulses less than 30 ns wide.

The SN75LBC031 is characterized for operation from –40°C to 85°C. The SN65LBC031 is characterized for operation from –40°C to 125°C. The SN65LBC031Q is characterized for operation over the automotive temperature range of –40°C to 125°C.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Bus terminal voltage . . . . . –5 V to 20 V
Input current at $\overline{TX}$ and ASC terminal, I_I . . . . . ±10 mA
Input voltage at $\overline{TX}$ and ASC terminal, V_I . . . . . $2 \times V_{CC}$
Operating free-air temperature range, T_A: SN65LBC031, SN65LBC031Q . . . . . –40°C to125°C
SN75LBC031 . . . . . –40°C to 85°C
Operating juncation range, T_J . . . . . –40°C to 150°C
Continuous total power dissipation at (or below) 25°C free-air temperature . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 sec T_C, D package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential bus voltage, are measured with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_C = 25°C$	$T_C = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	145 mW

DISSIPATION DERATING CURVE vs FREE-AIR TEMPERATURE

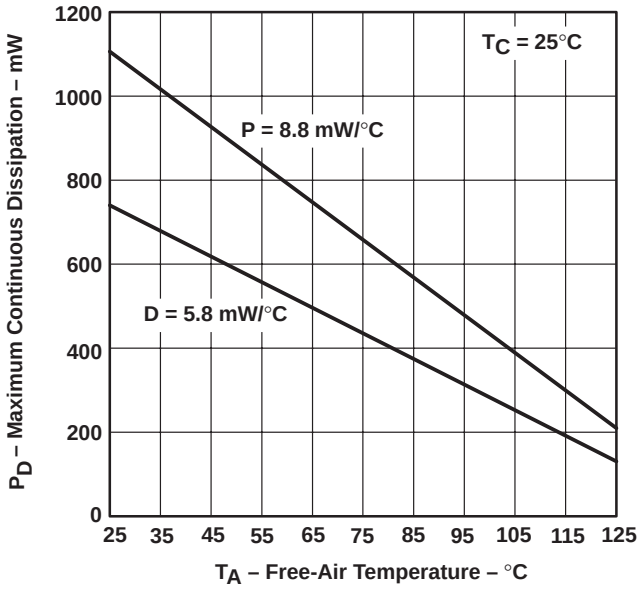


Figure 1

recommended operating conditions

		MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}		4.5	5	5.5	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC} (see Note 3)		–2		7	V
High-level input voltage, V_{IH}	$\overline{TX}$	2		V_{CC}	V
Low-level input voltage, V_{IL}	$\overline{TX}$	0		0.8	V
High-level output current, I_{OH}	Transmitter			–50	mA
	Receiver			–400	μA
Low-level output current, I_{OL}	Transmitter			50	mA
	Receiver			1	
Operating free-air temperature, T_A	SN75LBC031	–40		85	°C
	SN65LBC031, SN65LBC031Q	–40		125	

NOTES: 2. All voltage values, except differential bus voltage, are measured with respect to the ground terminal.
3. For bus voltages from –5 V to –2 V and 7 V to 20 V the receiver output is stable.

SYMBOL DEFINITION

DATA SHEET PARAMETER	DEFINITION
$V_{O(CANHR)}$	CANH bus output voltage (recessive state)
$V_{O(CANLR)}$	CANL bus output voltage (recessive state)
$V_{O(CANHD)}$	CANH bus output voltage (dominant state)
$V_{O(CANLD)}$	CANL bus output voltage (dominant state)
$V_{O(DIFFR)}$	Bus differential output voltage (recessive state)
$V_{O(DIFFD)}$	Bus differential output voltage (dominant state)
$V_{I(ASC)}$	Adjustable slope control input voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(REF)}$	Reference source output voltage	I_{REF} = ±20 μA	0.45 V_{CC}		0.55 V_{CC}	V
$R_{O(REF)}$	Reference source output resistance		5		10	kΩ
$I_{CC(REC)}$	Logic supply current, recessive state	See Figure 2, S1 closed		12	20	mA
$I_{CC(DOM)}$	Logic supply current, dominant state			55	80	

transmitter electrical characteristics over recommended ranges of supply and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(CANHR)}$ $V_{O(CANLR)}$	Output voltage (recessive state)	See Figure 2, S1 open	2	$0.5V_{CC}$	3	V
$V_{O(DIFFR)}$	Differential output voltage (recessive state)	See Figure 2, S1 open	–500	0	50	mV
$V_{O(CANHD)}$	Output voltage (dominant state)	See Figure 2, S1 closed	2.75	3.5	4.5	V
$V_{O(CANLD)}$	Output voltage (dominant state)	See Figure 2, S1 closed	0.5	1.5	2.25	V
$V_{O(DIFFD)}$	Differential output voltage (dominant state)	See Figure 2, S1 closed	1.5	2	3	V
$I_{IH(TX)}$	High-level input current (TX)	V_{IH} = 2.4 V		–100	–185	µA
		$V_{IH} = V_{CC}$			±2	µA
$I_{IH(ASC)}$	High-level input current (ASC)	V_{IH} = 2.4 V		100	165	µA
		$V_{IH} = V_{CC}$		200	340	µA
$I_{IL(TX)}$	Low-level input current ($\overline{TX}$)	V_{IL} = 0.4 V		–180	–400	µA
$I_{IL(ASC)}$	Low-level input current (ASC)	V_{IL} = 0.4 V		15	25	µA
$C_{I(TX)}$	$\overline{TX}$ input capacitance			8		pF
$I_{O(ssH)}$	CANH short circuit output current	$V_{O(CANH)}$ = –2 V to 20 V		–95	–200	mA
$I_{O(ssL)}$	CANL short circuit output current	$V_{O(CANL)}$ = 20 V to –2 V		140	250	mA

NOTE 2: All voltage values, except differential bus voltage, are measured with respect to the ground terminal.

transceiver dynamic characteristics over recommended operating free-air temperature range and V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(loop)}$	Loop time	See Figures 2 and 3, S1 closed, $V_{I(ASC)}$ = 0 V or open circuit, S2 open			280	ns
		See Figures 2 and 3, S1 closed, $V_{I(ASC)} = V_{CC}$, S2 closed			400	ns
$SR_{(RD)}$	Differential-output slew rate (recessive to dominant)	See Figures 2 and 4, S1 closed, $V_{I(ASC)}$ = 0 or open circuit, S2 open		35		V/µs
		See Figures 2 and 4, S1 closed, $V_{I(ASC)} = V_{CC}$, S2 closed		10		V/µs
$SR_{(DR)}$	Differential-output slew rate (dominant to recessive)	See Figures 2 and 4, S1 closed, $V_{I(ASC)}$ = 0 or open circuit, S2 open		10		V/µs
		See Figures 2 and 4, S1 closed, $V_{I(ASC)} = V_{CC}$, S2 closed		10		V/µs
$t_{d(RD)}$	Differential-output delay time	See Figure 2, S1 closed		55		ns
$t_{d(DR)}$	Differential-output delay time	See Figure 2, S1 closed		160		ns
$t_{pd(RECRD)}$	Receiver propagation delay time	See Figures 2 and 5		90		ns
$t_{pd(RECDR)}$	Receiver propagation delay time	See Figures 2 and 5		55		ns

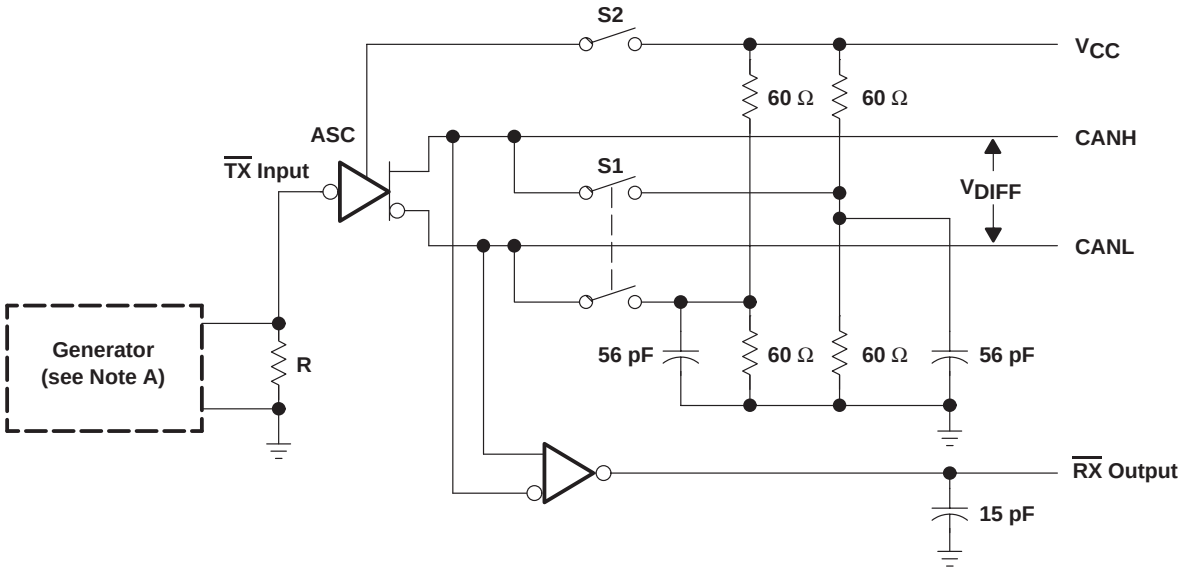
NOTE 4: Receiver input pulse width should be >50 ns. Input pulses of <30 ns are suppressed.

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(REC)}$	Differential input threshold voltage for recessive state	V_{IC} = –2 V to 7 V			500	mV
$V_{IT(DOM)}$	Differential input threshold voltage for dominant state		900			
V_{hys}	Recessive-dominant input hysteresis		100	180		mV
$V_{OH(RX)}$	High-level output voltage	$V_{O(DIFF)}$ = 500 mV, I_{OH} = –400 μA	V_{CC}–0.5 V		V_{CC}	V
$V_{OL(RX)}$	Low-level output voltage	$V_{O(DIFF)}$ = 900 mV, I_{OL} = 1 mA	0		0.5	V
$r_{I(REC)}$	CANH and CANL input resistance in recessive state	dc, no load	5		50	kΩ
$r_{I(DIFF)}$	Differential CANH and CANL input resistance in recessive state	dc, no load	10		100	kΩ
C_i	CANH and CANL input capacitance			20		pF
$C_{i(DHL)}$	Differential CANH and CANL input capacitance			10		pF

NOTE 2: All voltage values, except differential bus voltage, are measured with respect to the ground terminal.

PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied to $\overline{TX}$ by a generator having a t_r and t_f = 5 ns.

Figure 2. Test Circuit

PARAMETER MEASUREMENT INFORMATION

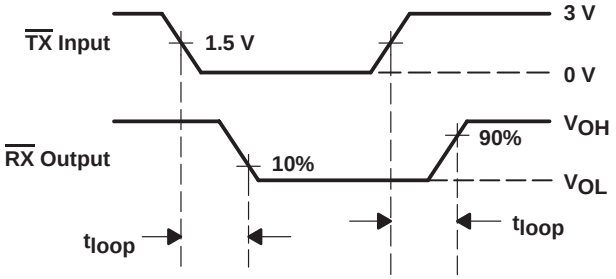


Figure 3. Loop Time

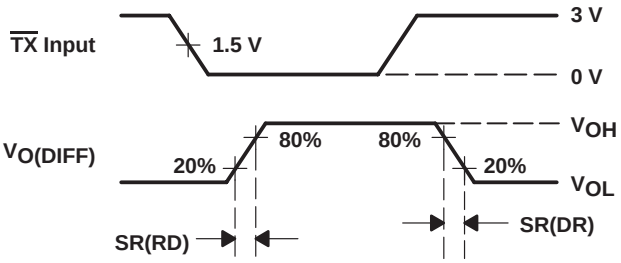
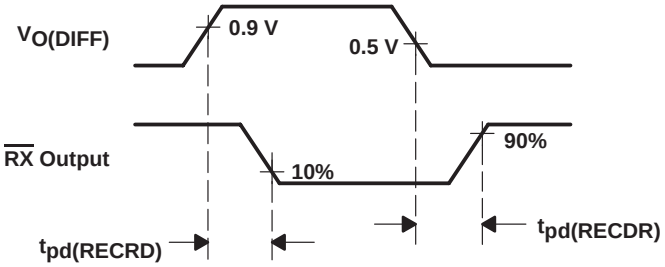


Figure 4. Slew Rate

NOTE A: The input pulse is supplied to $\overline{TX}$ by a generator having a t_r and t_f = 5 ns.



NOTE A: The input pulse is supplied as V_{DIFF} using CANH and CANL respectively by a generator having a t_r and t_f = 5 ns.

Figure 5. Receiver Delay Times

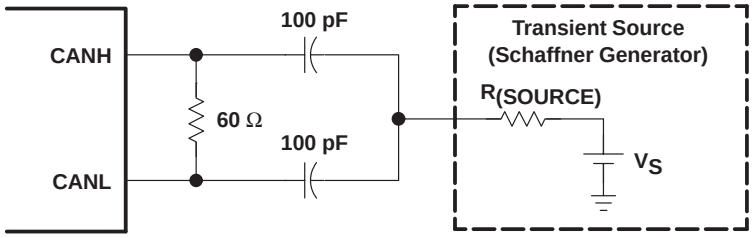


Figure 6. Transient Stress Capability Test Circuit

PARAMETER MEASUREMENT INFORMATION

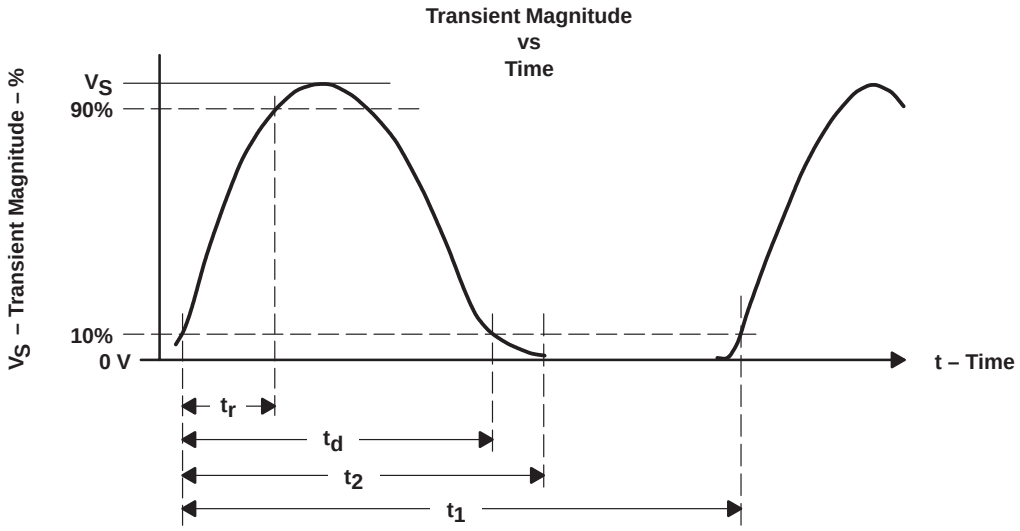


Figure 7. Transient Stress Capability Waveform

Table 1. Test Circuit Results According to DIN 40839

TEST PULSE	TRANSIENT MAGNITUDE V_S	SOURCE IMPEDANCE R_{SOURCE}	PULSE WIDTH t_d (see Note 5)	PULSE RISE TIME, t_r (see Note 6)	PULSE TIME, t_2 (see Figure 7)	REPETITION PERIOD, t_1 (see Figure 7)	NUMBER OF PULSES
1	–100 V	10 Ω	2 ms	1 µs	200 ms	5 s	5000
2	100 V	10 Ω	50 µs	1 µs	200 ms	5 s	5000
3a	–150 V	50 Ω	0.1 µs	5 ns	100 µs	100 µs	See Note 7
3b	100 V	50 Ω	0.1 µs	5 ns	100 µs	100 µs	See Note 7
5	60 V	1 Ω	400 ms	5 ms	—	—	1

NOTES: 5. Measured from 10% on rising edge to 10% on falling edge
6. Measured from 10% to 90% of pulse
7. Pulse package for a period of 3600 s, 10 ms pulse time, 90 ms stop time

APPLICATION INFORMATION

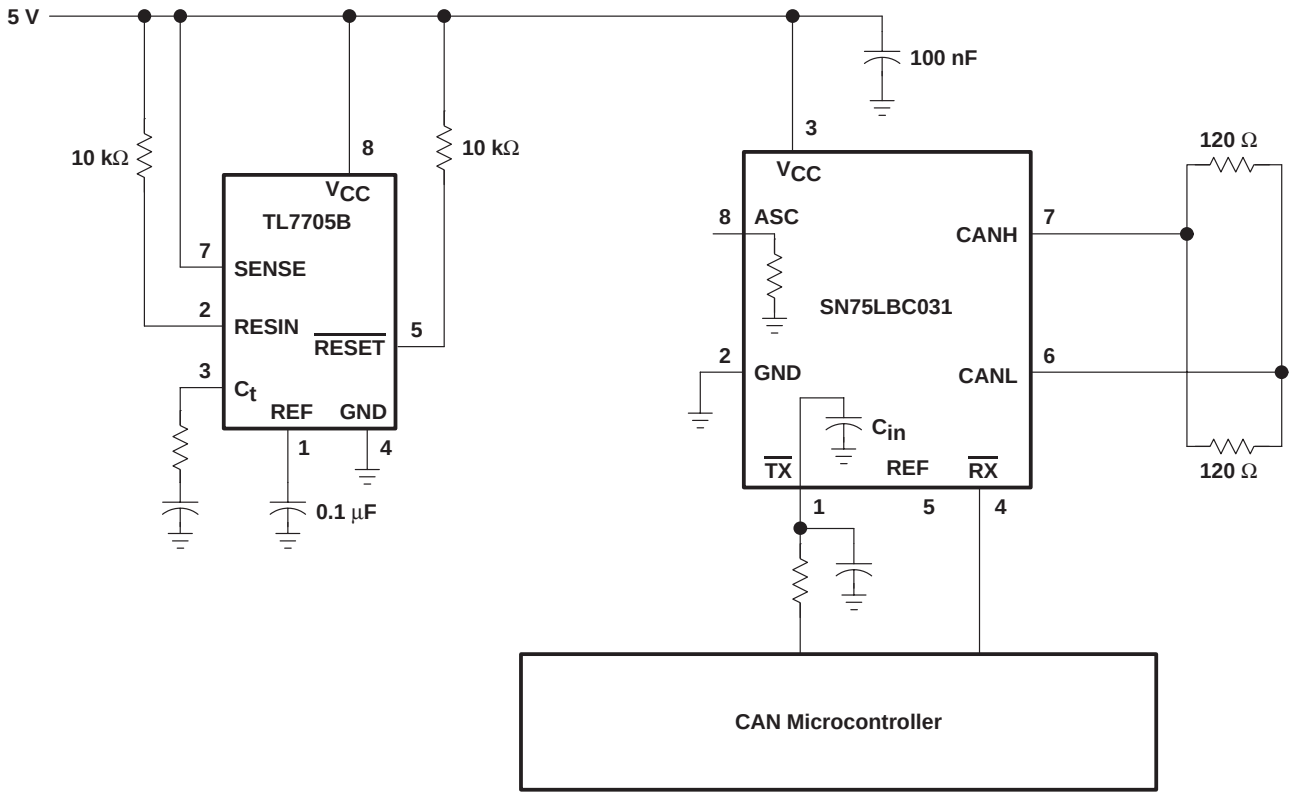
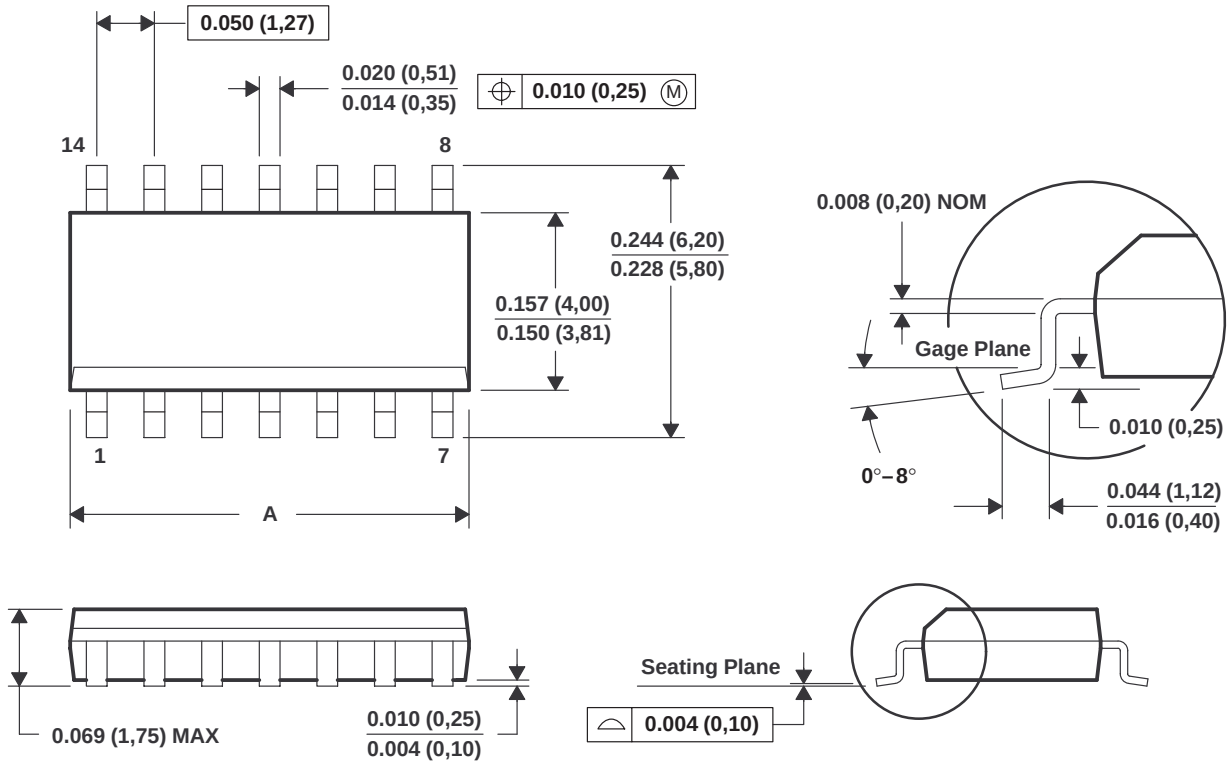


Figure 8. Typical SN75LBC031 Application

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC031D	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM	-40 to 85	6LB031	Samples
SN65LBC031DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB031	Samples
SN65LBC031DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		6LB031	Samples
SN65LBC031P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
SN65LBC031QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	6LB031Q	Samples
SN65LBC031QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	6LB031Q	Samples
SN65LBC031QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB031Q	Samples
SN65LBC031QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB031Q	Samples
SN75LBC031D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB031	Samples
SN75LBC031DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB031	Samples
SN75LBC031P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

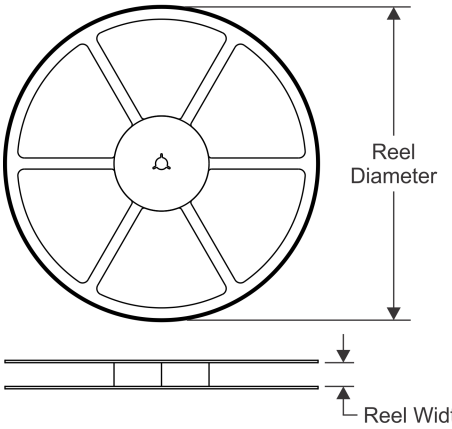
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

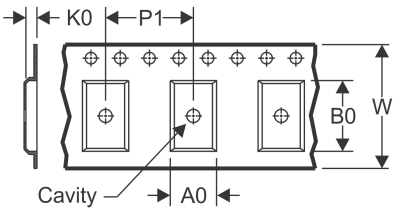
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

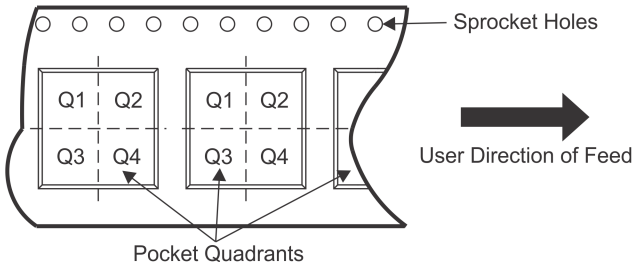


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

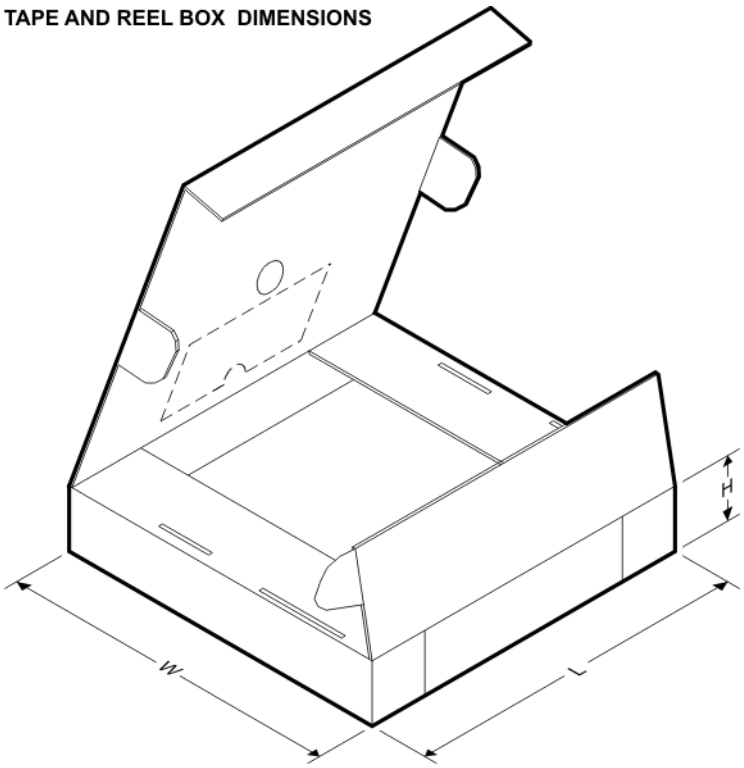
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC031QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC031QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC031DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

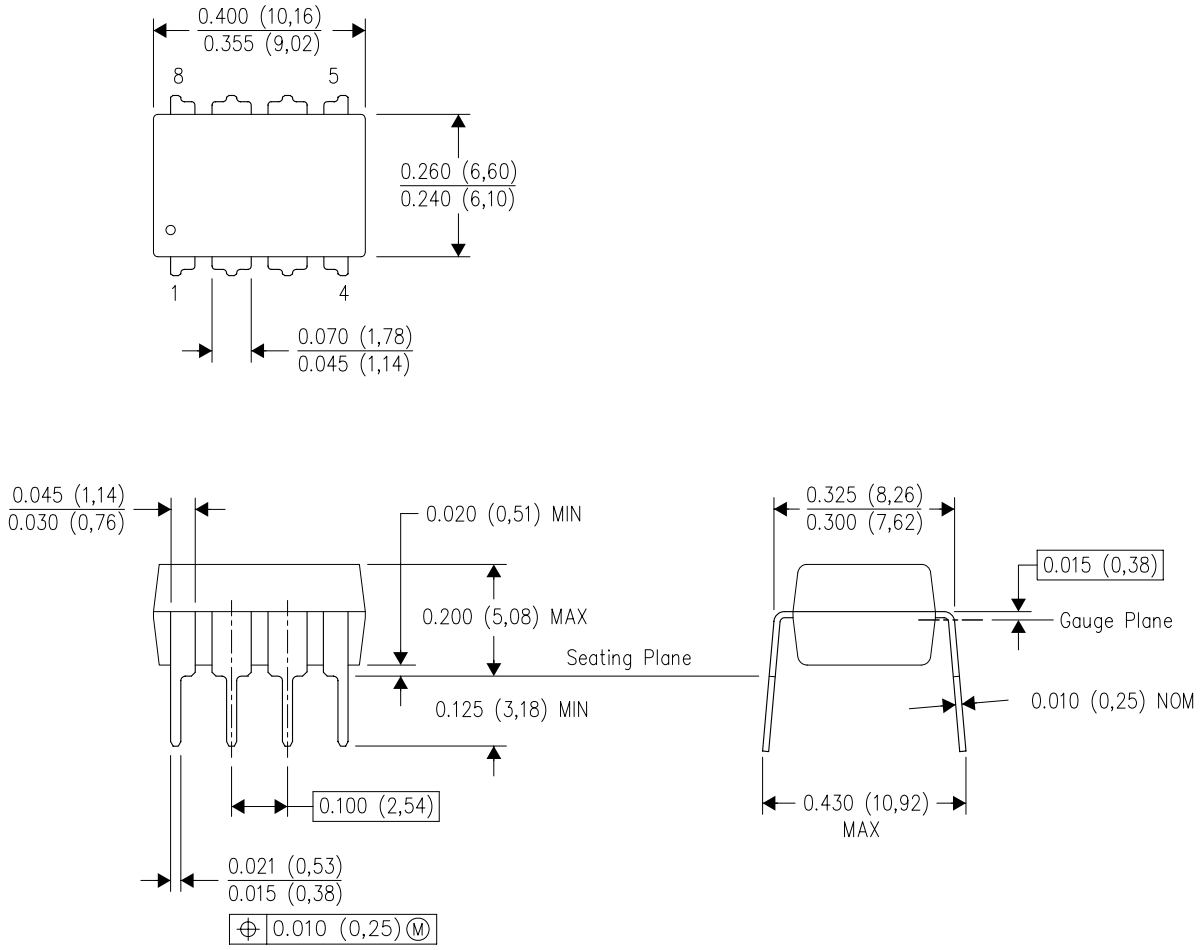
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

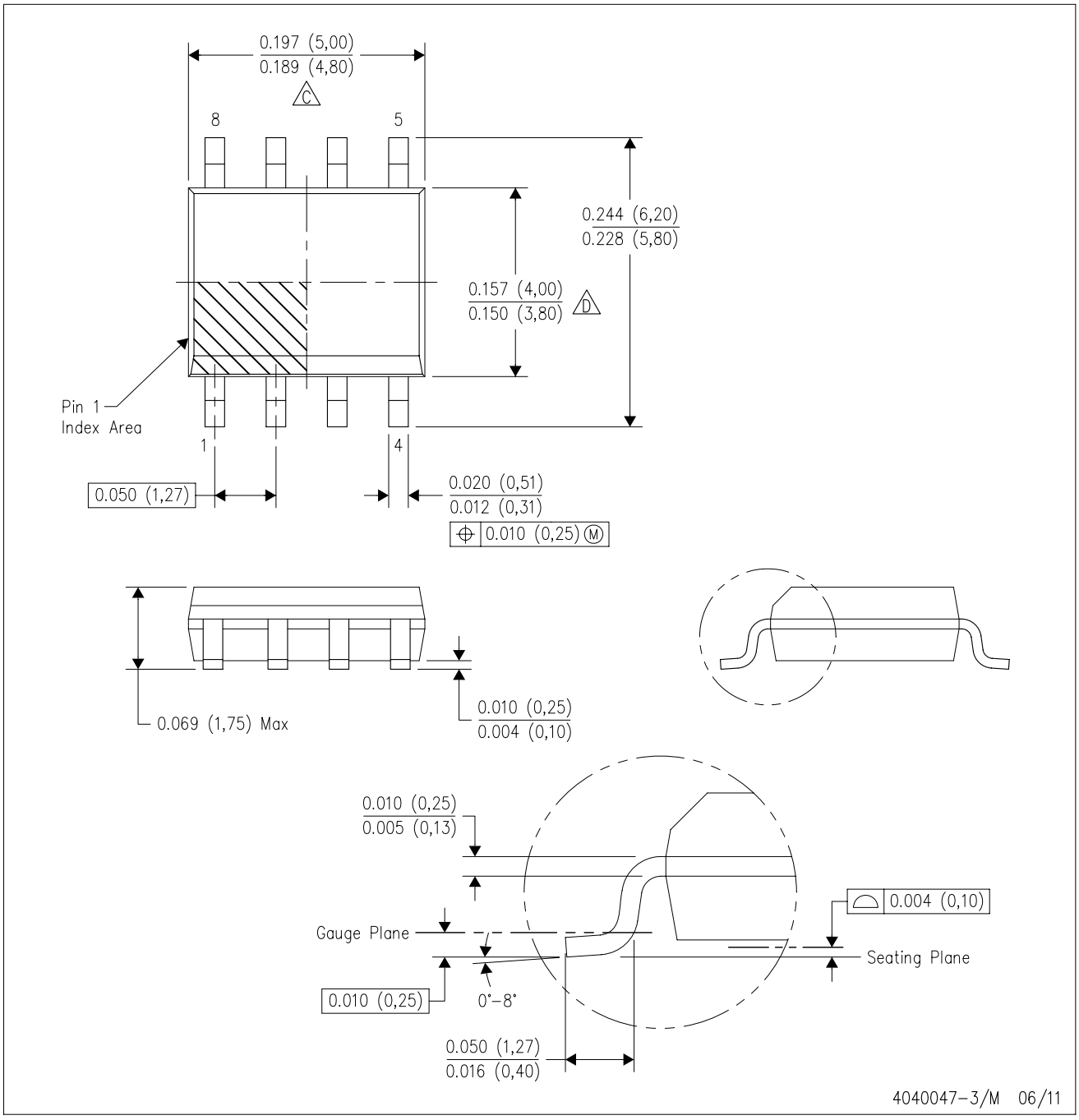
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC031QDR	SOIC	D	8	2500	367.0	367.0	38.0
SN65LBC031QDRG4	SOIC	D	8	2500	367.0	367.0	38.0
SN75LBC031DR	SOIC	D	8	2500	367.0	367.0	38.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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