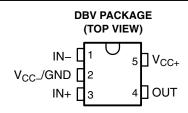
SLCS128F - APRIL 1996 - REVISED JUNE 2007

- Low-Voltage and Single-Supply Operation
 V_{CC} = 2 V to 7 V
- Common-Mode Voltage Range Includes Ground
- Fast Response Time . . . 0.7 μs Typ
- Low Supply Current . . . 80 μA Typ and 150 μA Max
- Fully Specified at 3-V and 5-V Supply Voltages



description/ordering informaton

The TLV1391 is a differential comparator built using a Texas Instruments low-voltage, high-speed bipolar process. These devices have been developed specifically for low-voltage, single-supply applications. Their enhanced performance makes them excellent replacements for the LM393 in the improved 3-V and 5-V system designs.

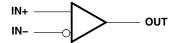
The TLV1391, with its typical supply current of only 80 μ A, is ideal for low-power systems. Response time also has been improved to 0.7 μ s.

ORDERING INFORMATION

T _A	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING [‡]
0°C to 70°C	COT 00 F (DD)/\	Reel of 3000	TLV1391CDBVR	Van
−0°C to 70°C	SOT-23-5 (DBV)	Reel of 250	TLV1391CDBVT	Y3D_
4000 to 0500	COT OO F (DD)/\	Reel of 3000	TLV1391IDBVR	Voc
–40°C to 85°C	SOT-23-5 (DBV)	Reel of 250	TLV1391IDBVT	Y3E_

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol (each comparator)



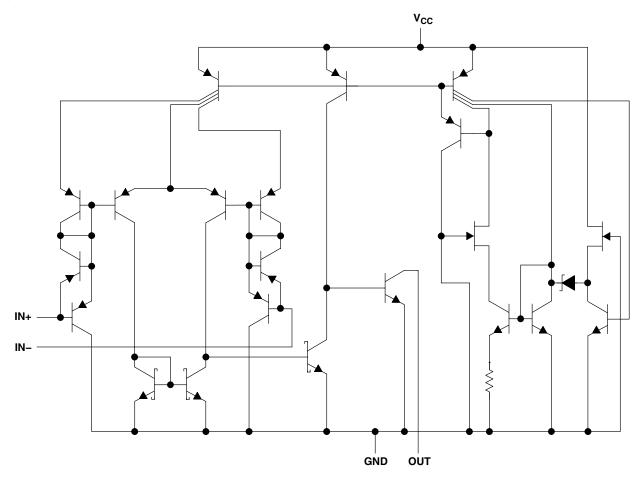


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[‡] The actual top-side marking has one additional character that designates the wafer fab/assembly site.

equivalent schematic



COMPONENT COUNT							
Transistors	26						
Resistors	1						
Diodes	4						
Epi-FET	1						



TLV1391 SINGLE DIFFERENTIAL COMPARATORS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	7 V
Differential input voltage, V _{ID} (see Note 2)	±7 V
Input voltage range, V _I (any input)	–0.3 V to V _{CC}
Output voltage, VO	7 V
Output current, IO (each output)	20 mA
Duration of short-circuit current to GND (see Note 3)	Unlimited
Package thermal impedance, θ_{JA} (see Note 4 and 5)	206°C/W
Operating virtual junction temperature, T _J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network GND.
 - 2. Differential voltages are at the noninverting input with respect to the inverting input.
 - 3. Short circuits from the outputs to V_{CC} can cause excessive heating and eventual destruction of the chip.
 - 4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 - 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2	7	V
_	Operating free-air temperature	391C	0	70	00
1A	TLV13	391I	-40	85	°C



TLV1391 SINGLE DIFFERENTIAL COMPARATORS

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electrical characteristics, $V_{CC} = 3 V$

	PARAMETER	TEST	CONDITIONS	T _A	MIN	TYP	MAX	UNIT	
V	loon it offert welleng	V 44V	V V (min)	25°C		1.5	5	\/	
V_{IO}	Input offset voltage	$V_0 = 1.4 V,$	$V_{IC} = V_{ICR}(min)$	Full range			9	mV	
V	Common-mode input voltage range			25°C	0 to V _{CC} -1.5	0 to V _{CC} -1.2		V	
V _{ICR}				Full range	0 to V _{CC} -2			V	
V_{OL}	Low-level output voltage	$V_{ID} = -1 V$,	$I_{OL} = 500 \mu A$	Full range		120	300	mV	
	loon to effect accompany	V 4.4V		25°C		5	50	- A	
I _{IO}	Input offset current	$V_0 = 1.4 \text{ V}$		Full range			150	nA	
		V _O = 1.4 V		25°C		-40	-250	4	
I _{IB}	Input bias current			Full range			-400	nA	
		$V_{ID} = 1 V$,	V _{OH} = 3 V	25°C		0.1			
Іон	High-level output current	$V_{ID} = 1 V$,	V _{OH} = 5 V	Full range			100	nA	
l _{OL}	Low-level output current	$V_{ID} = -1 V$,	V _{OL} = 1.5 V	25°C	500			μΑ	
	Hade level average average	\ \ \ \ \		25°C		80	125		
I _{CC(H)}	High-level supply current	$V_O = V_{OH}$		Full range		_	150	μΑ	
	Low level cumply current	, , , , , , , , , , , , , , , , , , ,		25°C		80	125		
I _{CC(L)}	Low-level supply current	$V_O = V_{OL}$		Full range			150	μΑ	

switching characteristics, V_{CC} = 3 V, C_L = 15 pF $^\dagger,\,T_A$ = 25 $^\circ C$

PARAMETER	TEST CONDITION	DNS	TYP	UNIT
Response time	100-mV input step with 5-mV overdrive,	$R_L = 5.1 \text{ k}\Omega$	0.7	μs

[†] C_L includes the probe and jig capacitance.



electrical characteristics, $V_{CC} = 5 V$

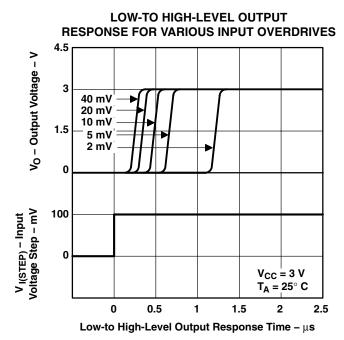
	PARAMETER	TEST	CONDITIONS	T _A	MIN	TYP	MAX	UNIT	
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	land offertualtens	V 44V	V V (main)	25°C		1.5	5	\/	
V _{IO}	Input offset voltage	$V_0 = 1.4 V,$	$V_{IC} = V_{ICR}(min)$	Full range			9	mV	
V	Common-mode input voltage range			25°C	0 to V _{CC} -1.5	0 to V _{CC} -1.2		V	
V _{ICR}				Full range	0 to V _{CC} -2			V	
V_{OL}	Low-level output voltage	$V_{ID} = -1 V$,	$I_{OL} = 500 \mu A$	Full range		120	300	mV	
l .	I _{IO} Input offset current	V 44V		25°C		5	50	~ ^	
IO		$V_0 = 1.4 \text{ V}$		Full range			150	nA	
				25°C		-40	-250	^	
I _{IB}	Input bias current	$V_0 = 1.4 \text{ V}$		Full range			-400	nA	
	I Park Tarrel and and annual	$V_{ID} = 1 V$,	V _{OH} = 3 V	25°C		0.1		A	
Іон	High-level output current	$V_{ID} = 1 V$,	V _{OH} = 5 V	Full range			100	nA	
I _{OL}	Low-level output current	$V_{ID} = -1 V$,	V _{OL} = 1.5 V	25°C	600			μΑ	
	I Park I and a mark a mark	, , ,,		25°C		100	150		
I _{CC(H)}	High-level supply current	$V_O = V_{OH}$		Full range			175	μΑ	
	Low lovel cumby cumont			25°C		100	150		
I _{CC(L)}	Low-level supply current	$V_O = V_{OL}$		Full range			175	μΑ	

switching characteristics, V_{CC} = 5 V, C_L = 15 pF†, T_A = 25°C

PARAMETER	TEST CONDITIONS	TEST CONDITIONS						
Deenenes time	100-mV input step with 5-mV overdrive,	$R_L = 5.1 \text{ k}\Omega$	0.65					
Response time	TTL-level input step,	$R_L = 5.1 \text{ k}\Omega$	0.18	μs				

[†] C_L includes the probe and jig capacitance.

TYPICAL CHARACTERISTICS





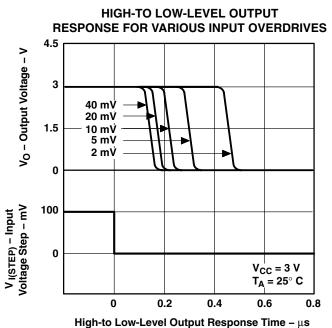


Figure 2

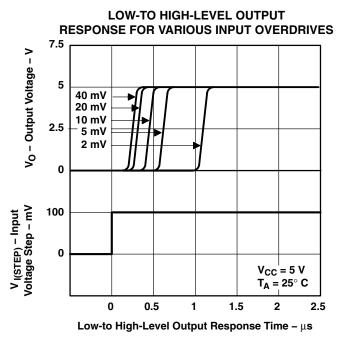


Figure 3

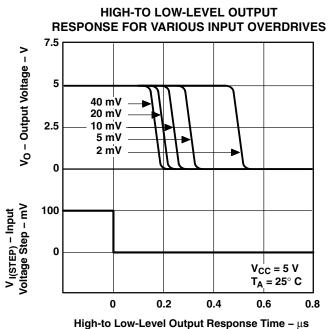


Figure 4





18-Sep-2015

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TLV1391CDBV	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	0 to 70		
TLV1391CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	(Y3D6 ~ Y3DG)	Samples
TLV1391CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	(Y3DB ~ Y3DG)	Sample
TLV1391CDBVTG4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	0 to 70		Sample
TLV1391IDBV	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85		
TLV1391IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(Y3E6 ~ Y3EB)	Sample
TLV1391IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3EB	Sample
TLV1391IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y3EB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



PACKAGE OPTION ADDENDUM

18-Sep-2015

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All differsions are norminal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1391CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV1391CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV1391IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV1391IDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

www.ti.com 5-Nov-2014



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1391CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1391CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV1391IDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TLV1391IDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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