National Semiconductor

March 1999

LM4835 Boomer® Audio Power Amplifier Series
Stereo 2W Audio Power Amplifiers with DC Volume Control and Selectable Gain

General Description

The LM4835 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD or 2.2W into 3Ω (Note 2) with less than 1.0% THD.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4835 incorporates a DC volume control, stereo bridged audio power amplifiers and a selectable gain or bass boost, making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4835 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note 1: When properly mounted to the circuit board, the LM4835MTE will deliver 2W into 4Ω. The LM4835MT will deliver 1.1W into 8Ω. See the Application Information section for LM4835MTE usage information.

Note 2: An LM4835MTE which has been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Key Specifications

- P_O at 1% THD+N
  - into 3Ω (LM4835MTE) 2.2W(typ)
  - into 4Ω (LM4835MTE) 2.0W(typ)
  - into 8Ω (LM4835) 1.1W(typ)
- Single-ended mode - THD+N at 85mW into 32Ω 1.0%(typ)
- Shutdown current 0.7µA(typ)

Features

- PC98 Compliant
- DC Volume Control Interface
- System Beep Detect
- Stereo switchable bridged/single-ended power amplifiers
- Selectable internal/external gain and bass boost configurable
- “Click and pop” suppression circuitry
- Thermal shutdown protection circuitry

Applications

- Portable and Desktop Computers
- Multimedia Monitors
- Portable Radios, PDAs, and Portable TVs

Block Diagram

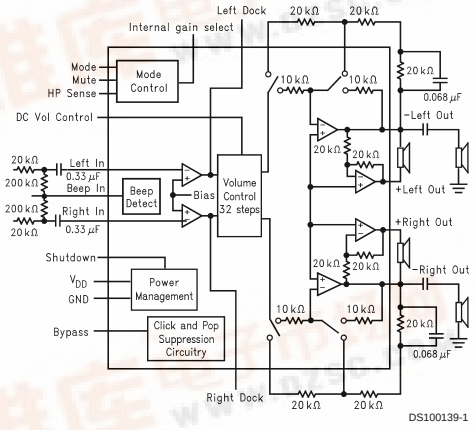
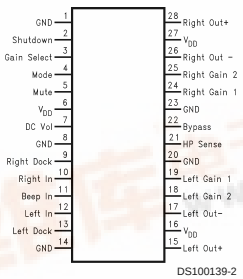


FIGURE 1. LM4835 Block Diagram

Connection Diagram

TSSOP Package



Top View
Order Number LM4835MT
See NS Package Number MTC28 for TSSOP
Order Number LM4835MTE
See NS Package Number MXA28A for Exposed DAP TSSOP

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Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65˚C to +150˚C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation	Internally limited
ESD Susceptibility (Note 12)	2000V
ESD Susceptibility (Note 13)	200V
Junction Temperature	150˚C
Soldering Information	
Small Outline Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 “Surface Mounting and their Effects on Product Reliability” for other methods of soldering surface mount devices.

θ_{JC} (typ) — MTC28	20˚C/W
θ_{JA} (typ) — MTC28	80˚C/W
θ_{JC} (typ) — MXA28A	2˚C/W
θ_{JA} (typ) — MXA28A (Note 4)	41˚C/W
θ_{JA} (typ) — MXA28A (Note 3)	54˚C/W
θ_{JA} (typ) — MXA28A (Note 5)	59˚C/W
θ_{JA} (typ) — MXA28A (Note 6)	93˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	−40˚C ≤TA ≤ 85˚C
Supply Voltage	2.7V≤ V_{DD} ≤ 5.5V

Electrical Characteristics for Entire IC

(Notes 7, 10)
The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4835		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
V_{DD}	Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A	15	30	mA (max)
I_{SD}	Shutdown Current	$V_{pin\ 2} = V_{DD}$	0.7	2.0	µA (max)
V_{IH}	Headphone Sense High Input Voltage			4	V (min)
V_{IL}	Headphone Sense Low Input Voltage			0.8	V (max)

Electrical Characteristics for Volume Attenuators

(Notes 7, 10)
The following specifications apply for V_{DD} = 5V. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4835		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
C_{RANGE}	Attenuator Range	Gain with $V_{pin\ 7}$ = 5V	0	±0.5	dB (max)
		Attenuation with $V_{pin\ 7}$ = 0V	-81	-80	dB (min)
A_M	Mute Attenuation	$V_{pin\ 5}$ = 5V, Bridged Mode	-88	-80	dB (min)
		$V_{pin\ 5}$ = 5V, Single-Ended Mode	-88	-80	dB (min)

Electrical Characteristics for Single-Ended Mode Operation

(Notes 7, 10)
The following specifications apply for V_{DD} = 5V. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4835		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
P_O	Output Power	THD = 1.0%; f = 1kHz; R_L = 32Ω	85		mW
		THD = 10%; f = 1 kHz; R_L = 32Ω	95		mW
THD+N	Total Harmonic Distortion+Noise	V_{OUT} = 1V_{RMS}, f=1kHz, R_L = 10kΩ, A_{VD} = 1	0.065		%

Electrical Characteristics for Single-Ended Mode Operation (Continued)

(Notes 7, 10)
The following specifications apply for V_{DD} = 5V. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4835		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f =120 Hz, V_{RIPPLE} = 200 mVrms	58		dB
SNR	Signal to Noise Ratio	P_{OUT} =75 mW, R_L = 32Ω, A-Wtd Filter	102		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	65		dB

Electrical Characteristics for Bridged Mode Operation

(Notes 7, 10)
The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A = 25˚C.

Symbol	Parameter	Conditions	LM4835		Units (Limits)
			Typical (Note 14)	Limit (Note 15)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	30	mV (max)
P_O	Output Power	THD + N = 1.0%; f=1kHz; R_L = 3Ω (Note 8)	2.2		W
		THD + N = 1.0%; f=1kHz; R_L = 4Ω (Note 9)	2		W
		THD = 0.5% (max);f = 1 kHz; R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%;f = 1 kHz; R_L = 8Ω	1.5		W
THD+N	Total Harmonic Distortion+Noise	P_O = 1W, 20 Hz< f < 20 kHz, R_L = 8Ω, A_{VD} = 2	0.3		%
		P_O = 340 mW, R_L = 32Ω	1.0		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, f = 120 Hz, V_{RIPPLE} = 200 mVrms; R_L = 8Ω	74		dB
SNR	Signal to Noise Ratio	V_{DD} = 5V, P_{OUT} = 1.1W, R_L = 8Ω, A-Wtd Filter	93		dB
X_{talk}	Channel Separation	f=1kHz, C_B = 1.0 µF	70		dB

Note 3: The θ_{JA} given is for an MXA28A package whose exposed-DAP is soldered to an exposed $2in^2$ piece of 1 ounce printed circuit board copper.

Note 4: The θ_{JA} given is for an MXA28A package whose exposed-DAP is soldered to a $2in^2$ piece of 1 ounce printed circuit board copper on a bottom side layer through 21 8mil vias.

Note 5: The θ_{JA} given is for an MXA28A package whose exposed-DAP is soldered to an exposed $1in^2$ piece of 1 ounce printed circuit board copper.

Note 6: The θ_{JA} given is for an MXA28A package whose exposed-DAP is not soldered to any copper.

Note 7: All voltages are measured with respect to the ground pins, unless otherwise specified. All specifications are tested using the typical application as shown in *Figure 1.*

Note 8: When driving 3Ω loads from a 5V supply the LM4835MTE must be mounted to the circuit board and forced-air cooled.

Note 9: When driving 4Ω loads from a 5V supply the LM4835MTE must be mounted to the circuit board.

Note 10: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Marshall Chiu feels there are better ways to obtain "More Wattage in the Cottage." Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 11: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4835MT, T_{JMAX} = 150˚C, and the typical junction-to-ambient thermal resistance, when board mounted, is 80˚C/W assuming the MTC28 package.

Note 12: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 13: Machine Model, 220 pF–240 pF discharged through all pins.

Note 14: Typicals are measured at 25˚C and represent the parametric norm.

Note 15: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Typical Application

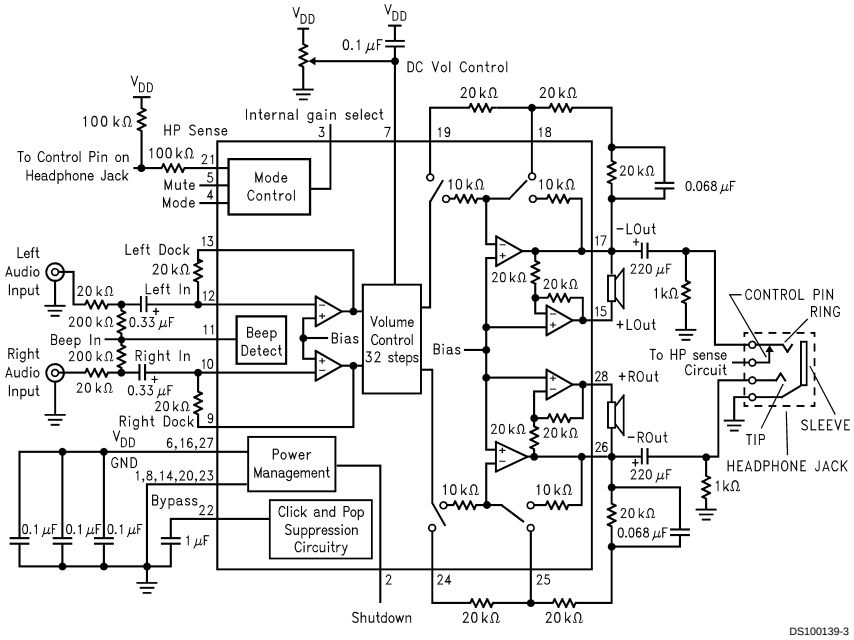


FIGURE 2. Typical Application Circuit

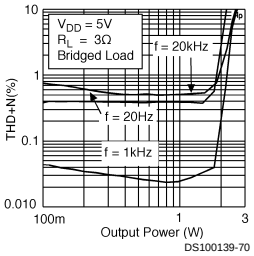
Truth Table for Logic Inputs (Note 16)

Mute	Mode	HP Sense	DC Vol. Control	Bridged Output	Single-Ended Output
0	0	0	Fixed Level	Vol. Fixed	_
0	0	1	Fixed Level	Muted	Vol. Fixed
0	1	0	Adjustable	Vol. Changes	_
0	1	1	Adjustable	Muted	Vol. Changes
1	X	X	_	Muted	Muted

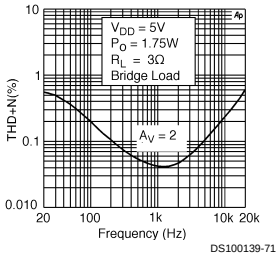
Note 16: If system beep is detected on the Beep In pin (pin 11), the system beep will be passed through the bridged amplifier regardless of the logic of the Mute and HP sense pins.

Typical Performance Characteristics
MTE Specific Characteristics

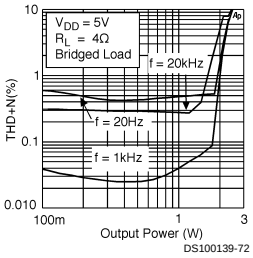
LM4835MTE
THD+N vs Output Power



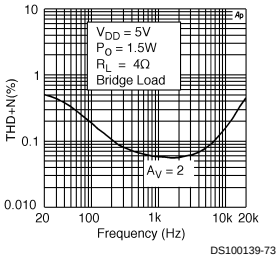
LM4835MTE
THD+N vs Frequency



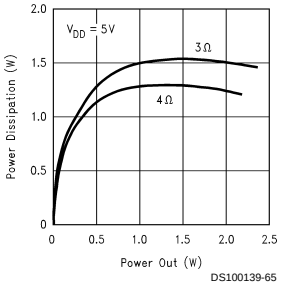
LM4835MTE
THD+N vs Output Power



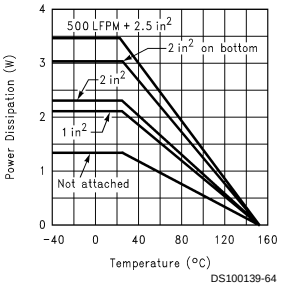
LM4835MTE
THD+N vs Frequency



LM4835MTE
Power Dissipation vs Output Power



LM4835MTE(Note 17)
Power Derating Curve



Note 17: These curves show the thermal dissipation ability of the LM4835MTE at different ambient temperatures given these conditions:

500LFPM + 2in^2: The part is soldered to a 2in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it.

2in^{2}on bottom: The part is soldered to a 2in^2, 1oz. copper plane that is on the bottom side of the PC board through 21 8 mil vias.

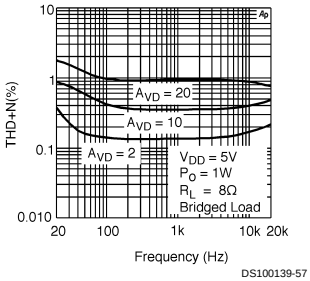
2in^2: The part is soldered to a 2in^2, 1oz. copper plane.

1in^2: The part is soldered to a 1in^2, 1oz. copper plane.

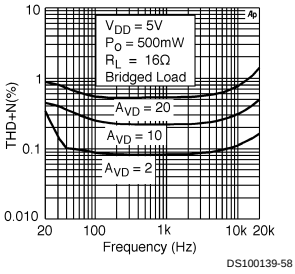
Not Attached: The part is not soldered down and is not forced-air cooled.

Non-MTE Specific Characteristics

THD+N vs Frequency

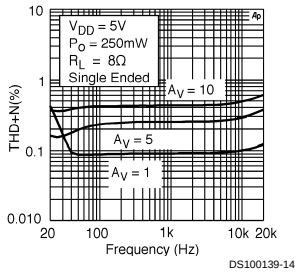


THD+N vs Frequency



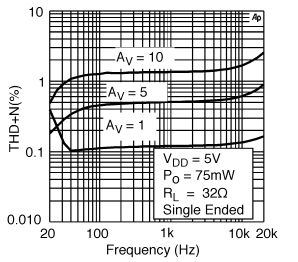
Non-MTE Specific Characteristics (Continued)

THD+N vs Frequency



DS100139-14

THD+N vs Frequency



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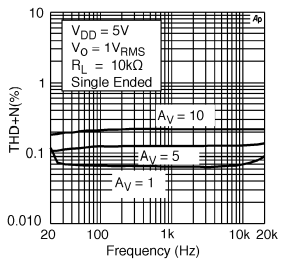
THD+N vs Frequency



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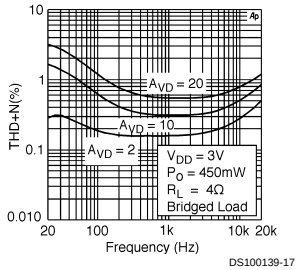
THD+N vs Frequency



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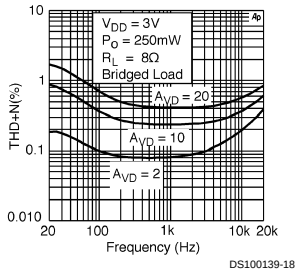
THD+N vs Frequency



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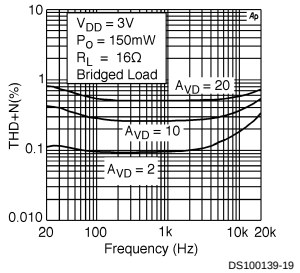
THD+N vs Frequency



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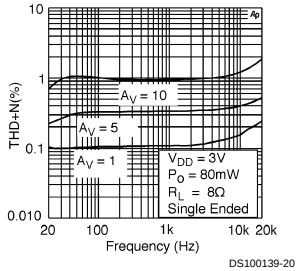
THD+N vs Frequency



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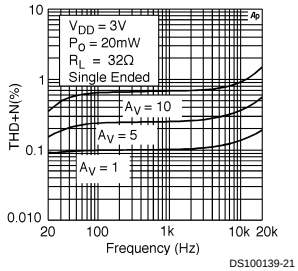
THD+N vs Frequency



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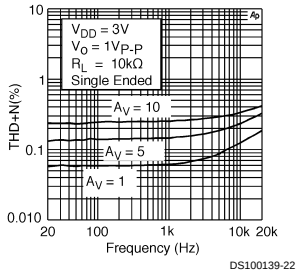
THD+N vs Frequency



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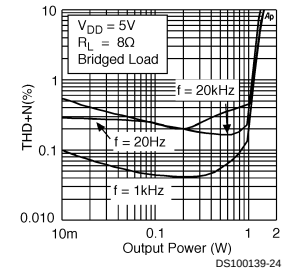
THD+N vs Output Power



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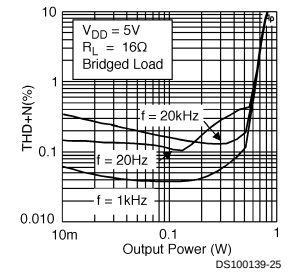
THD+N vs Output Power



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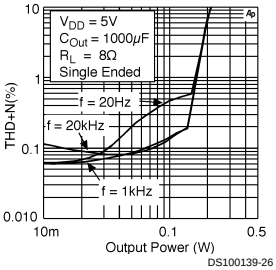
Non-MTE Specific Characteristics (Continued)

THD+N vs Output Power



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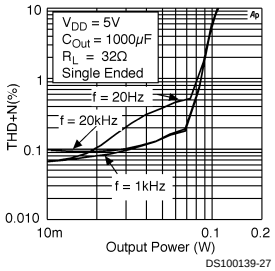
THD+N vs Output Power



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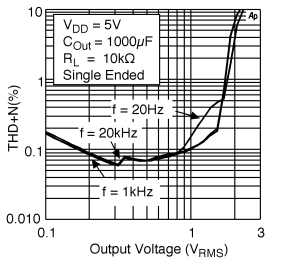
THD+N vs Output Power



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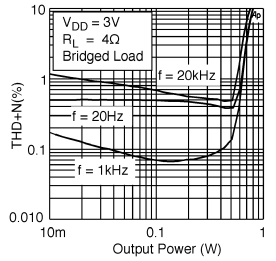
THD+N vs Output Power



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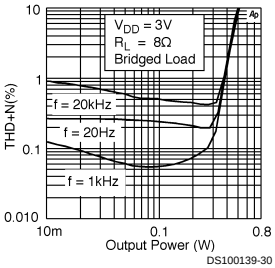
THD+N vs Output Power



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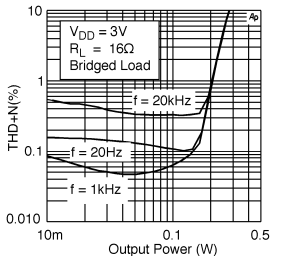
THD+N vs Output Power



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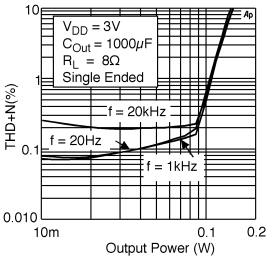
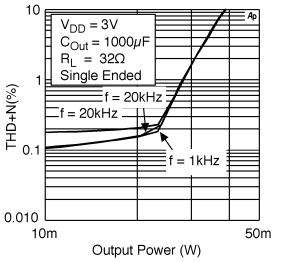
THD+N vs Output Power



DS100139-32

THD+N vs Output Power



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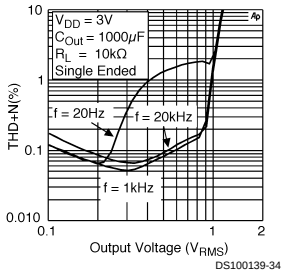
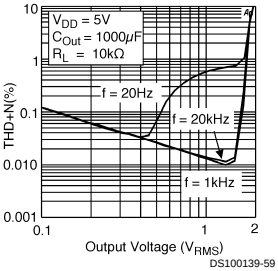
THD+N vs Output Power



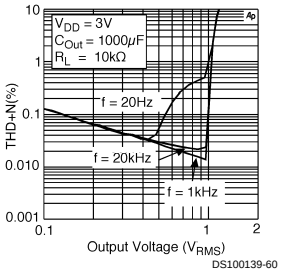
DS100139-34

THD+N vs Output Voltage
Docking Station Pins



DS100139-59

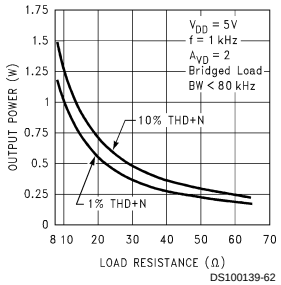
THD+N vs Output Voltage
Docking Station Pins



DS100139-60

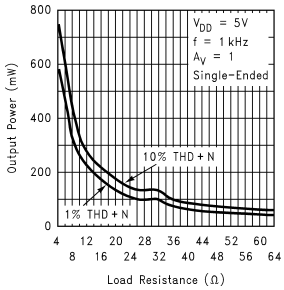
Non-MTE Specific Characteristics (Continued)

Output Power vs Load Resistance



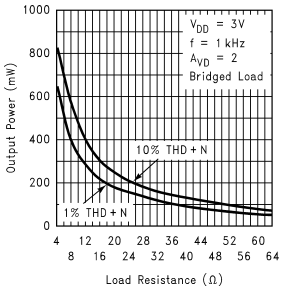
DS100139-62

Output Power vs Load Resistance



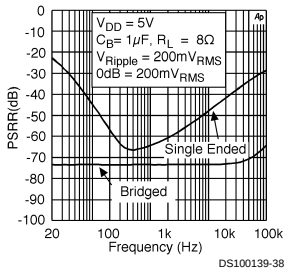
DS100139-6

Output Power vs Load Resistance



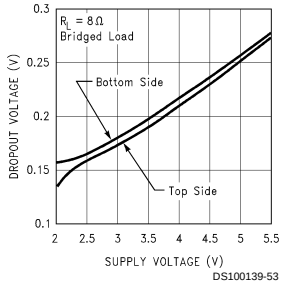
DS100139-7

Power Supply Rejection Ratio



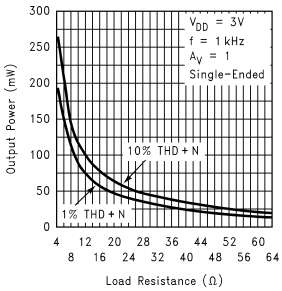
DS100139-38

Dropout Voltage



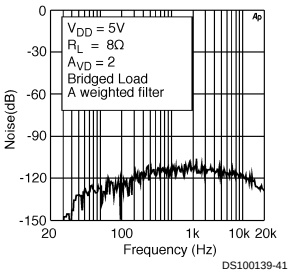
DS100139-53

Output Power vs Load Resistance



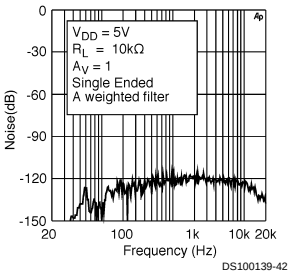
DS100139-8

Noise Floor



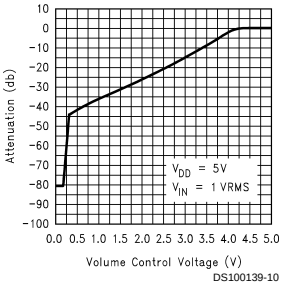
DS100139-41

Noise Floor



DS100139-42

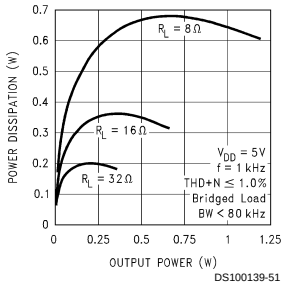
Volume Control Characteristics



DS100139-10

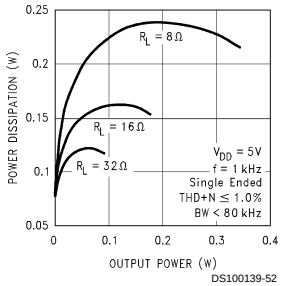
Non-MTE Specific Characteristics (Continued)

Power Dissipation vs Output Power



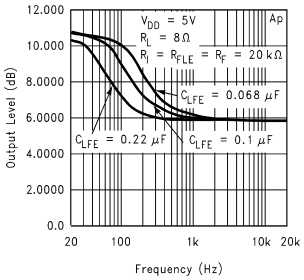
DS100139-51

Power Dissipation vs Output Power



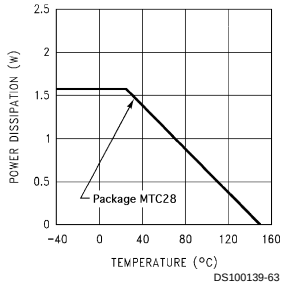
DS100139-52

External Gain/ Bass Boost Characteristics



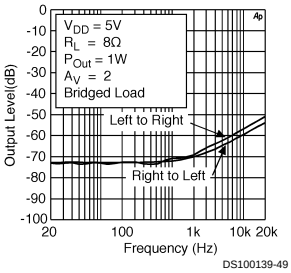
DS100139-61

Power Derating Curve



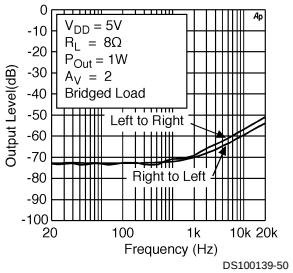
DS100139-63

Crosstalk



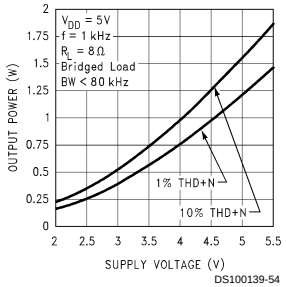
DS100139-49

Crosstalk



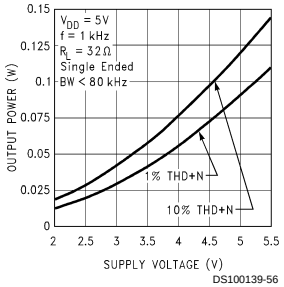
DS100139-50

Output Power vs Supply voltage



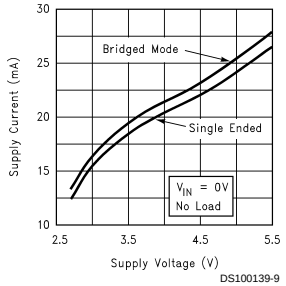
DS100139-54

Output Power vs Supply Voltage



DS100139-56

Supply Current vs Supply Voltage



DS100139-9

Application Information

EXPOSED-DAP MOUNTING CONSIDERATIONS

The exposed-DAP (die attach pad) must be tied to ground. The exposed-DAP of the LM4835MTE requires special attention to thermal design. If thermal design issues are not properly addressed, an LM4835MTE driving 4Ω will go into thermal shutdown.

The exposed-DAP on the bottom of the LM4835MTE should be soldered down to a copper plane on the circuit board. The copper plane will conduct heat away from the exposed-DAP. If the copper plane is not on the top surface of the circuit board, 20 to 30 vias of 0.010 inches or smaller in diameter should be used to thermally couple the exposed-DAP to the plane. For good thermal conduction, the vias must be plated-through and solder-filled.

The copper plane used to conduct heat away from the exposed-DAP should be as large as practical. If the plane is on the same side of the circuit board as the exposed-DAP, 2 in^2 is the minimum for 5V operation into 4Ω. If the heat sink plane is buried or not on the same side as the exposed-DAP, 5in^2 is the minimum for 5V operation into 4Ω. If the ambient temperature is higher than 25˚C, a larger copper plane or forced-air cooling may be required to keep the LM4835MTE junction temperature below the thermal shutdown temperature (150˚C). See the power derating curve for the LM4835MTE for derating information.

The LM4835MTE requires forced-air cooling when operating into 3Ω.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = (V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

However, a direct consequence of the increased power delivered to the load by a bridged amplifier is an increase in internal power dissipation. Equation 2 states the maximum power dissipation point for a bridged amplifier operating at a given supply voltage and driving a specified load.

$$P_{DMAX} = 4(V_{DD})^2/(2\pi^2 R_L) \quad (2)$$

Since theLM4835 is a stereo power amplifier, the maximum internal power dissipation is two times that of Equation 1 or Equation 2 depending on the mode of operation. Even with the power dissipation of the stereo amplifiers, the LM4835 does not require heatsinking. The power dissipation from the amplifiers, must not be greater than the package power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA} \quad (3)$$

For the LM4835 TSSOP package, θ_{JA} = 80˚C/W and T_{JMAX} = 150˚C. Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 and 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased, or the ambient temperature reduced. For the typical application of a 5V power supply, with an 8Ω bridged loads, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 48˚C provided that device operation is around the maximum power dissipation points. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature can be increased. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers.

LAYOUT

As stated in the Grounding section, placement of ground return lines is imperative in maintaining the highest level of system performance. It is not only important to route the correct ground return lines together, but also to be aware of where the ground return lines are routed with respect to each other. The output load ground returns should be physically located as far as possible from low signal level lines and their ground return lines.

3Ω and 4Ω Layout Considerations

With low impedance loads, the output power at the loads is heavily dependent on trace resistance from the output pins of the LM4835. Traces from the output of the LM4835MTE to the load or load connectors should be as wide as practical. Any resistance in the output traces will reduce the power delivered to the load. For example, with a 4Ω load and 0.1Ω of trace resistance in each output, output power at the load drops from 2W to 1.8W.

Output power is also dependent on supply regulation. To keep the supply voltage from sagging under full output conditions, the supply traces should be as wide as practical.

Grounding

In order to achieve the best possible performance, there are certain grounding techniques to be followed. All input reference grounds should be tied with their respective source grounds and brought back to the power supply ground separately from the output load ground returns. Bringing the ground returns for the output loads back to the supply separately will keep large signal currents from interfering with the stable AC input ground references. The exposed-DAP of the LM4835MTE package must be tied to ground.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor is improved PSRR due to increased half-supply stability. Typical applications employ a 5 volt regulator with 10 µF and a 0.1 µF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4835. The selection of bypass capacitors, especially C_B, is thus dependant upon desired PSRR requirements, click and pop performance as explained in the section, **Proper Selection of External Components,** system cost, and size constraints. It is also recommended to decouple each of the V_{DD} pins with a 0.1µF capacitor to ground.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4835 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4835's bridged amplifier should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large in-

Application Information (Continued)

put signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs.

Besides gain, one of the major considerations is the closed-loop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 3*. Both the input coupling capacitor, C_I, and the output coupling capacitor form first order high pass filters which limit low frequency response given in Equations 4 and 5.

$$f_{IC} = 1/(2\pi R_i C_i) \quad (4)$$

$$f_{OC} = 1/(2\pi R_L C_O) \quad (5)$$

These values should be chosen based on required frequency response.

Selection of Input and Output Capacitor Size

Large input and output capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. In many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100 Hz–150 Hz. In this case, usinga large input or output capacitor may not increase system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}.) This charge comes from the output through the feedback and is apt to create pops once the device is enabled. By minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

CLICK AND POP CIRCUITRY

The LM4835 contains circuitry to minimize turn-on transients or “click and pops”. In this case, turn-on refers to either power supply turn-on or the device coming out of shutdown mode. When the device is turning on, the amplifiers are internally muted. An internal current source ramps up the voltage of the bypass pin. Both the inputs and outputs ideally track the voltage at the bypass pin. The device will remain in mute mode until the bypass pin has reached its half supply voltage, 1/2 V_{DD}. As soon as the bypass node is stable, the device will become fully operational.

Although the bypass pin current source cannot be modified, the size of the bypass capacitor, C_B, can be changed to alter the device turn-on time and the amount of “click and pop”. By increasing C_B, the amount of turn-on pop can be reduced. However, the trade-off for using a larger bypass capacitor is an increase in the turn-on time for the device. Reducing C_B will decrease turn-on time and increase “click and pop”.

There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for different values of C_B:

C_B	T_{ON}
0.01 µF	2 ms
0.1 µF	20 ms
0.22 µF	42 ms
0.47 µF	84 ms
1.0 µF	200 ms
4.7 µF	1sec

In order to eliminate “click and pop”, all capacitors must be discharged before turn-on. Rapid on/off switching of the device or shutdown function may cause the “click and pop” circuitry to not operate fully, resulting in increased “click and pop” noise.

In systems where the line out and headphone jack are the same, the output coupling cap, C_O, is of particular concern. C_O is chosen for a desired cutoff frequency with a headphone load. This desired cutoff frequency will change when the headphone load is replaced by a high impedance line out load(powered speakers). The input impedance of headphones are typically between 32Ω and 64Ω. Whereas, the input impedance of powered speakers can vary from 1kΩ to 100kΩ. As the RC time constant of the load and the output coupling capacitor increases, the turn off transients are increased.

To improve click and pop performance in this situation, external resistor R7 should be added as shown in Figure 4. The recommended value for R7 is between 150Ω to 1kΩ. To achieve virtually clickless and popless performance R7 = 150Ω, C_O = 220µF, and C_B = 1.0µF should be used. Lower values of R6 will result in better click and pop performance. However, it should be understood that lower resistance values of R7 will increase current consumption.

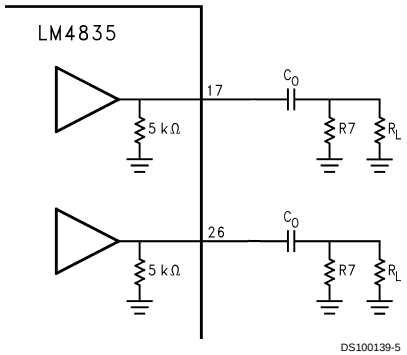


FIGURE 3. Resistor for Varying Output Loads

DOCKING STATION

In an application such as a notebook computer, docking station or line level outputs may be required. Pin 9 and Pin 13 can drive loads greater than 1kΩ rail to rail. These pins are tied to the output of the input op-amp to drive powered speakers and other high impedance loads. Output coupling capacitors need to be placed in series with the load. The recommended values of the capacitors are between 0.33µF to 1.0µF with the positive side of the capacitors toward the IC. The outputs of the docking station pins cannot be attenuated with the DC volume control. However the gain of the outputs can be configured by adjusting the feedback and input resistors for the input op-amp. The input op-amp is in an inverting configuration where the gain is:

$$R_F / R_i = - A_v$$

Note that by adjusting the gain of the input op-amp the overall gain of the output amplifiers are also affected. Although the single ended outputs of the output amplifiers can be used to drive line level outputs, it is recommended to use Pins 9 and 13 to achieve better performance.

Application Information (Continued)

BEEP DETECT FUNCTION

The Beep Detect pin (pin 11) is a mono input that detects the presence of a beep signal. When a signal greater than $2.5V_{P-P}$ (or 1/2 V_{DD}) is present at pin 11, the Beep Detect circuitry will enable the bridged amplifiers. Beep in signals less than $2.5V_{P-P}$ (or 1/2 V_{DD}) will not trigger the Beep Detect circuitry. When triggered, the Beep Detect circuitry will enable the bridged amplifiers regardless of the state of the mute, mode, or HP sense pins. As shown in the Fig. 2, a 200kΩ resistor is placed in series with the input capacitor. This 200kΩ resistor can be changed to vary the amplitude of the beep in signal. Higher values of the resistor will reduce the amplifier gain and attenuate the beep in signal. These resistors are required in order for the beep signal to pass to the output. The Beep Detect pin will not pass the beep signal to the output. In cases where system beeps are required when the system is in a suspended mode, the LM4835 must be brought out of shutdown before the beep in signal is input.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4835 contains a shutdown pin to externally turn off the bias circuitry. The LM4835 will shutdown when a logic high is placed on the shutdown pin. The trigger point between a logic low and logic high level is typically half supply. It is best to switch between ground and the supply V_{DD} to provide maximum device performance. By switching the shutdown pin to V_{DD}, the LM4835 supply current draw will be minimized. While the device will be disabled with shutdown pin voltages less than V_{DD}, the idle current may be greater than the typical value of 0.7 µA.The shutdown pin should not be floated, since this may result in an unwanted shutdown condition.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjuction with an external pull-up resistor. When the switch is closed,the shutdown pin is connected to ground and enables the amplifier. If the switch is open, then the external pull-up resistor will shutdown the LM4835. This scheme prevents the shutdown pin from floating.

MODE FUNCTION

The LM4835 was designed to operate in two modes. In mode 0 (lineout mode),where the mode pin (pin 4) is given a logic level low, the attenuation of the outputs are fixed at unity gain. In mode 1 (adjustable mode), where the mode pin is given a logic level high, the attenuation of the amplifier outputs is controlled through the DC voltage at pin 7.

MUTE FUNCTION

By placing a logic level high on the mute pin (pin5), the outputs of the amplifiers and pins 9 and 13 will be muted. The beep in signal will be output even if the LM4835 is muted. The mute pin must not be floated.

HP SENSE FUNCTION

The LM4835 possesses a headphone sense pin (pin 21) that mutes the bridged amplifier, when given a logic high, so that headphone or line out operation can occur while the bridged connected load will be muted.

Figure 4 shows the implementation of the LM4835's headphone control function using a single-supply. The voltage divider of R1, R2, and R4 sets the voltage at the HP sense pin (pin 21) to be approximately 50 mV when there are no headphones plugged into the system. This logic-low voltage at the HP sense pin enables the bridged power amplifiers. Resistor R4 limits the amount of current flowing out of the HP sense pin when the voltage at that pin goes below ground resulting from the music coming from the headphone amplifier. Since the threshold of the HP sense pin is set at 4V (or 80% V_{DD}), the output swing cannot cause false triggering.

When a set of headphones are plugged into the system, the contact pin of the headphone jack is disconnected from the signal pin, interrupting the voltage divider set up by resistors R1, R2, and R4. Resistor R1 then pulls up the HP sense pin, enabling the headphone function and disabling the bridged amplifier. The headphone amplifier then drives the headphones, whose impedance is in parallel with resistor R2 and R3. Also shown in *Figure 4* are the electrical connections for the headphone jack and plug. A 3-wire plug consists of a Tip, Ring and Sleeve, where the Tip and Ring are signal carrying conductors and the Sleeve is the common ground return. One control pin contact for each headphone jack is sufficient to indicate that the user has inserted a plug into a jack and that another mode of operation is desired.

The LM4835 can be used to drive both a bridged 8Ω internal speaker and a pair of 32Ω speakers without using the HP sense circuit. In this case the HP sense is controlled by a microprocessor or a switch.

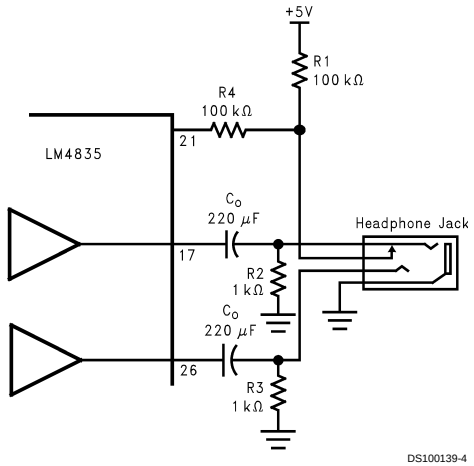


FIGURE 4. Headphone Sensing Circuit

GAIN SELECT FUNCTION (Bass Boost)

External gain/internal gain can be toggled by changing the logic at pin 3. A logic high will switch the power amplifiers to external gain mode. In external gain mode the gain of the amplifier is set by the external resistors. Whereas the internal gain mode sets the amplifiers to unity gain.

In some cases a designer may want to improve the low frequency response of the bridged amplifier or incorporate a bass boost feature. This bass boost can be useful in systems where speakers are housed in small enclosures. A resistor, R_{LFE}, and a capacitor, C_{LFE}, in parallel, can be placed in series with the feedback resistor of the bridged amplifier as seen in *Figure 5*.

Application Information (Continued)

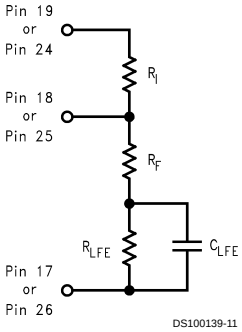


FIGURE 5. Low Frequency Enhancement

At low frequencies the capacitor will be virtually an open circuit. At high frequencies the capacitor will be virtually a short circuit. As a result of this, the gain of the bridge amplifier is increased at low frequencies. A first order pole is formed with a corner frequency at:

$$f_c = 1/(2\pi R_{LFE} C_{LFE})$$

The resulting low frequency differential gain of this bridged amplifier becomes:

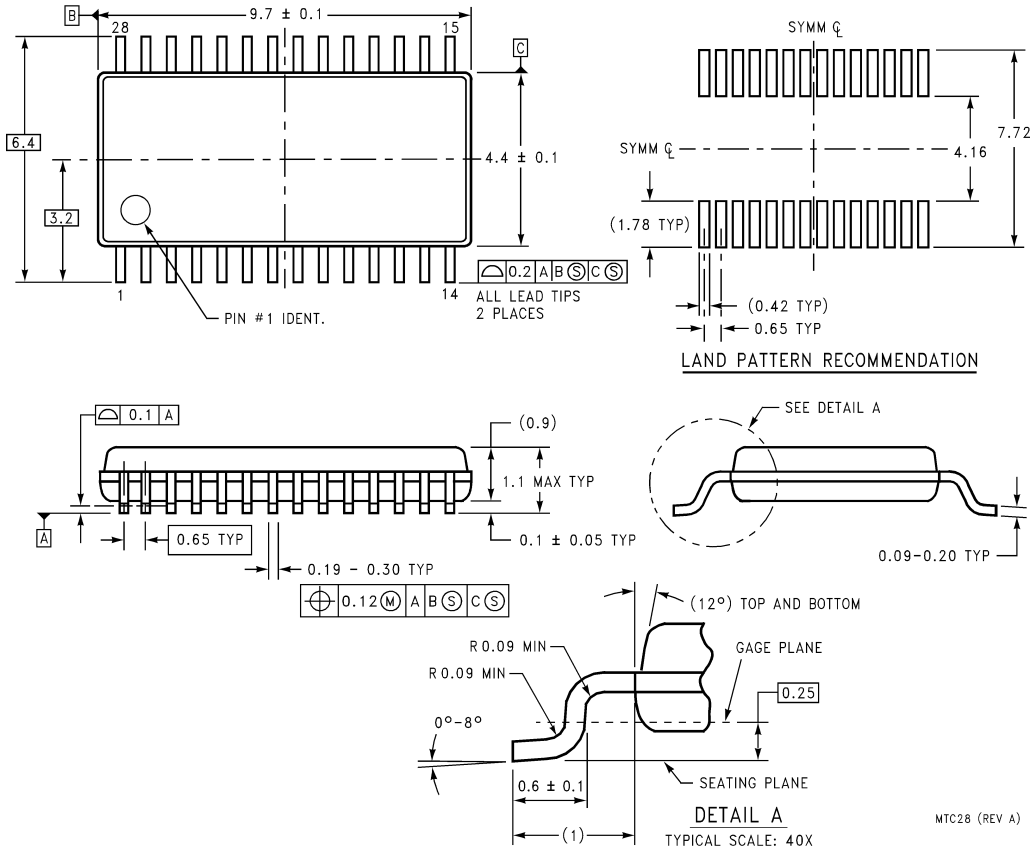
$$2(R_f + R_{LFE}) / R_i = A_{vd}$$

With R_F = 20kΩ, R_{LFE} = 20kΩ, and C_{LFE} = 0.068 µF, a first order pole is formed with a corner frequency of 120 Hz. At low frequencies the differential gain will be 4, assuming R_S = 20kΩ. The low frequency boost formulas assume that C_O, C_i, f_{IC}, f_{OC} allow the appropriate low frequency response. The bass boost feature is enabled/disable by toggling the logic at pin 3.

DC VOLUME CONTROL

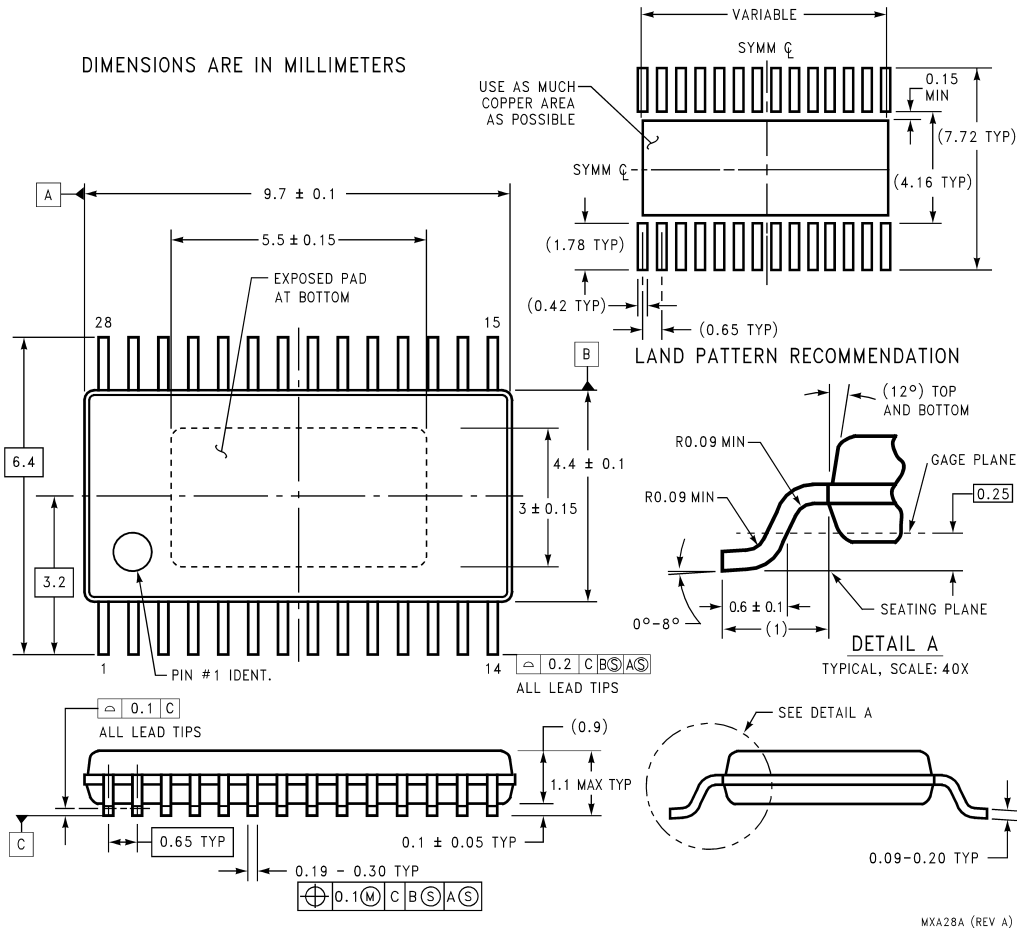
The DC voltage at the DC Volume Control pin (pin 7) determines the attenuation of output of the amplifiers. If the DC potential of pin 7 is at 4V (or 80% V_{DD}) the internal amplifiers are set at unity gain. The attenuator range is from 0dB (pin7 = 80% V_{DD}) to -81dB (pin7 = 0V). Any DC voltage greater than 4V (or 80% V_{DD}) will result in a gain of unity. When the mode pin is given a logic low,amplifiers will be fixed at a gain of unity regardless of the voltage of pin 7. Refer to the **Typical Performance Characteristics** for detailed information of the attenuation characteristics of the DC Volume Control pin.

Physical Dimensions inches (millimeters) unless otherwise noted



TSSOP Package
Order Number LM4835MT
NS Package Number MTC28 for TSSOP

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Exposed-DAP TSSOP Package
Order Number LM4835MTE
NS Package Number MXA28A for Exposed-DAP TSSOP

Notes

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