19-4446; Rev 1; 8/94

MAXIM

Quad Comparator with Programmable Threshold

MAX516

General Description

The MAX516 combines four low-power, programmable-threshold comparators on a single CMOS IC. Separate 8-bit digital-to-analog converters (DACs) drive the comparator inverting (-) inputs so that individual trip thresholds can be digitally set. All noninverting (+) comparator inputs are brought out as analog inputs (AIN0-AIN3). Each comparator output swings high when its analog input exceeds its digitally set threshold. All four DACs share a common reference input to optimize matching and eliminate external trims.

Digital inputs and comparator outputs are compatible with TTL and CMOS logic. A separate logic supply (V_{CC}) allows comparator output levels to be set independently of V_{DD}. The MAX516 operates conveniently from a single supply with V_{DD} tied to V_{CC}. Commercial, extended, and military temperature ranges are provided in 24-pin narrow DIP and wide SO packages.

Applications

Window Comparators

Power-Supply Monitors

Alarm Limit Detectors

Battery Chargers

Automated Test Equipment

Process Control

Features

- ♦ 4 Comparators and 4 DACs
- ♦ Digitally Set Threshold
- ♦ Monotonic Over Temperature
- ♦ Parallel Microprocessor Interface
- ♦ +5V to +15V Supply Operation

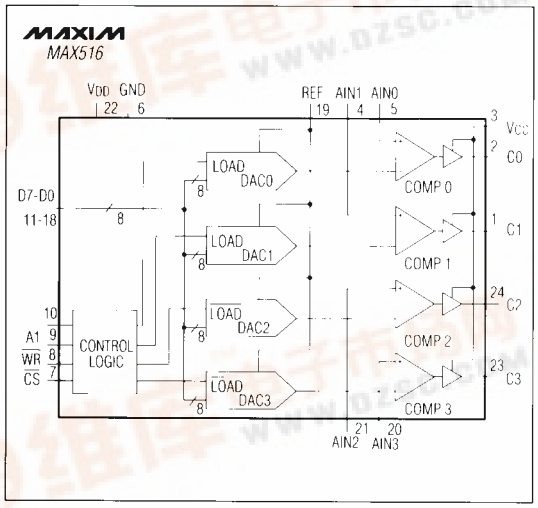
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX516ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX516BCNG	0°C to +70°C	24 Narrow Plastic DIP	±2
MAX516ACWG	0°C to +70°C	24 Wide SO	±1
MAX516BCWG	0°C to +70°C	24 Wide SO	±2
MAX516BC/D	0°C to +70°C	Dice*	±2
MAX516AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX516BENG	-40°C to +85°C	24 Narrow Plastic DIP	±2
MAX516AEWG	-40°C to +85°C	24 Wide SO	±1
MAX516BEWG	-40°C to +85°C	24 Wide SO	±2
MAX516AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1
MAX516BMRG	-55°C to +125°C	24 Narrow CERDIP**	±2

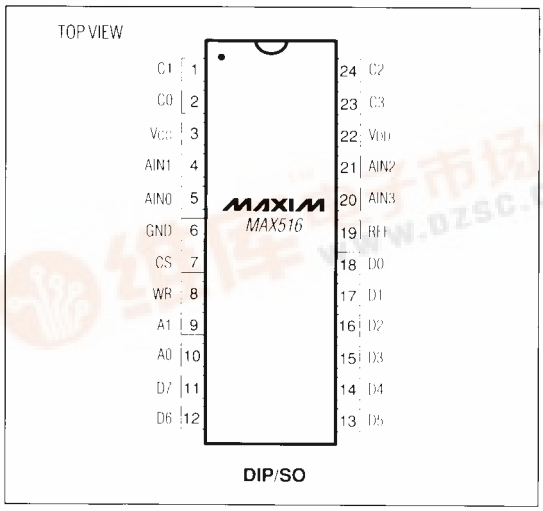
* Contact factory for dice specifications.

** Contact factory for availability and processing to MIL-STD-883

Functional Diagram



Pin Configuration



Quad Comparator with Programmable Threshold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V, +17V
V_{CC} to GND .....-0.3V, V_{DD} + 0.3V
V_{DD} to V_{CC} .....-0.3V, +17V
Digital Input Voltage to GND .....-0.3V, V_{DD} + 0.3V
REF to GND .....-0.3V, V_{DD} + 0.3V
Comparator Input to GND.....-0.3V, V_{DD} + 0.3V
C0–C3 to GND (Note 1) .....GND, V_{CC} + 0.3V
Continuous Current V_{CC} or GND 12mA

Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 8.7mW/°C above +70°C)..480mW
Wide SO (derate 11.8mW/°C above +70°C).....650mW
Narrow CERDIP (derate 12.5mW/°C above +70°C) 690mW
Operating Temperature Ranges:
MAX516_C__ .....0°C to +70°C
MAX516_E__.....-40°C to +85°C
MAX516_MRG .....-55°C to +125°C
Store Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec).....+300°C

Note 1: The outputs may be shorted to GND or V_{DD}, provided the package's power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Total Unadjusted Error	TUE		MAX516A			±1	LSB
			MAX516B			±2	
Relative Accuracy	INL		MAX516A			±0.5	LSB
			MAX516B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Full-Scale Error			MAX516A			±0.5	LSB
			MAX516B			±1	
Full-Scale Temperature Coefficient		V_{DD} = 15V, REF = 10V			±5		ppm/°C
Zero-Code Error		T_A = +25°C	MAX516A			±5	mV
		T_A = T_{MIN} to T_{MAX}	MAX516A			±10	
		T_A = +25°C	MAX516B			±10	
		T_A = T_{MIN} to T_{MAX}	MAX516B			±15	
Zero-Code Temperature Coefficient					±30		µV/°C
REFERENCE INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Reference Input Range	REF			1.25		V_{DD} -3.50	V
Reference Input Resistance	RREF	Worst-case code		3.0	4.5		kΩ
Reference Input Capacitance	CREF	Worst-case code (Note 2)			100	250	pF
COMPARATOR INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Comparator Input Range	V_{AIN}			0		V_{DD}	V
Comparator Input Bias Current	I_B	T_A = +25°C			50	300	nA
		T_A = T_{MIN} to T_{MAX}			100	400	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS D0–D7, $\overline{WR}$, $\overline{CS}$, (4.75 ≤ V_{DD} ≤ 16.5V)							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance	C_{IN}	(Note 2)	All except MAX516_MRG			10	pF
			MAX516_MRG			15	
DIGITAL OUTPUTS C0–C3 (V_{CC} = 5V)							
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA		V_{CC} - 1			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
DYNAMIC PERFORMANCE (1.25V ≤ REF ≤ V_{DD} - 3.5V, 0V ≤ AIN < V_{DD} -2V)							
Digital Input to Comparator Out Delay	t_{DCO}	(Note 3)			0.8	2.0	µs
Analog Input to Comparator Out Delay	t_{ACO}	(Note 4)			0.8	1.5	µs
TIMING CHARACTERISTICS							
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CS}			0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CH}			0			ns
Address to $\overline{WR}$ Setup Time	t_{AS}			50	30		ns
Address to $\overline{WR}$ Hold Time	t_{AH}			5	0		ns
Data Valid to $\overline{WR}$ Setup Time	t_{DS}			50	30		ns
Data Valid after $\overline{WR}$ Hold Time	t_{DH}			5	0		ns
$\overline{WRITE}$ Pulse Width	t_{WR}			120	50		ns
POWER SUPPLIES							
V_{DD} Range	V_{DD}			4.75		16.5	V
V_{CC} Range	V_{CC}			4.75		V_{DD} + 0.30	V
Positive Supply Current	I_{DD}	Logic inputs < V_{IL} or > V_{IH}				10	mA
Logic Supply	I_{CC}					10	µA

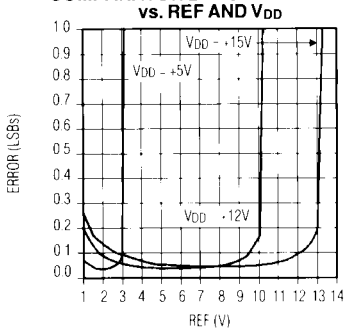
Note 2: Guaranteed by design. Not production tested.

Note 3: V_{DD} = 5.00V, differential comparator input voltage changes by 1.25V with 5mV overdrive. V_{IN} must be 3.5V less than V_{DD}, or longer propagation delays will result.

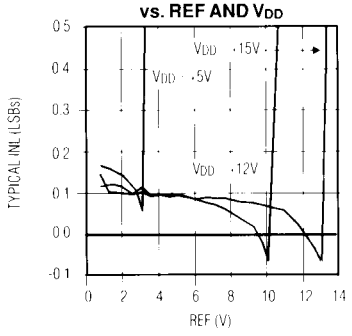
Note 4: Not tested, but guaranteed by correlation to t_{DCO}.

Typical Operating Characteristics

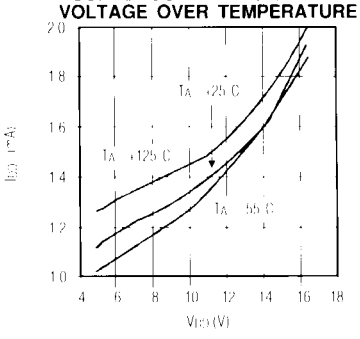
COMPARATOR ERROR AT CODE 255 vs. REF AND V_{DD}



RELATIVE ACCURACY vs. REF AND V_{DD}



SUPPLY CURRENT vs. SUPPLY VOLTAGE OVER TEMPERATURE



Quad Comparator with Programmable Threshold

Pin Description

PIN	NAME	FUNCTION
1, 2	C1, C0	Comparator Outputs
3	V_{CC}	Comparator Output Supply
4, 5	AIN1, AIN0	Comparator Analog Inputs
6	GND	Ground
7	CS	CHIP SELECT
8	WR	WRITE
9, 10	A1 , A0	DAC Address Inputs
11-18	D7-D0	DAC Data Inputs, 8 bits
19	REF	Reference Input
20, 21	AIN3, AIN2	Comparator Analog Inputs
22	V_{DD}	Positive Supply Voltage
23, 24	C3, C2	Comparator Outputs

Detailed Description

The MAX516 contains four analog comparators and four matched 8-bit digital-to-analog converters (DACs). The voltage output of each DAC is expressed in the equation:

$$V_{DAC} = REF \times N/256,$$

where N is the numerical equivalent of the 8-bit DAC input code (D0-D7). N ranges from 0 to 255 and may be set to a different level for each DAC (Table 1). The DAC output, V_{DAC}, does not appear on an output pin of the MAX516 but is instead compared to an analog input signal by one of four internal comparators (see *Functional Diagram*). A comparator output is high when AIN is more positive than the comparator's digitally set threshold.

Table 1. Comparator Threshold vs. DAC Input Code

DAC CODE MSB	DAC CODE LSB	COMPARATOR THRESHOLD
1111	1111	$+REF\left(\frac{255}{256}\right)$
1000	0001	$+REF\left(\frac{129}{256}\right)$
1000	0000	$+REF\left(\frac{128}{256}\right) = +\frac{REF}{2}$
0111	1111	$+REF\left(\frac{127}{256}\right)$
0000	0001	$+REF\left(\frac{1}{256}\right)$
0000	0000	0V

NOTE: $1LSB = (REF)(2^{-8}) = +REF\left(\frac{1}{256}\right)$

Reference Input

Comparator trip thresholds vary digitally between 0V and 1LSB below REF. All DACs share the same reference input.

The input impedance of REF is code dependent. The lowest impedance, typically 2kΩ, occurs when 0101 0101 (HEX 55) is loaded into D0-D7 on all four DACs. When 0000 0000 is loaded into all DACs, REF appears as an open circuit. Because the input resistance at REF is code dependent, the reference source should have an output impedance of no more than 4Ω to maintain linearity. Input capacitance at REF is also code dependent and typically varies between 100pF and 250pF.

Comparator Inputs

The "+" input of each comparator is brought out to AIN0-AIN3. Comparator input bias current is typically 100nA. Analog source resistances below 1.25kΩ generate less than 250µV of bias-current induced comparator offset error.

Digital Interface

The digital inputs (D0-D7, CS, WR) are both TTL and 5V CMOS logic compatible; however, the power-supply current, I_{DD}, depends on input logic levels. Supply currents will be highest with TTL levels (tested limits are with worst-case logic levels). Supply current is reduced when digital inputs are driven near GND and above 4V.

Address lines A0 and A1 select which DAC receives data from the input port. Because CS and WR are internally ORed, the write cycle begins only after both go low, but data is latched and transferred to a DAC when either input returns high. Figure 1 shows the input control logic, Table 2 lists DAC addresses, and Table 3 is the truth table for WR and CS. Figure 2 shows write-cyle timing.

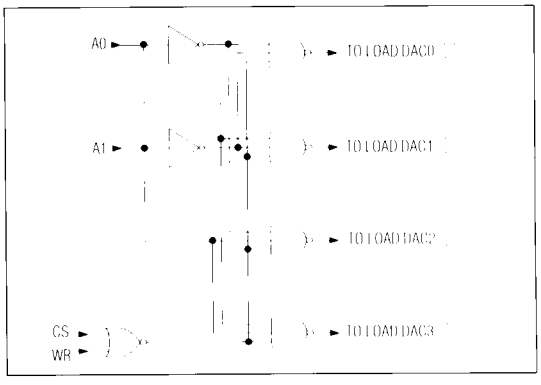


Figure 1. Input Control Logic

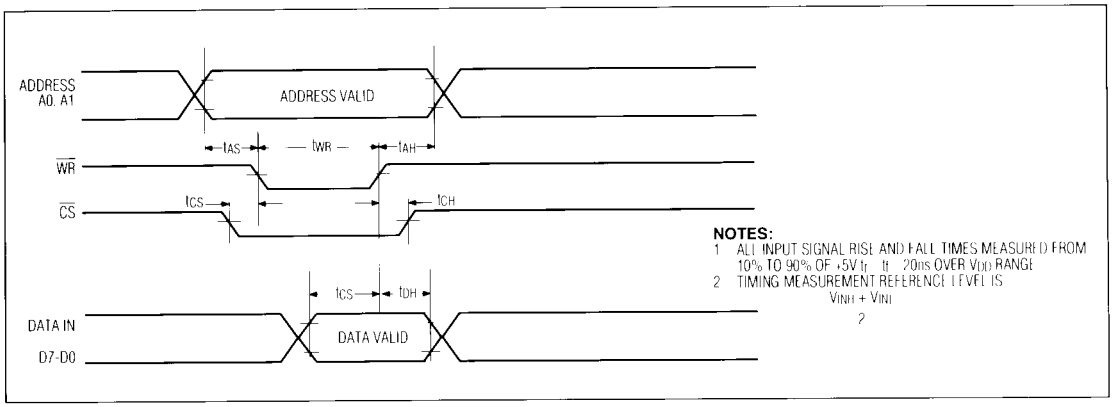


Figure 2. Write-Cycle Timing

Table 2. DAC Addressing

A1	A0	SELECTED DAC
0	0	DAC0 Input Register
0	1	DAC1 Input Register
1	0	DAC2 Input Register
1	1	DAC3 Input Register

Table 3. Write-Cycle Truth Table

CS	WR	FUNCTION
1	X	No operation. The MAX516 is deselected. Existing register contents remain unchanged.
0	0	DAC contents for selected address are loaded, but do not update the DAC until WR goes high.
0	↑	Latch D0-D7 into input register of the selected DAC on rising edge.

NOTES: X = Don't Care, ↑ = Rising Edge

Applications Information

Power-Supply and Reference Operating Ranges

The MAX516 is fully specified to operate with V_{DD} between +4.75V and +16.5V and is specified to operate with a reference input range of +1.25V to V_{DD} -3.5V.

The comparator output supply, V_{CC}, has a range of +4.5V to (V_{DD} + 0.3V). This allows the comparators' logic-high output levels to be set independently from V_{DD}. In most applications, simply connect V_{CC} and V_{DD} together. Comparator outputs typically swing within 200mV of the supply rails when loaded with CMOS logic inputs.

Hysteresis

When analog input signals are slow moving or contain noise, comparator outputs may "chatter" near the threshold point. Be sure that proper power-supply bypass capacitors are in place (see *Grounds and Bypassing* section), because supply current rises when an output switches.

Hysteresis may be added to any or all comparators to further resist oscillation during output transitions. This is accomplished with two resistors, as shown in Figure 3. When hysteresis is added, the threshold point will shift slightly as a result of the voltage divider formed by R1 and R2. The amount of shift is described below:

$$V_{TH} = V_T\left(\frac{R1}{R2} + 1\right)$$

$$V_{TL} = V_T\left(\frac{R1}{R2} + 1\right) - V_{CC}\left(\frac{R1}{R2}\right)$$

$$V_{HYST} = V_{TH} - V_{TL}$$

$$V_{HYST} = V_{CC}\left(\frac{R1}{R2}\right)$$

V_T is the threshold voltage set by the internal DAC with no hysteresis connected. V_{TH} is the shifted high-going threshold with hysteresis added. V_{TL} is the shifted low-going threshold with hysteresis. V_{HYST} is the total hysteresis and equals V_{TH} - V_{TL}. Note that V_{TL} and V_{HYST} change with V_{CC}. With V_{CC} = 5V, R1 = 1kΩ, and R2 = 200kΩ, V_{HYST} = 25mV. Even though R1 is relatively small, the impedance seen by the signal source is large: R1 + R2. However, if R1 is large, input bias current (400nA

Quad Comparator with Programmable Threshold

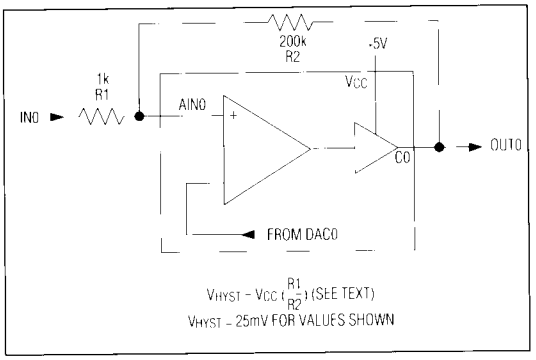


Figure 3. Adding Hysteresis to Any Comparator

max over temp.) may add offset error. 1kΩ x 400nA = 0.4mV offset error is due to bias current.

Grounds and Bypassing

Careful PC-board layout significantly minimizes crosstalk among the reference input, comparator outputs, and digital inputs. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Separate AIN0-AIN3 and REF from each other by running a ground trace between these pins.

Bypass both V_{DD} and V_{CC} to GND with a combination of a 0.1µF low ESR and a 4.7µF capacitor close to the device. If V_{DD} and V_{CC} are connected together, only one set of bypass capacitors is needed. If REF is not an AC input, it should be bypassed as well. Keep bypass-capacitor leads short for best supply noise rejection.

Applications

Threshold detection is often useful in automated test applications. Four individual thresholds can be independently altered under software control.

Figure 4 shows the connection for a hardware window comparison. DAC0 provides the upper trip point, DAC1 the lower trip point. The difference between the trip points is the window size. The AIN0 and AIN1 inputs are tied together. One logic output is inverted and then ORed with the noninverted comparator output. The window output goes high when the analog input sits between the thresholds set by DAC0 and DAC1. The external logic in Figure 4 can also be simulated in software, or use a single comparator to perform a window comparison by loading two threshold limits in succession and noting the comparator results of each (Figure 5).

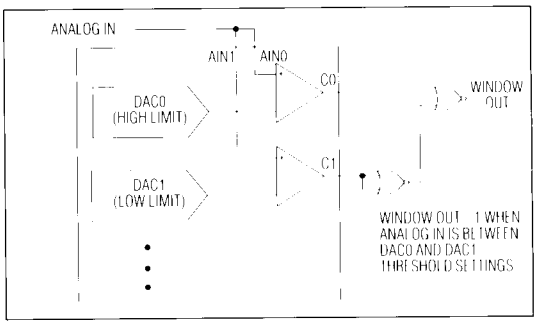


Figure 4. Window Comparison

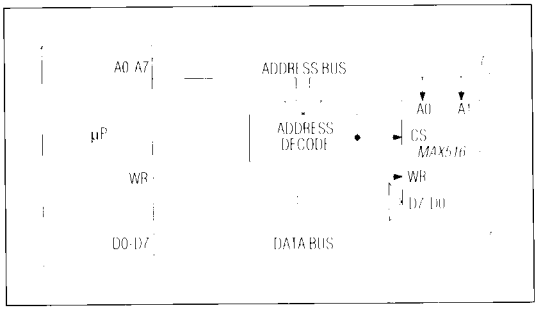
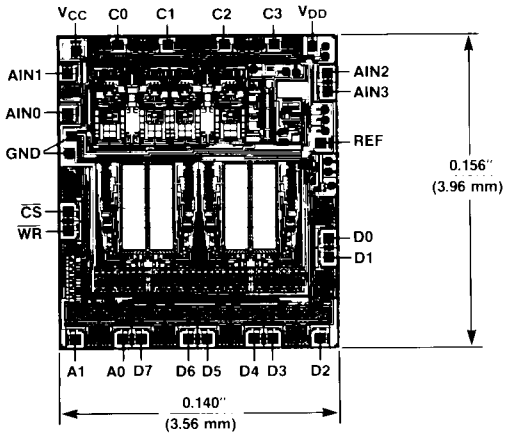
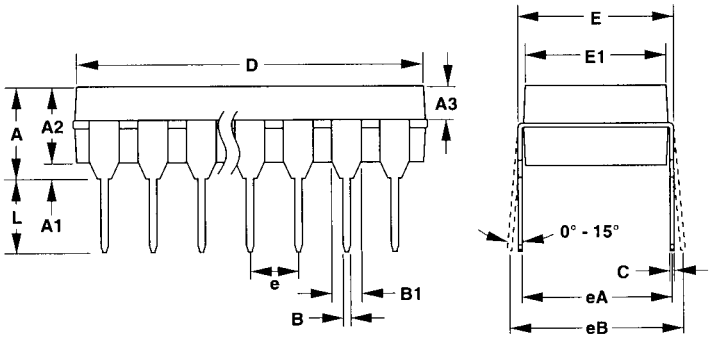


Figure 5. Microprocessor Interface

Chip Topography



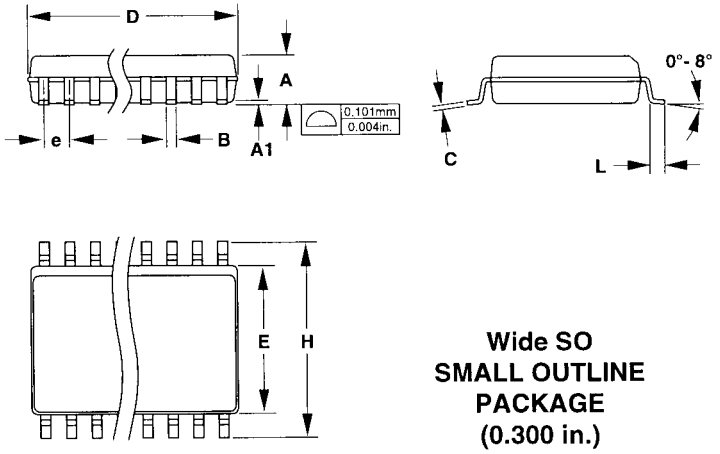
NOTE: Substrate connected to V_{DD}.



Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.348	0.390	8.84	9.91
D	14	0.735	0.765	18.67	19.43
D	16	0.745	0.765	18.92	19.43
D	18	0.885	0.915	22.48	23.24
D	20	1.015	1.045	25.78	26.54
D	24	1.14	1.265	28.96	32.13



Wide SO
SMALL OUTLINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

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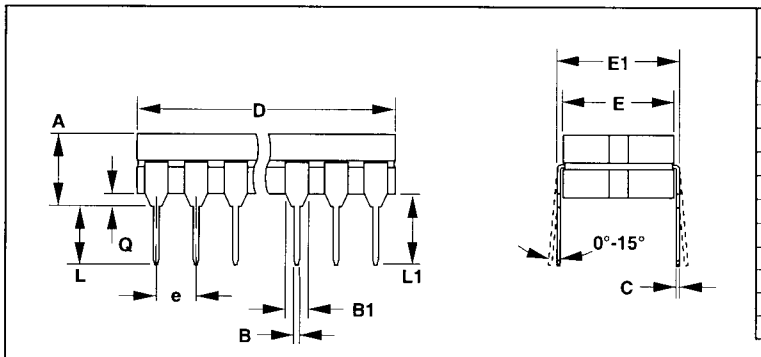
Quad Comparator with Programmable Threshold



CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51