3-A OUTPUT TRACKING/TERMINATION SYNCHRONOUS PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- Tracks Externally Applied Reference Voltage
- 60-mΩ MOSFET Switches for High Efficiency at 3-A Continuous Output Source or Sink Current
- 6% to 90% V_I Output Tracking Range
- Wide PWM Frequency: Fixed 350 kHz or Adjustable 280 kHz to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Total Cost

APPLICATIONS

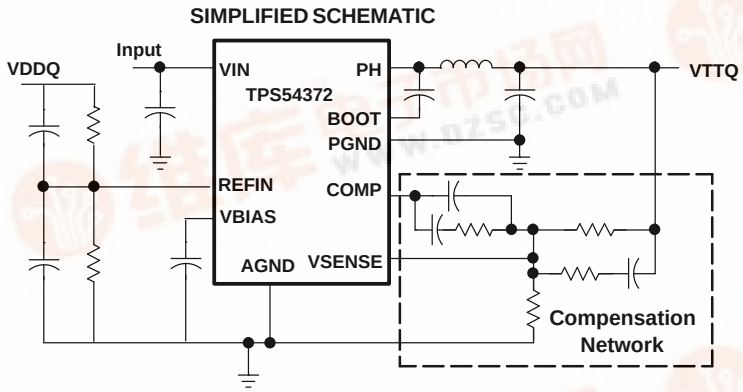
- DDR Memory Termination Voltage
- Active Termination of GTL and SSTL High-Speed Logic Families
- DAC Controlled, High-Current Output Stage
- Precision Point-of-Load Power Supply

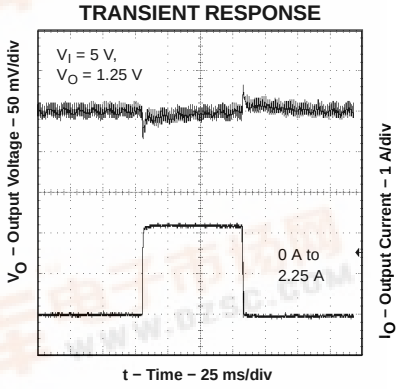
DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54372 low-input voltage, high-output current, synchronous-buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a status output to indicate valid operating conditions.

The TPS54372 is available in a thermally enhanced 20-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

SIMPLIFIED SCHEMATIC





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	REFIN VOLTAGE	PACKAGE	PART NUMBER(2)
-40°C to 85°C	0.2 V to 1.75 V	Plastic HTSSOP (PWP)	TPS54372PWP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54372PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS54372	UNITS
Input voltage range, V_I	VIN, ENA	–0.3 to 7	V
	RT	–0.3 to 6	
	VSENSE, REFIN	–0.3 to 4	
	BOOT	–0.3 to 17	
Output voltage range, V_O	VBIAS, COMP, STATUS	–0.3 to 7	V
	PH	–0.6 to 6	
Source current, I_O	PH	Internally limited	
	COMP, VBIAS	6	mA
Sink current, I_S	PH	6	A
	COMP	6	mA
	ENA, STATUS	10	
Voltage differential	AGND to PGND	±0.3	V
Operating virtual junction temperature range, T_J		–40 to 125	°C
Storage temperature, T_{stg}		–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I	3		6	V
Operating junction temperature, T_J	–40		125	°C

DISSIPATION RATINGS (1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
20-Pin PWP with solder	26.0°C/W	3.85 W (3)	2.11 W	1.54 W
20-Pin PWP without solder	57.5°C/W	1.73 W	0.96 W	0.69 W

(1) For more information on the PWP package, see TI technical brief, literature number SLMA002.
(2) Test board conditions:
  a. 3-inch x 3-inch, 4 layers, thickness: 0.062-inch
  b. 1.5-oz. copper traces located on the top of the PCB
  c. 1.5-oz. copper ground plane on the bottom of the PCB
  d. Ten thermal vias (see *Recommended Land Pattern* in applications section of this data sheet)
(3) Maximum power dissipation may be limited by overcurrent protection.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
VIN	Input voltage range		3.0		6.0	V
$I_{(Q)}$	Quiescent current	f_s = 350 kHz, RT open, PH pin open		6.2	9.60	mA
		f_s = 500 kHz, RT = 100 kΩ, PH pin open		8.4	12.8	
		Shutdown, ENA = 0 V		1	1.4	
UNDERVOLTAGE LOCKOUT						
	Start threshold voltage, UVLO			2.95	3.0	V
	Stop threshold voltage, UVLO		2.70	2.80		V
	Hysteresis voltage, UVLO		0.14	0.16		V
	Rising and falling edge deglitch, UVLO (1)			2.5		µs
BIAS VOLTAGE						
	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	V
	Output current, VBIAS (2)				100	µA
REGULATION						
	Line regulation (1)(3)	I_L = 1.5 A, f_s = 350 kHz, T_J = 85°C		0.07		%/V
	Load regulation (1)(3)	I_L = 0 A to 3 A, f_s = 350 kHz, T_J = 85°C		0.03		%/A
OSCILLATOR						
	Internally set free-running frequency	RT open	280	350	420	kHz
	Externally set free-running frequency range	RT = 180 kΩ (1% resistor to AGND) (1)	252	280	308	kHz
		RT = 100 kΩ (1% resistor to AGND)	460	500	540	
		RT = 68 kΩ (1% resistor to AGND) (1)	663	700	762	
	Ramp valley (1)			0.75		V
	Ramp amplitude (peak-to-peak) (1)			1		V
	Minimum controllable on time (1)				200	ns
	Maximum duty cycle (1)		90%			
ERROR AMPLIFIER						
	Error amplifier open-loop voltage gain	1 kΩ COMP to AGND (1)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND (1)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO (1)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP (1)		1.0	1.4		V/µs

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 8

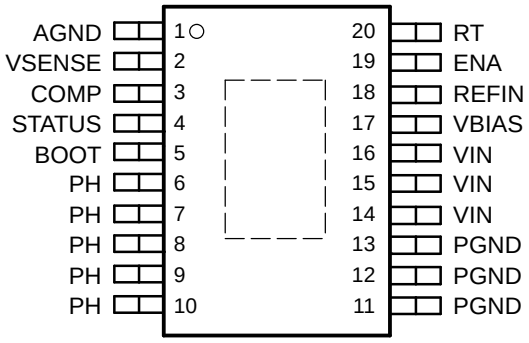
ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding dead time)	10-mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, ENA		0.82	1.20	1.40	V
	Enable hysteresis voltage, ENA(1)			0.03		V
	Falling edge deglitch, ENA(1)			2.5		µs
	Internal slow-start time		2.6	3.35	4.1	ms
STATUS						
	Output saturation voltage, STATUS	I_{sink} = 2.5 mA		0.18	0.30	V
	Leakage current, STATUS	V_I= 3.6 V			1	µA
CURRENT LIMIT						
	Current limit	V_I = 3 V(1)	4	6.5		A
		V_I= 6 V (1)	4.5	7.5		
	Current limit leading edge blanking time(1)			100		ns
	Current limit total response time(4)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point(4)		135	150	165	°C
	Thermal shutdown hysteresis(4)			10		°C
OUTPUT POWER MOSFETs						
$r_{DS(on)}$	Power MOSFET switches	V_I = 6 V(5)		59	88	mΩ
		V_I = 3 V(5)		85	136	

(4) Specified by design
(5) Matched MOSFETs low-side $r_{DS(on)}$, and high-side $r_{DS(on)}$ production tested.

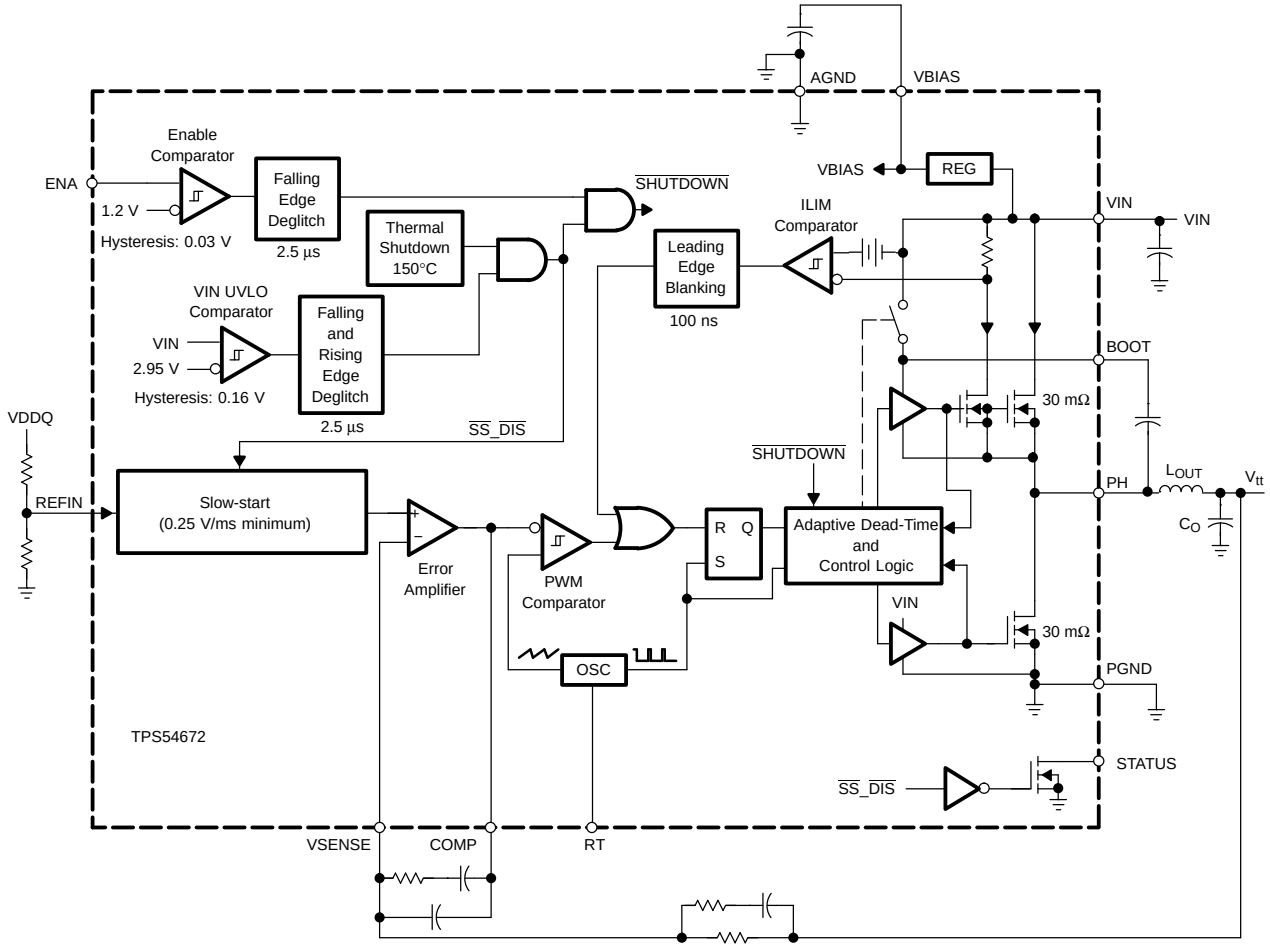
HTTSOP PowerPAD
(TOP VIEW)



Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. Connect PowerPAD connection to AGND.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
ENA	19	Enable input. Logic high enables oscillator, PWM control and MOSFET driver circuits. Logic low disables operation and places device in a low quiescent current state.
PGND	11-13	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single-point connection to AGND is recommended.
PH	6-10	Phase input/output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
RT	20	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_s.
REFIN	18	External reference input. High impedance input to slow-start and error amplifier circuits.
STATUS	4	Open-drain output. Asserted low when VIN < UVLO, VBIAS and internal reference are not settled or the internal shutdown signal is active. Otherwise STATUS is high.
VBIAS	17	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
V_{IN}	14-16	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high-quality, low-ESR 10-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

INTERNAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

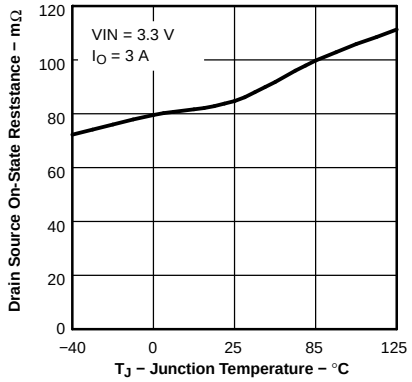


Figure 1.

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

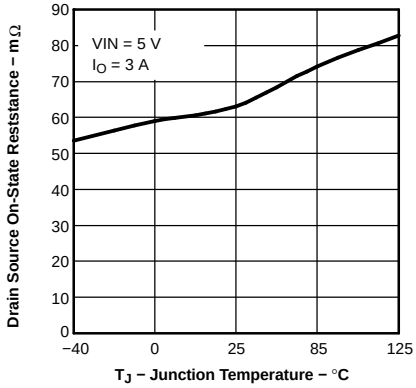


Figure 2.

INTERNALLY SET OCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

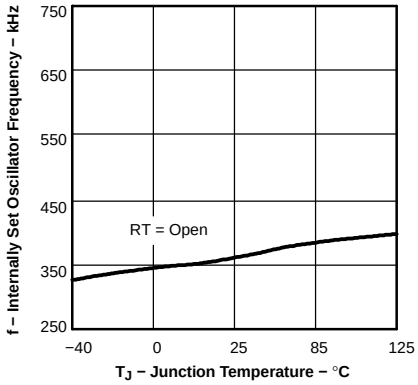


Figure 3.

EXTERNALLY SET OCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

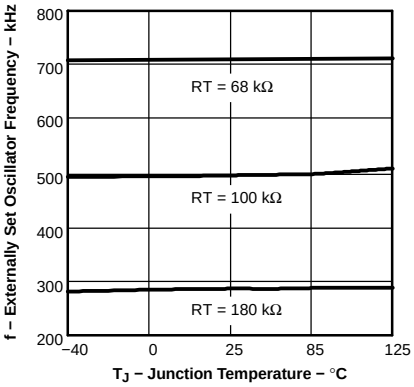


Figure 4.

DEVICE POWER LOSSES vs LOAD CURRENT

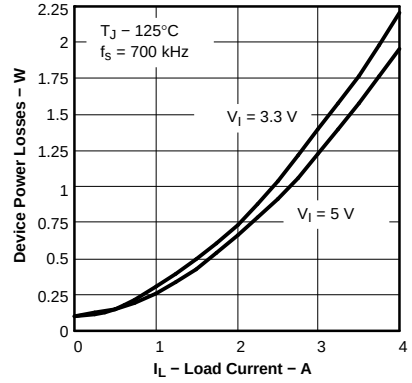


Figure 5.

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

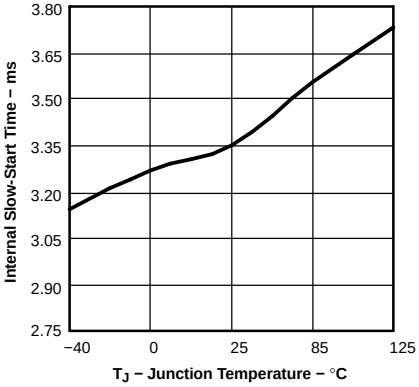


Figure 6.

ERROR AMPLIFIER OPEN-LOOP RESPONSE

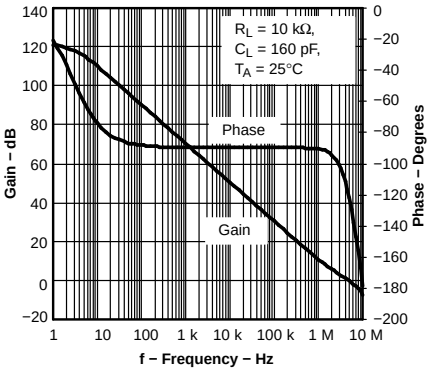


Figure 7.

APPLICATION INFORMATION

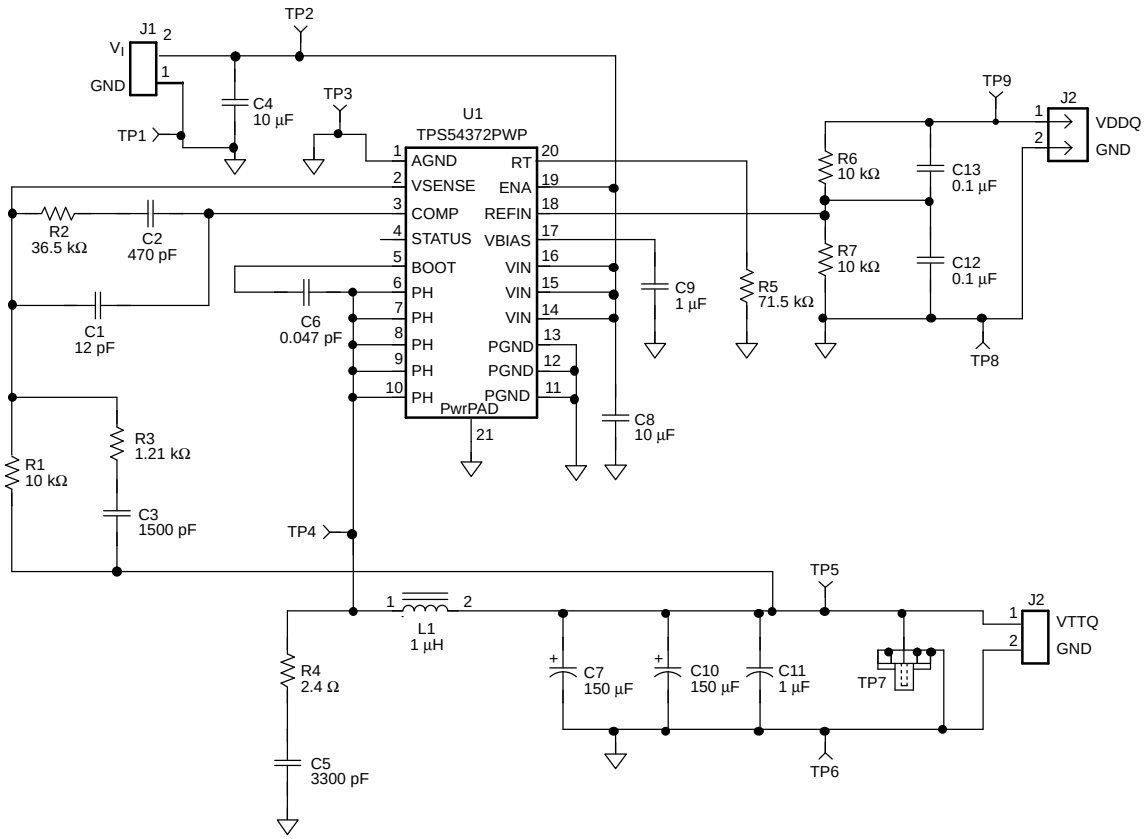


Figure 8. Application Circuit

TYPICAL CIRCUIT

Figure 8 shows the schematic diagram for a typical TPS54372 application. The TPS54372 (U1) can provide up to 3 A of output current at a nominal output voltage of one half of V_{DDQ} (typically 1.25 V). For proper operation, the PowerPAD underneath the integrated circuit TPS54372 is soldered directly to the printed-circuit board.

COMPONENT SELECTION

The values for the components used in this design example were selected for good transient response and small PCB area. Special polymer capacitors are used in the output filter circuit. A small size, small value output inductor is also used. Compensation network components are chosen to maximize closed-loop bandwidth and provide good transient response characteristics. Additional design information is available at www.ti.com.

INPUT VOLTAGE

The input voltage is a nominal 3.3 or 5.0 Vdc. The input filter (C4) is a 10-µF ceramic capacitor (Taiyo Yuden). Capacitor C8, a 10-µF ceramic capacitor (Taiyo Yuden) that provides high-frequency decoupling of the TPS54372 from the input supply, must be located as close as possible to the device. Ripple current is carried in both C4 and C8, and the return path to PGND should avoid the current circulating in the output capacitors C7, C10, and C11.

FEEDBACK CIRCUIT

The values for these components are selected to provide fast transient response times. Components R1, R2, R3, C1, C2, and C3 form the loop compensation network for the circuit. For this design, a Type-3 topology is used. The transfer function of the feedback network is chosen to provide maximum closed-loop gain available with open-loop characteristics of the internal error amplifier. Closed-loop crossover frequency is typically between 80 kHz and 125 kHz for input from 3 V to 6 V.

OPERATING FREQUENCY

In the application circuit, RT is grounded through a 71.5-kΩ resistor to select the operating frequency of 700 kHz. To set a different frequency, place a 68-kΩ to 180-kΩ resistor between RT (pin 20) and analog ground or leave RT floating to select the default of 350 kHz. The resistance can be approximated using the following equation:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ [\text{k}\Omega]$$

OUTPUT FILTER

The output filter is composed of a 1.0-µH inductor and two 150-µF capacitors. The inductor is a low dc resistance (0.010 Ω) type, Vishay IHLP-2525CZ-01 1.0-µH, 8.5-A rated dc output. The capacitors used are 150-µF, 6.3-V special polymer types.

PCB LAYOUT

Figure 9 shows a generalized PCB layout guide for the TPS54372.

The VIN pins should be connected together on the printed-circuit board (PCB) and bypassed with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54372 ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R- or X7R-grade dielectric, and the optimum placement is closest to the VIN pins and the PGND pins.

The TPS54372 has two internal grounds (analog and power). Inside the TPS54372, the analog ground ties to all of the noise-sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54372, particularly at higher output currents. Ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground traces are recommended. There should be an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. The only components that should tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the TPS54372. Use a separate wide trace for the analog ground signal path. This analog ground should be used for the voltage set-point divider, timing resistor RT, and bias capacitor grounds. Connect this trace directly to AGND (pin 1).

The PH pins should be tied together and routed to the output inductor. Because the PH connection is the switching node, the inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. Connect the output filter capacitor(s) as shown, between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout, and PGND as small as practical.

Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pinout, they have to be routed somewhat close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If an RT resistor is used, connect it to this trace as well.

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3-inch by 3-inch plane of 1-ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3-A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013-inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018 inch. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

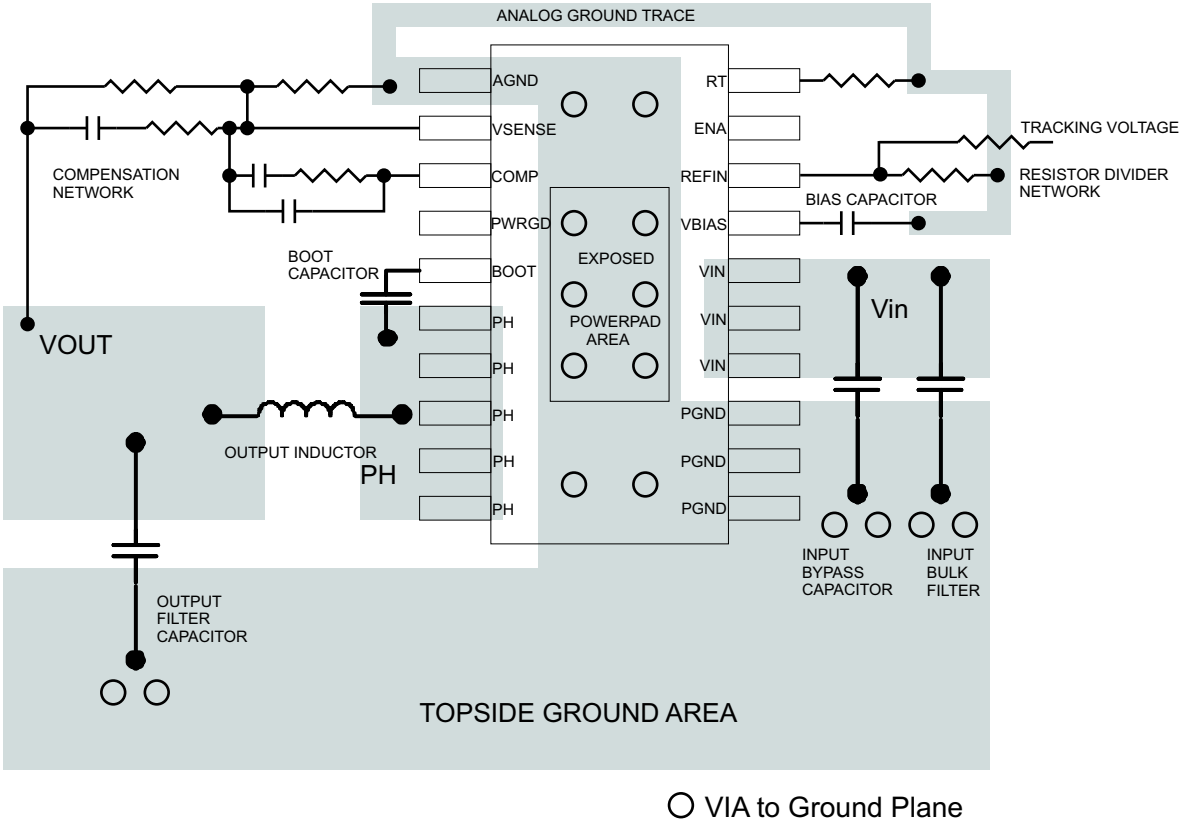


Figure 9. PCB Layout for 20-Pin PWP PowerPAD

PERFORMANCE GRAPHS

EFFICIENCY VS OUTPUT CURRENT

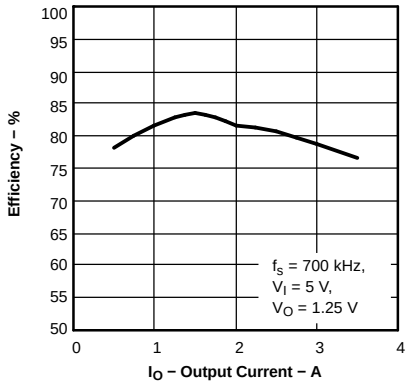


Figure 10.

LOAD REGULATION VS OUTPUT CURRENT

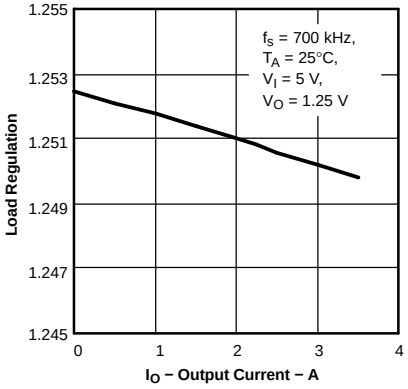


Figure 11.

PERFORMANCE GRAPHS (continued)

LINE REGULATION vs INPUT VOLTAGE

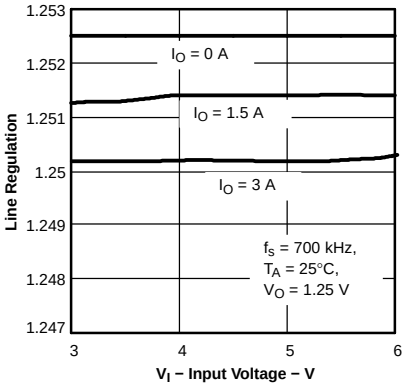


Figure 12.

OUTPUT RIPPLE VOLTAGE

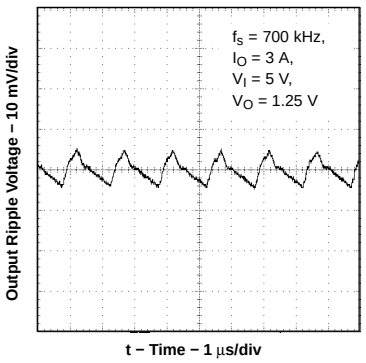


Figure 13.

TRANSIENT RESPONSE

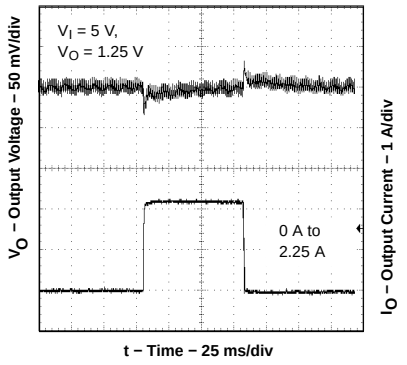


Figure 14.

SLOW-START TIMING

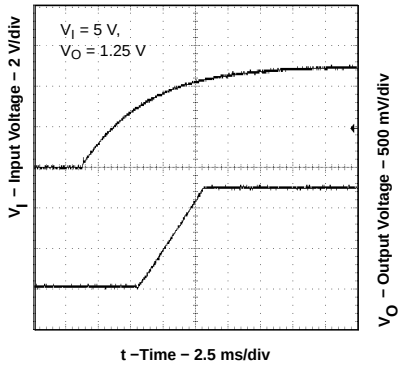


Figure 15.

SOURCE-SINK TRANSIENT RESPONSE

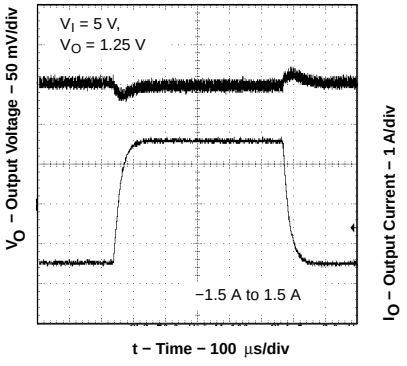
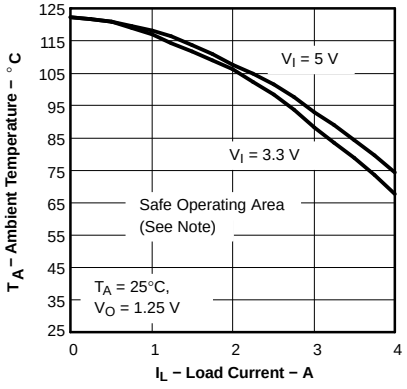


Figure 16.

AMBIENT TEMPERATURE vs LOAD CURRENT(1)



(1) Safe operating area is applicable to the test board conditions listed in the dissipation rating table section of this data sheet.

Figure 17.

DETAILED DESCRIPTION

UNDERVOLTAGE LOCKOUT (UVLO)

The TPS54372 incorporates an undervoltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO comparator. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

ENABLE (ENA)

The enable pin, ENA, provides a digital control to enable or disable (shutdown) the TPS54372. An input voltage of 1.4 V or greater ensures the TPS54372 is enabled. An input of 0.82 V or less ensures the device operation is disabled. These are not standard logic thresholds, even though they are compatible with TTL outputs.

When ENA is low, the oscillator, slow-start, PWM control and MOSFET drivers are disabled and held in an initial state ready for device start-up. On an ENA transition from low to high, device start-up begins with the output starting from 0 V.

SLOW-START

The slow-start circuit provides start-up slope control of the output voltage to limit in-rush currents. The nominal internal slow-start rate is 0.25 V/ms with the minimum rate being 0.35 V/ms. When the voltage on REFIN rises faster than the internal slope or is present when device operation is enabled, the output rises at the internal rate. If the reference voltage on REFIN rises more slowly, then the output rises at approximately the same rate as REFIN.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R- or X5R-grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

VOLTAGE REFERENCE

The REFIN pin provides an input for a user supplied tracking voltage. Typically this input is one half of V_{DDQ}. The input range for this external reference is 0.2 V to 1.75 V. Above this level, the internal bandgap reference overrides the externally supplied reference voltage.

OSCILLATOR AND PWM RAMP

The oscillator frequency can be set to an internally fixed value of 350 kHz by leaving the RT pin unconnected (floating). If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor to the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ \text{[kHz]}$$

The following table summarizes the frequency selection configurations:

Frequency Selection

SWITCHING FREQUENCY	RT PIN
350 kHz, internally set	Float
Externally set 280 kHz to 700 kHz	R = 180 kΩ to 68 kΩ

ERROR AMPLIFIER

The high-performance, wide bandwidth, voltage error amplifier sets the TPS54372 apart from most dc/dc converters. The user has a wide range of output L and C filter components to suit the particular application needs. Type-2 or type-3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the

error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54372 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V, while the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V. The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω. bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents false tripping of the current limit when the high-side switch is turning on. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip-point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down on reaching the thermal limit trip-point. This sequence repeats until the fault condition is removed.

STATUS

The status pin is an open-drain output that indicates when internal conditions are sufficient for proper operation. STATUS can be coupled back to a system controller or monitor circuit to indicate that the termination or tracking regulator is ready for start-up. STATUS is high impedance when the TPS54372 is operating or ready to be enabled.

STATUS is active low if any of the following occur:

- VIN < UVLO threshold
- VBIAS or internal reference have not settled.
- Thermal shutdown is active.

THERMAL PAD MECHANICAL DATA

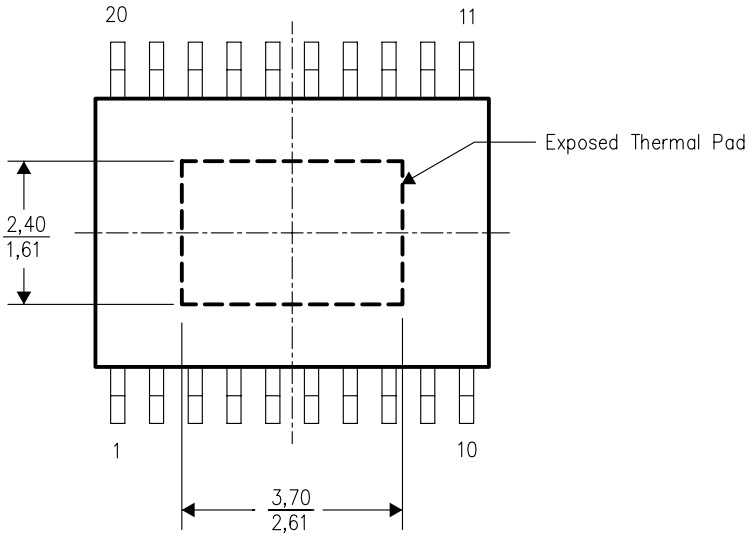
PWP (R–PDSO–G20)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGE OPTION ADDENDUM

30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS54372PWP	ACTIVE	HTSSOP	PWP	20	70	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS54372PWPR	ACTIVE	HTSSOP	PWP	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS54372PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	TBD	Call TI	Call TI

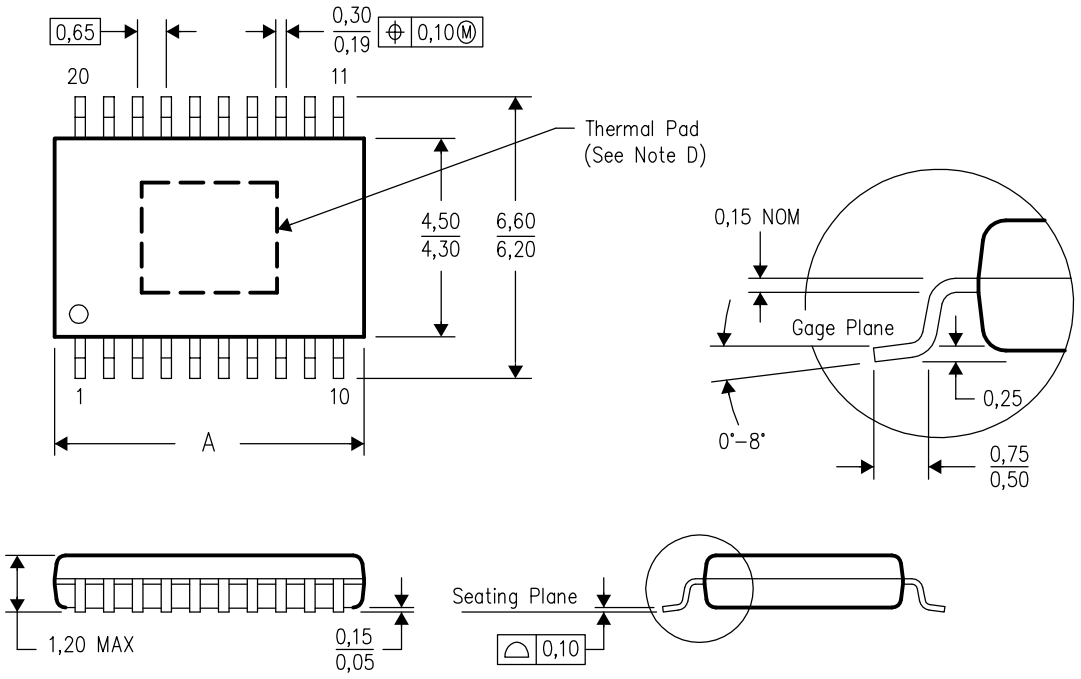
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

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