



**ANALOG
DEVICES**

Precision Micropower Low Noise CMOS Rail-to-Rail Input/Output Operational Amplifiers

AD8603/AD8607/AD8609

FEATURES

- Low offset voltage: 50 μ V max
- Low input bias current: 1 pA max
- Single-supply operation: 1.8 V to 5 V
- Low noise: 22 nV/ $\sqrt{\text{Hz}}$
- Micropower: 50 μ A max
- Low distortion
- No phase reversal
- Unity gain stable

APPLICATIONS

- Battery-powered instrumentation
- Multipole filters
- Sensors
- Low power ASIC input or output amplifiers

GENERAL DESCRIPTION

The AD8603/AD8607/AD8609 are, single/dual/quad micro-power rail-to-rail input and output amplifiers, respectively, that features very low offset voltage as well as low input voltage and current noise.

These amplifiers use a patented trimming technique that achieves superior precision without laser trimming. The parts are fully specified to operate from 1.8 V to 5.0 V single supply or from ± 0.9 V to ± 2.5 V dual supply. The combination of low offsets, low noise, very low input bias currents, and low power consumption make the AD8603/AD8607/AD8609 especially useful in portable and loop-powered instrumentation.

The ability to swing rail to rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in low power single-supply systems.

The AD8603 is available in a tiny 5-lead TSOT-23 package. The AD8607 is available in 8-lead MSOP and SOIC packages. The AD8609 is available in 14-lead TSSOP and SOIC packages.

PIN CONFIGURATIONS

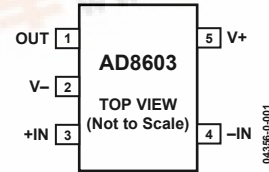


Figure 1. 5-Lead TSOT-23 (UJ Suffix)

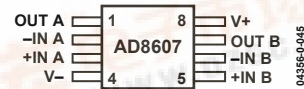


Figure 2. 8-Lead MSOP (RM Suffix)

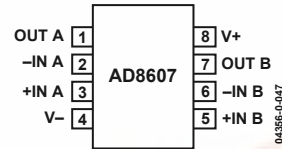


Figure 3. 8-Lead SOIC (R Suffix)

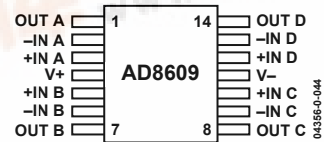


Figure 4. 14-Lead TSSOP (RU Suffix)

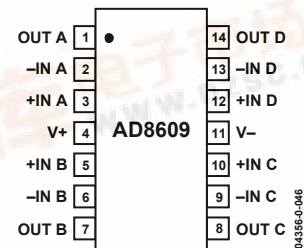


Figure 5. 14-Lead SOIC (R Suffix)



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REVISION HISTORY

10/03—Data Sheet Changed from Rev. 0 to Rev. A

Change	Page
Added AD8607 and AD8609 parts	Universal
Changes to Specifications	3
Changes to Figure 35.....	10
Added Figure 41.....	11

SPECIFICATIONS

Table 1. Electrical Characteristics @ $V_S = 5\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	$V_S = 3.3\text{ V}$ @ $V_{CM} = 0.5\text{ V}$ and 2.8 V		12	50	μV	
		$-0.3\text{ V} < V_{CM} < +5.2\text{ V}$		40	300	μV	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$, $-0.3\text{ V} < V_{CM} < +5.2\text{ V}$				700	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4.5	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2	1	pA	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				50	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				500	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.1	0.5	pA	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				50	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				250	pA
Input Voltage Range	IVR		-0.3		+5.2	V	
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 5\text{ V}$	85	100		dB	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80			dB	
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $0.5\text{ V} < V_O < 4.5\text{ V}$		400	1000	V/mV	
				250	450	V/mV	
Input Capacitance	C_{DIFF} C_{CM}			1.9		pF	
				2.5		pF	
OUTPUT CHARACTERISTICS							
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$	4.95	4.97		V	
		-40°C to $+125^\circ\text{C}$	4.9			V	
		$I_L = 10\text{ mA}$	4.65	4.97		V	
		-40°C to $+125^\circ\text{C}$	4.50			V	
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$		16	30	mV	
		-40°C to $+125^\circ\text{C}$			50	mV	
		$I_L = 10\text{ mA}$		160	250	mV	
		-40°C to $+125^\circ\text{C}$			330	mV	
Output Current	I_{OUT}		± 80			mA	
Closed-Loop Output Impedance	Z_{OUT}	$f = 10\text{ kHz}$, $A_V = 1$		36		Ω	
POWER SUPPLY							
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_S < 5\text{ V}$	80	100		dB	
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$		40	50	μA	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			60	μA	
DYNAMIC PERFORMANCE							
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ μs	
Settling Time 0.1%	t_S	$G = \pm 1$, 2 V Step		23		μs	
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$		400		kHz	
		$R_L = 10\text{ k}\Omega$		316		kHz	
Phase Margin	ϕ_O	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$		70		Degrees	
NOISE PERFORMANCE							
Peak-to-Peak Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		2.3	3.5	μV	
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 10\text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$	
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$	
Channel Separation	C_S	$f = 10\text{ kHz}$		-115		dB	
		$f = 100\text{ kHz}$		-110		dB	

AD8603/AD8607/AD8609

Table 2. Electrical Characteristics @ $V_S = 1.8\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	$V_S = 3.3\text{ V}$ @ $V_{CM} = 0.5\text{ V}$ and 2.8 V $-0.3\text{ V} < V_{CM} < +1.8\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$, $-0.3\text{ V} < V_{CM} < +1.8\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$, $-0.3\text{ V} < V_{CM} < +1.7\text{ V}$		12	50	μV	
				40	300	μV	
						500	μV
						700	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4.5	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA	
						50	pA
						500	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA	
						50	pA
						250	pA
Input Voltage Range	IVR		-0.3		+1.8	V	
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 1.8\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	80	98		dB	
			70			dB	
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $0.5\text{ V} < V_O < 4.5\text{ V}$		150	3000	V/mV	
				100	2000	V/mV	
Input Capacitance	C_{DIFF} C_{CM}			2.1		pF	
				3.8		pF	
OUTPUT CHARACTERISTICS							
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ -40°C to $+125^\circ\text{C}$	1.65 1.6	1.72		V V	
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ -40°C to $+125^\circ\text{C}$		38	60	mV mV	
Output Current	I_{OUT}			± 7		mA	
Closed-Loop Output Impedance	Z_{OUT}	$f = 10\text{ kHz}$, $A_V = 1$		36		Ω	
POWER SUPPLY							
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_S < 5\text{ V}$	80	100		dB	
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		40	50	μA	
					60	μA	
DYNAMIC PERFORMANCE							
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ μs	
Settling Time 0.1%	t_s	$G = \pm 1$, 1 V Step		9.2		μs	
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$		385		kHz	
				316		kHz	
Phase Margin	\emptyset_O	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$		70		Degrees	
NOISE PERFORMANCE							
Peak-to-Peak Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		2.3	3.5	μV	
Voltage Noise Density	e_n	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$	
				22		$\text{nV}/\sqrt{\text{Hz}}$	
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$	
Channel Separation	C_s	$f = 10\text{ kHz}$ $f = 100\text{ kHz}$		-115		dB	
				-110		dB	

ABSOLUTE MAXIMUM RATINGS

Table 3. AD8603/AD8607/AD8609 Stress Ratings^{1,2}

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	± 6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	
All Packages	-65°C to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 Sec)	300°C
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Junction Temperature Range	
All Packages	-65°C to $+150^{\circ}\text{C}$

Table 4. Package Characteristics

Package Type	θ_{JA} ³	θ_{JC}	Unit
5-Lead TSOT-23 (UJ)	207	61	$^{\circ}\text{C}/\text{W}$
8-Lead MSOP (RM)	210	45	$^{\circ}\text{C}/\text{W}$
8-Lead SOIC (R)	158	43	$^{\circ}\text{C}/\text{W}$
14-Lead SOIC (R)	120	36	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU)	180	35	$^{\circ}\text{C}/\text{W}$

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

² Absolute maximum ratings apply at 25°C , unless otherwise noted.

³ θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these parts feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

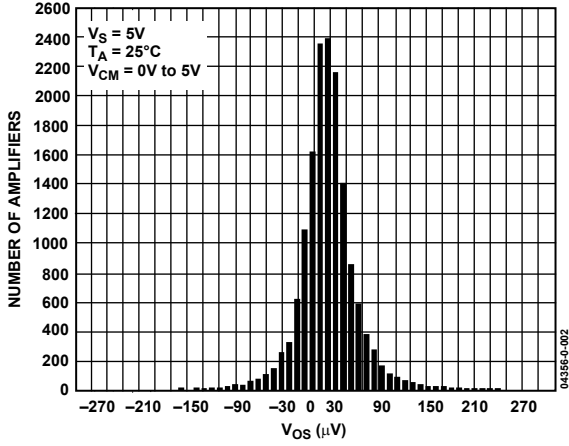


Figure 6. Input Offset Voltage Distribution

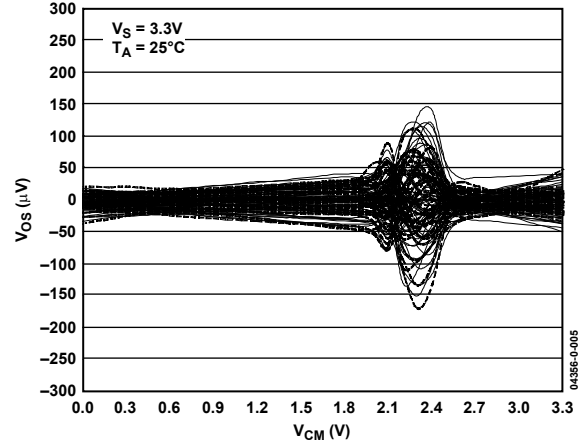


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

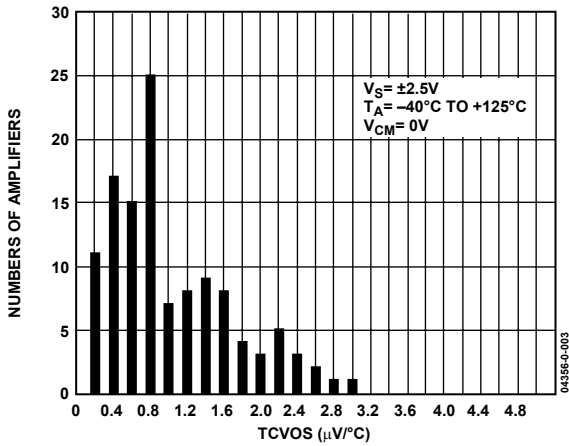


Figure 7. Input Offset Voltage Drift Distribution

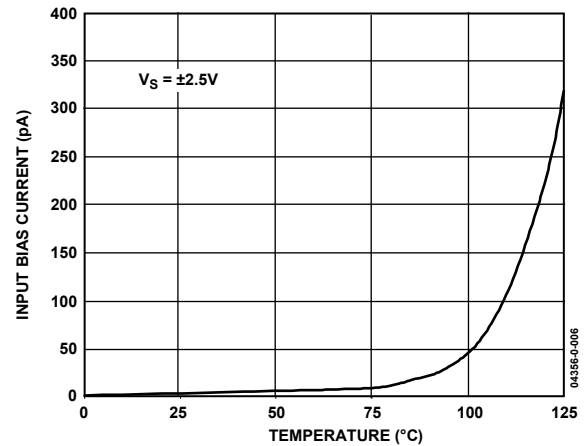


Figure 10. Input Bias vs. Temperature

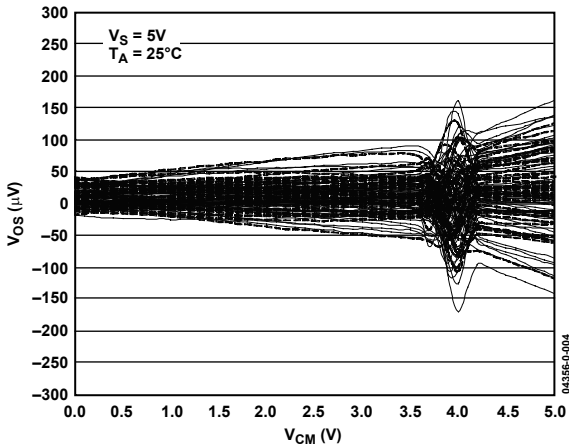


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

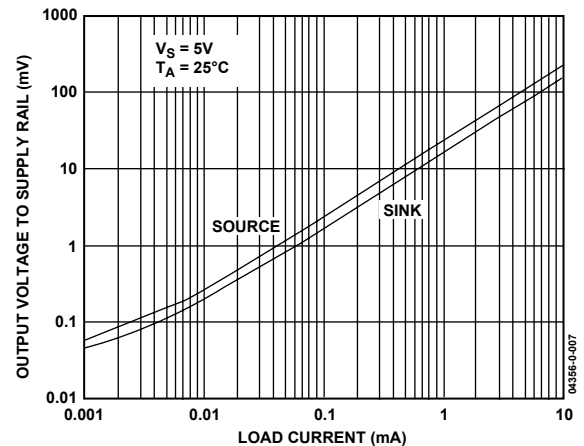


Figure 11. Output Voltage to Supply Rail vs. Load Current

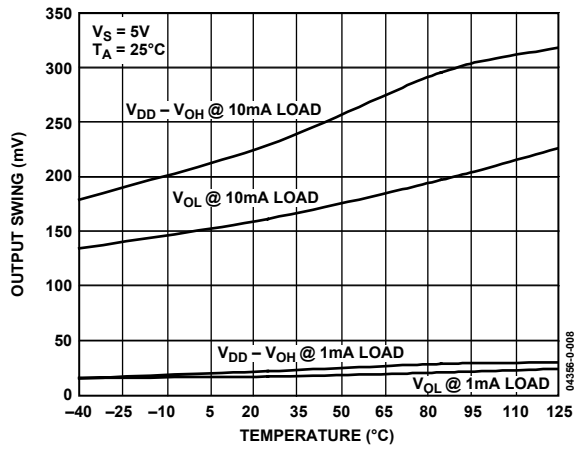


Figure 12. Output Voltage Swing vs. Temperature

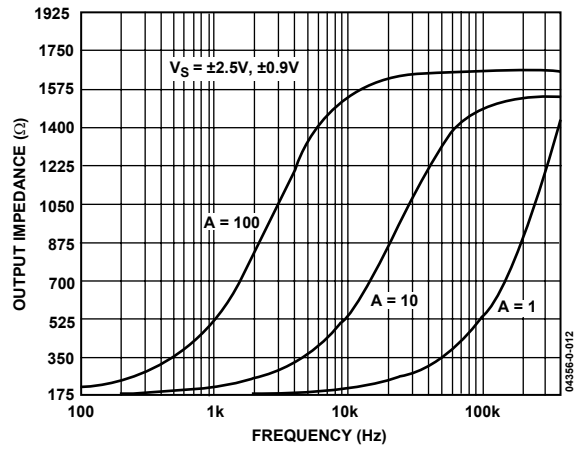


Figure 15. Output Impedance vs. Frequency

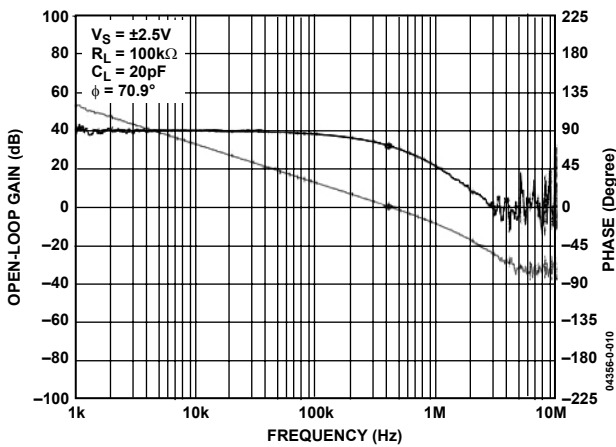


Figure 13. Open-Loop Gain and Phase vs. Frequency

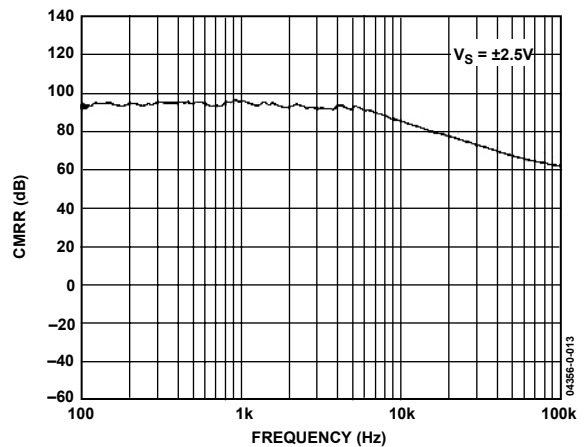


Figure 16. Common-Mode Rejection Ratio vs. Frequency

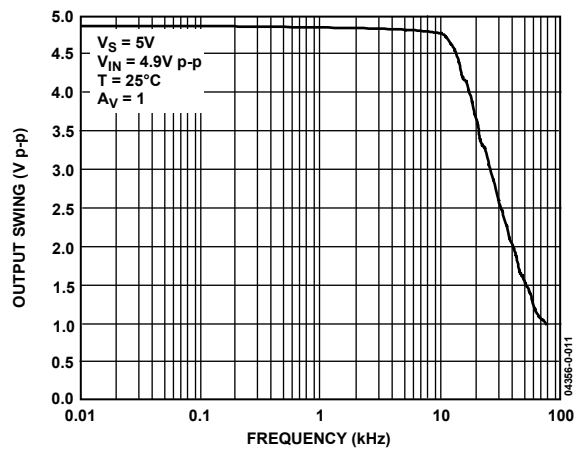


Figure 14. Closed-Loop Output Voltage Swing vs. Frequency

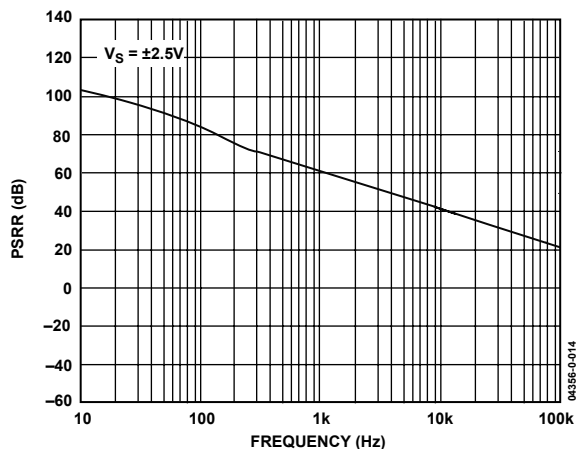


Figure 17. PSRR vs. Frequency

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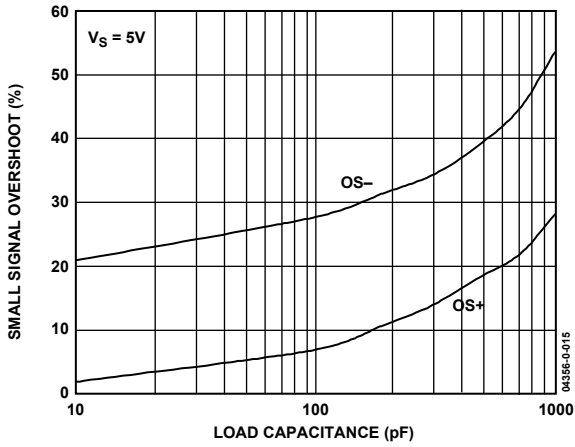


Figure 18. Small Signal Overshoot vs. Load Capacitance

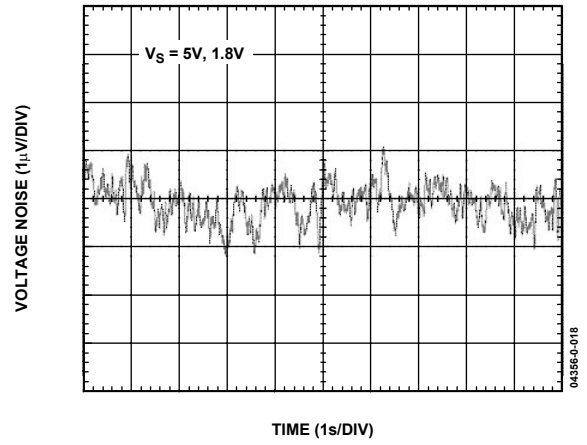


Figure 21. 0.1 Hz to 10 Hz Input Voltage Noise

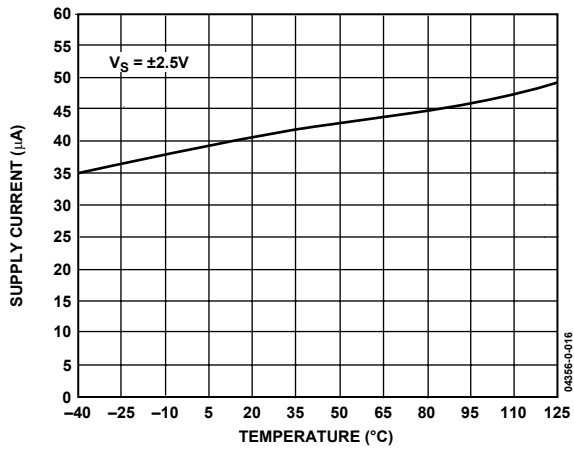


Figure 19. Supply Current vs. Temperature

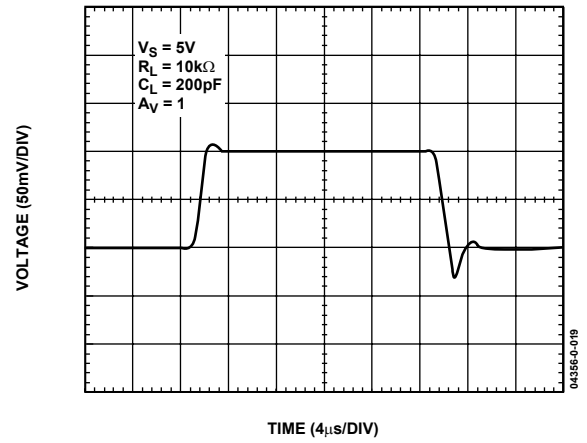


Figure 22. Small Signal Transient

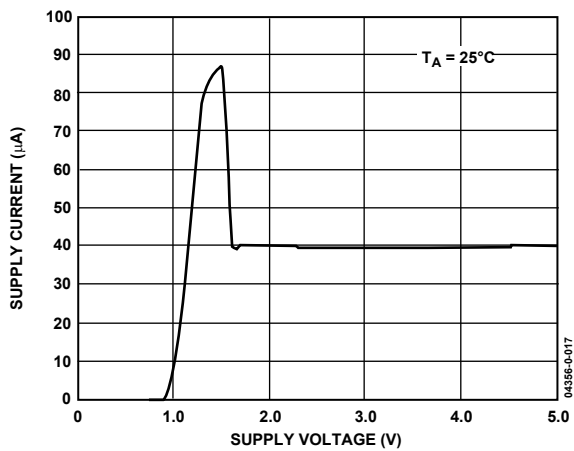


Figure 20. Supply Current vs. Supply Voltage

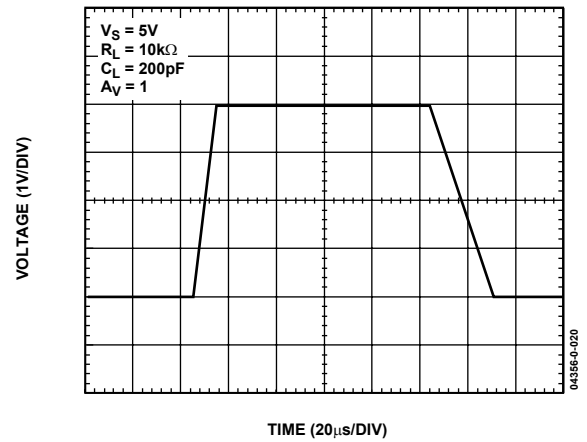


Figure 23. Large Signal Transient

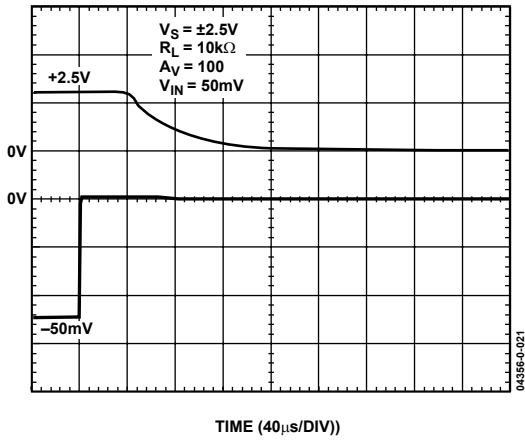


Figure 24. Negative Overload Recovery

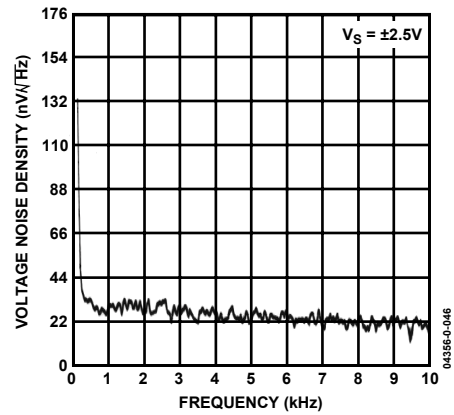


Figure 27. Voltage Noise Density vs. Frequency

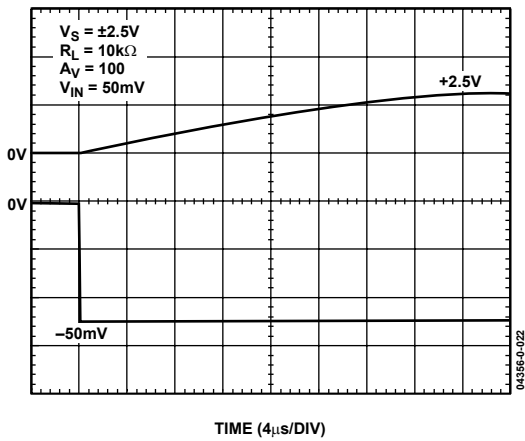


Figure 25. Positive Overload Recovery

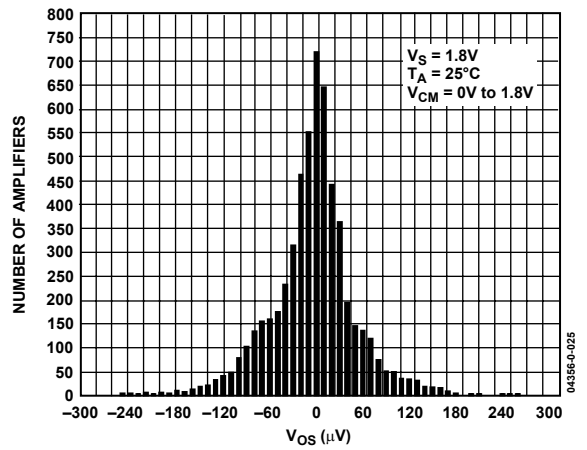


Figure 28. V_{OS} Distribution

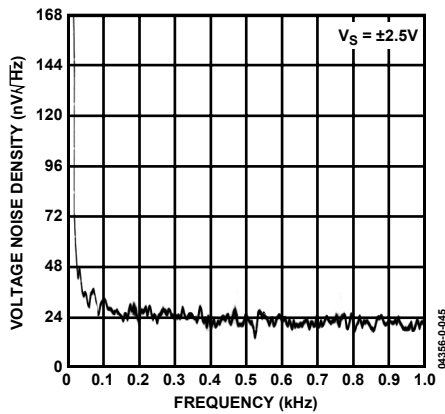


Figure 26. Voltage Noise Density vs. Frequency

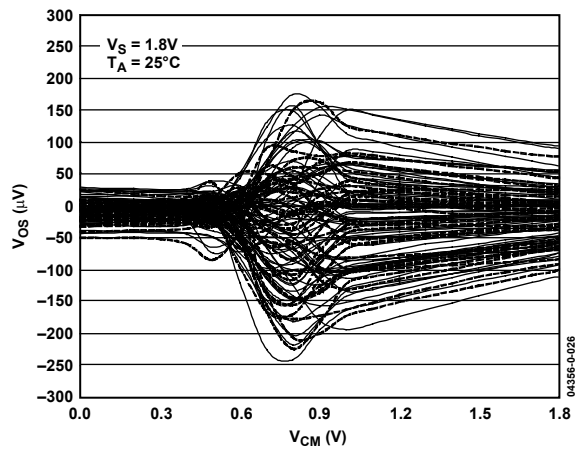


Figure 29. Input Offset Voltage vs. Common-Mode Voltage

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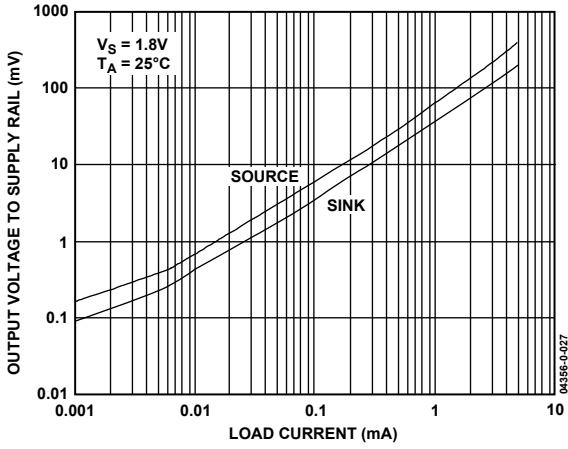


Figure 30. Output Voltage to Supply Rail vs. Load Current

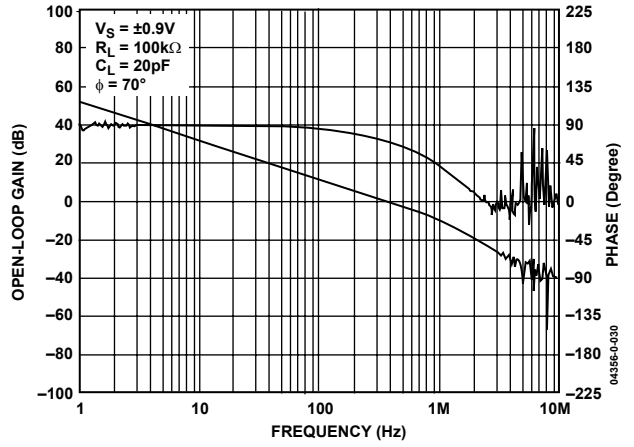


Figure 33. Open-Loop Gain and Phase vs. Frequency

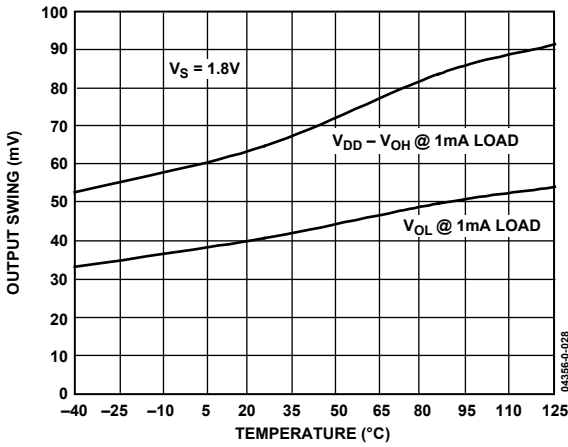


Figure 31. Output Voltage Swing vs. Temperature

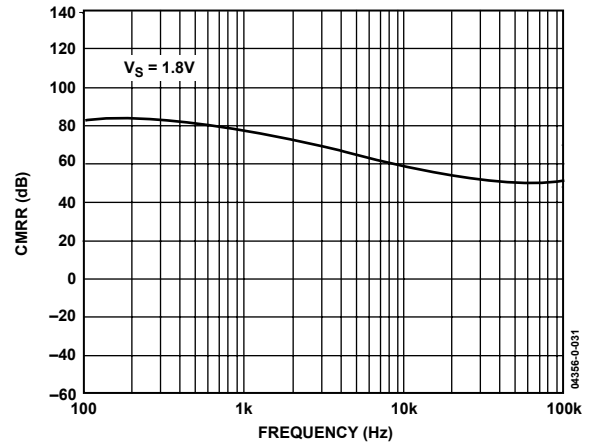


Figure 34. Common-Mode Rejection Ratio vs. Frequency

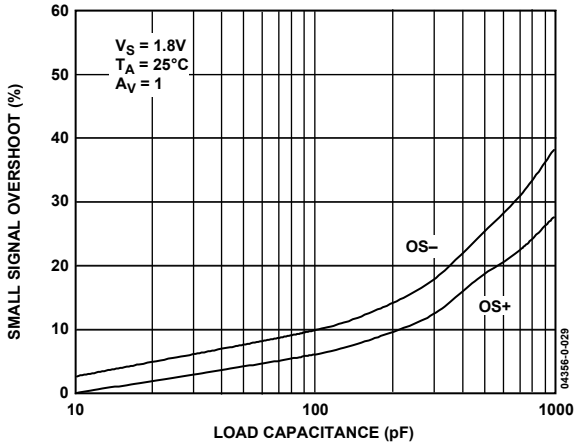


Figure 32. Small Signal Overshoot vs. Load Capacitance

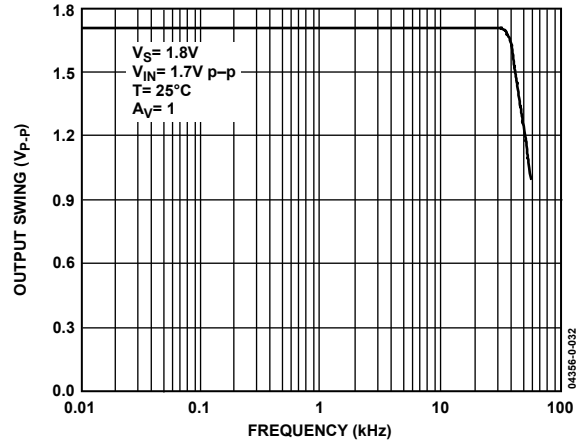


Figure 35. Closed-Loop Output Voltage Swing vs. Frequency

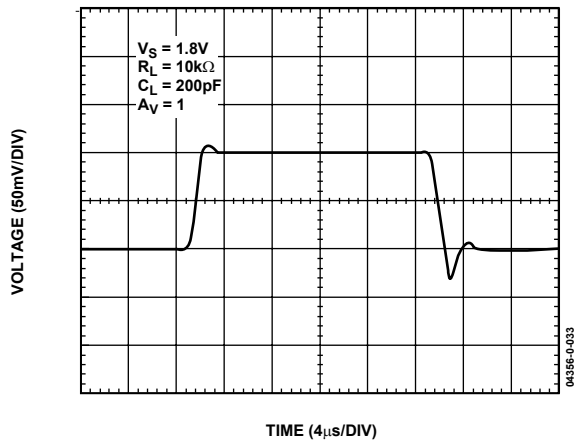


Figure 36. Small Signal Transient

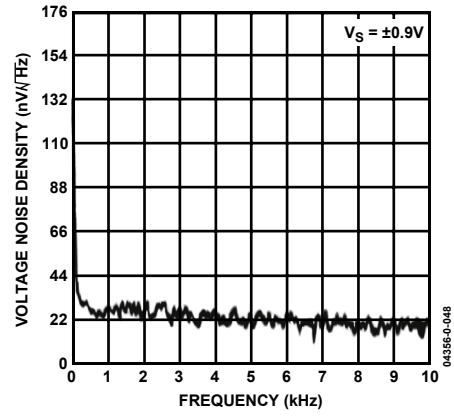


Figure 39. Voltage Noise Density

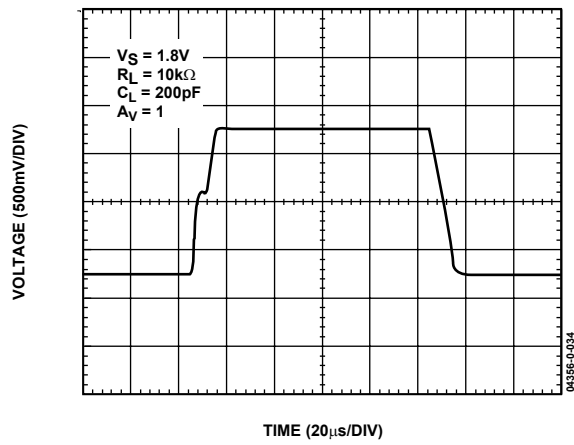


Figure 37. Large Signal Transient

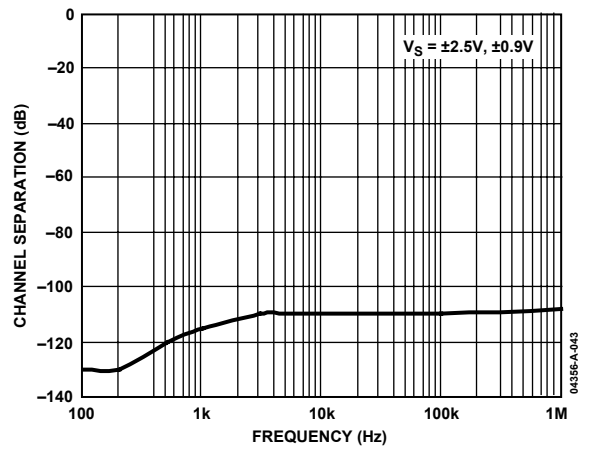


Figure 40. Channel Separation

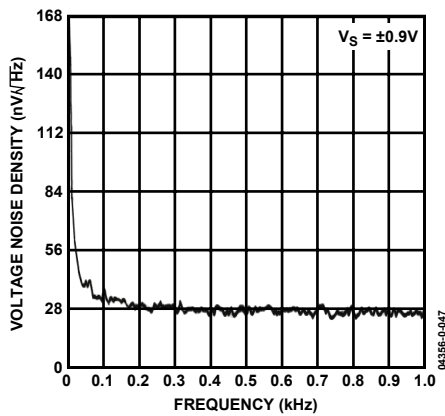


Figure 38. Voltage Noise Density

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APPLICATIONS

NO PHASE REVERSAL

The AD8603/AD8607/AD8609 do not exhibit phase inversion even when the input voltage exceeds the maximum input common-mode voltage. Phase reversal can cause permanent damage to the amplifier, resulting in system lockups. The AD8603/AD8607/AD8609 can handle voltages of up to 1 V over the supply.

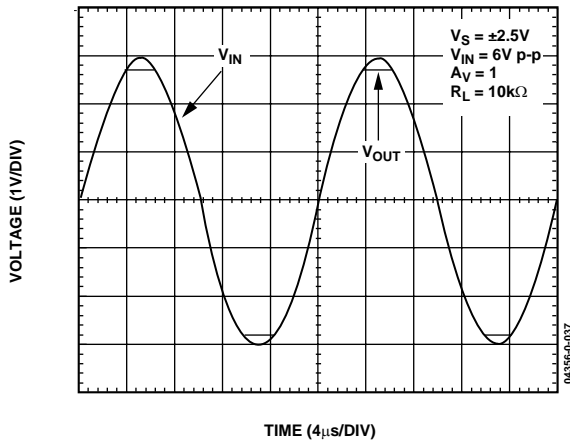


Figure 41. No Phase Response

INPUT OVERVOLTAGE PROTECTION

If a voltage 1 V higher than the supplies is applied at either input, the use of a limiting series resistor is recommended. If both inputs are used, each one should be protected with a series resistor.

To ensure good protection, the current should be limited to a maximum of 5 mA. The value of the limiting resistor can be determined from the equation

$$(V_{IN} - V_S)/(R_S + 200 \Omega) \leq 5 \text{ mA}$$

DRIVING CAPACITIVE LOADS

The AD8603/AD8607/AD8609 are capable of driving large capacitive loads without oscillating. Figure 42 shows the output of the AD8603/AD8607/AD8609 in response to a 100 mV input signal, with a 2 nF capacitive load.

Although it is configured in positive unity gain (the worst case), the AD8603 shows less than 20% overshoot. Simple additional circuitry can eliminate ringing and overshoot.

One technique is the snubber network, which consists of a series RC and a resistive load (see Figure 43). With the snubber in place, the AD8603/AD8607/AD8609 are capable of driving capacitive loads of 2 nF with no ringing and less than 3% overshoot.

The use of the snubber circuit is usually recommended for unity gain configurations. Higher gain configurations help improve the stability of the circuit. Figure 44 shows the same output response with the snubber in place.

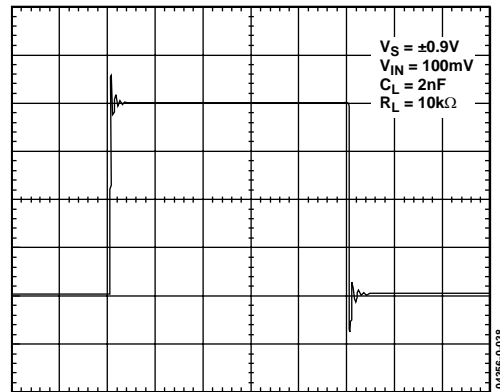


Figure 42. Output Response to a 2 nF Capacitive Load, without Snubber

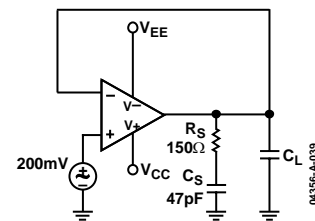


Figure 43. Snubber Network

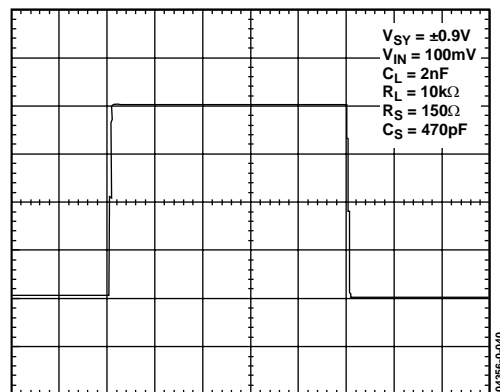


Figure 44. Output Response to a 2 nF Capacitive Load, with Snubber

Optimum values for R_S and C_S are determined empirically; Table 5 lists a few starting values.

Table 5. Optimum Values for the Snubber Network

C_L (pF)	R_S (Ω)	C_S (pF)
100~500	500	680
1500	100	330
1600~2000	400	100

PROXIMITY SENSORS

Proximity sensors can be capacitive or inductive and are used in a variety of applications. One of the most common applications is liquid level sensing in tanks. This is particularly popular in pharmaceutical environments where a tank must know when to stop filling or mixing a given liquid. In aerospace applications, these sensors detect the level of oxygen used to propel engines. Whether in a combustible environment or not, capacitive sensors generally use low voltage. The precision and low voltage of the AD8603/AD8607/AD8609 make the parts an excellent choice for such applications.

COMPOSITE AMPLIFIERS

A composite amplifier can provide a very high gain in applications where high closed-loop dc gains are needed. The high gain achieved by the composite amplifier comes at the expense of a loss in phase margin. Placing a small capacitor, C_F , in the feedback in parallel with R_2 (Figure 45) improves the phase margin. Picking $C_F = 50$ pF yields a phase margin of about 45° for the values shown in Figure 45.

A composite amplifier can be used to optimize dc and ac characteristics. Figure 46 shows an example using the AD8603 and the AD8541. This circuit offers many advantages. The bandwidth is increased substantially, and the input offset voltage and noise of the AD8541 become insignificant since they are divided by the high gain of the AD8603.

The circuit of Figure 46 offers a high bandwidth (nearly double that of the AD8603), a high output current, and a very low power consumption of less than $100 \mu\text{A}$.

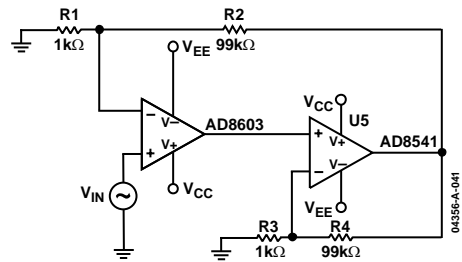


Figure 45. High Gain Composite Amplifier

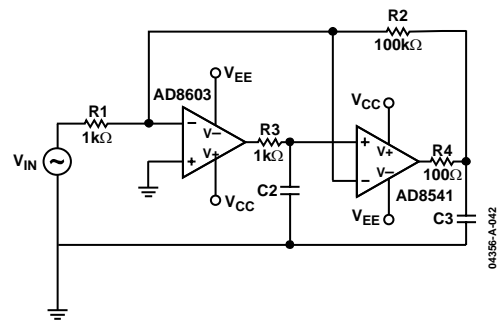


Figure 46. Low Power Composite Amplifier

AD8603/AD8607/AD8609

BATTERY-POWERED APPLICATIONS

The AD8603/AD8607/AD8609 are ideal for battery-powered applications. The parts are tested at 5 V, 3.3 V, 2.7 V, and 1.8 V and are suitable for various applications whether in single or dual supply.

In addition to their low offset voltage and low input bias, the AD8603/AD8607/AD8609 have a very low supply current of 40 μ A, making the parts an excellent choice for portable electronics. The TSOT package allows the AD8603 to be used on smaller board spaces.

PHOTODIODES

Photodiodes have a wide range of applications from bar code scanners to precision light meters and CAT scanners. The very low noise and low input bias current of the AD8603/AD8607/AD8609 make the parts very attractive amplifiers for I-V conversion applications.

Figure 47 shows a simple photodiode circuit. The feedback capacitor helps the circuit maintain stability. The signal bandwidth can be increased at the expense of an increase in the total noise; a low-pass filter can be implemented by a simple RC

network at the output to reduce the noise. The signal bandwidth can be calculated by $\frac{1}{2\pi R_2 C_2}$ and the closed-loop bandwidth is the intersection point of the open-loop gain and the noise gain.

The circuit shown in Figure 47 has a closed-loop bandwidth of 58 kHz and a signal bandwidth of 16 Hz. Increasing C_2 to 50 pF yields a closed-loop bandwidth of 65 kHz, but only 3.2 Hz of signal bandwidth can be achieved.

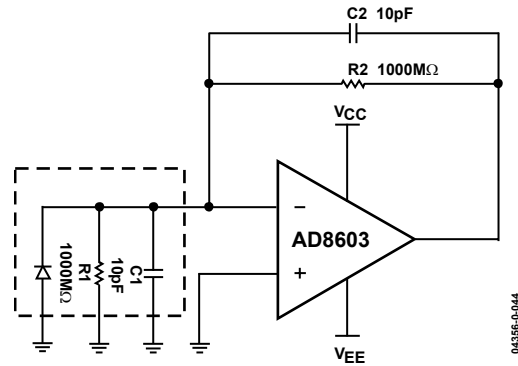
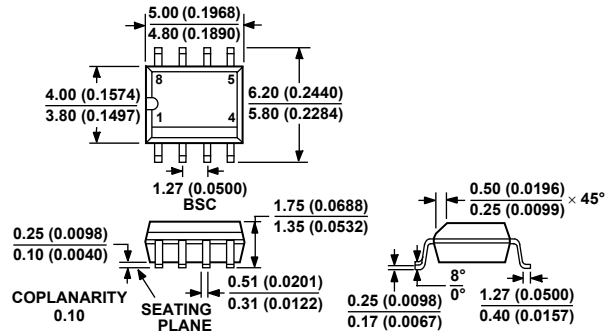


Figure 47. Photodiode Circuit

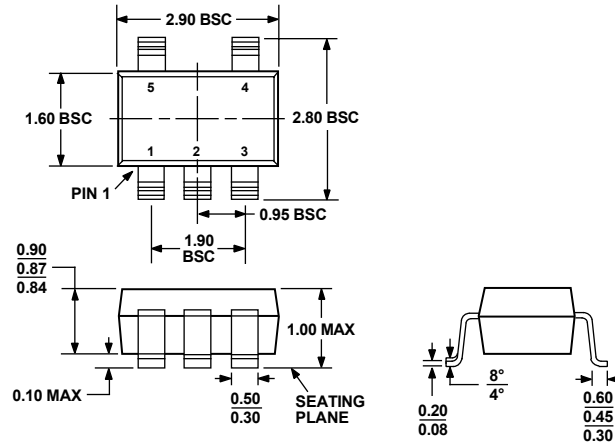
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OUTLINE DIMENSIONS



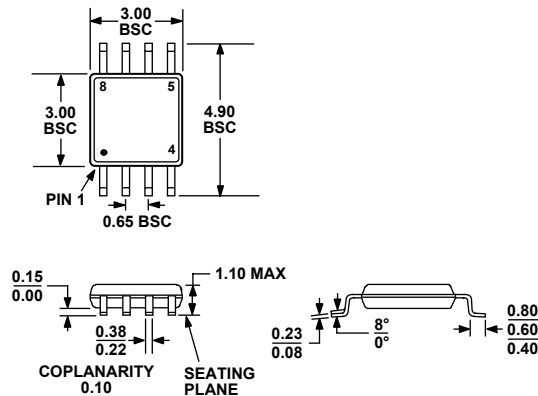
COMPLIANT TO JEDEC STANDARDS MS-012AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 48. 8-Lead Standard Small Outline Package (SOIC) [R-8]
 Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-193AB

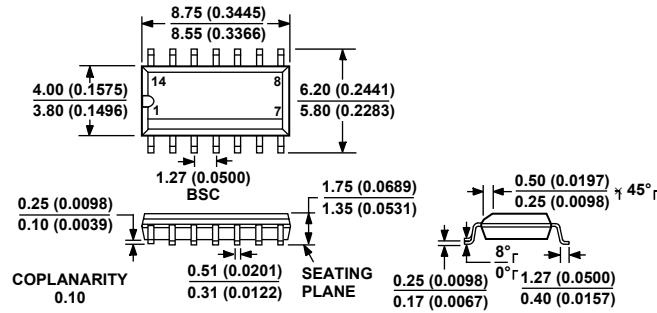
Figure 49. 5-Lead Thin Small Outline Transistor Package [TSOT]
 (UJ-5)
 Dimensions in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

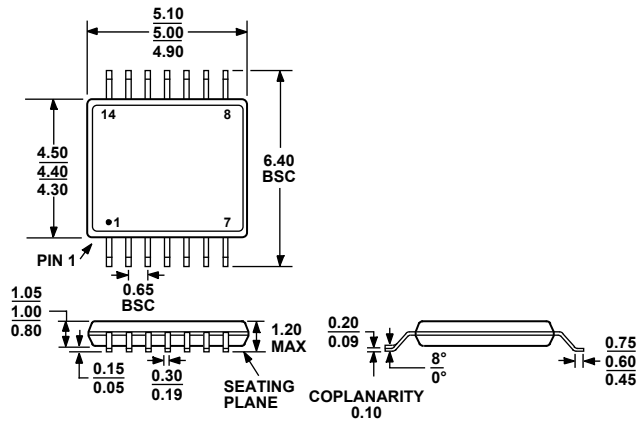
Figure 50. 8-Lead MSOP Package (RM-8)
 Dimensions in millimeters

AD8603/AD8607/AD8609



COMPLIANT TO JEDEC STANDARDS MS-012AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 51. 14-Lead Standard Small Outline Package (SOIC) [R-14]
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

Figure 52. 14-Lead Thin Shrink Small Outline Package (TSSOP) [RU-14]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8603AUJ-R2	-40°C to +125°C	5-Lead TSOT-23	UJ-5	BFA
AD8603AUJ-REEL	-40°C to +125°C	5-Lead TSOT-23	UJ-5	BFA
AD8603AUJ-REEL7	-40°C to +125°C	5-Lead TSOT-23	UJ-5	BFA
AD8607ARM-R2	-40°C to +125°C	8-Lead MSOP	RM-8	A00
AD8607ARM-REEL	-40°C to +125°C	8-Lead MSOP	RM-8	A00
AD8607AR	-40°C to +125°C	8-Lead SOIC	R-8	
AD8607AR-REEL	-40°C to +125°C	8-Lead SOIC	R-8	
AD8607AR-REEL7	-40°C to +125°C	8-Lead SOIC	R-8	
AD8609AR	-40°C to +125°C	14-Lead SOIC	R-14	
AD8609AR-REEL	-40°C to +125°C	14-Lead SOIC	R-14	
AD8609AR-REEL7	-40°C to +125°C	14-Lead SOIC	R-14	
AD8609ARU	-40°C to +125°C	14-Lead TSSOP	RU-14	
AR8609ARU-REEL	-40°C to +125°C	14-Lead TSSOP	RU-14	