19-1327; Rev 1; 2/98

EVALUATION KIT AVAILABLE

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

General Description

The MAX686 DAC-controlled boost/inverter IC converts a positive input voltage to a positive or negative LCD bias voltage up to +27.5V or -27.5V. The device features an internal N-channel MOSFET switch, programmable current limiting, and an internal 6-bit digital-to-analog converter (DAC) for digital adjustment of the output voltage. It comes in a small 16-pin QSOP package (same size as an 8-pin SO).

The MAX686 uses a current-limited, pulse-frequency-modulation (PFM) control scheme to provide high efficiency over a wide range of load conditions. Its high switching frequency (up to 300kHz) allows the use of small external components.

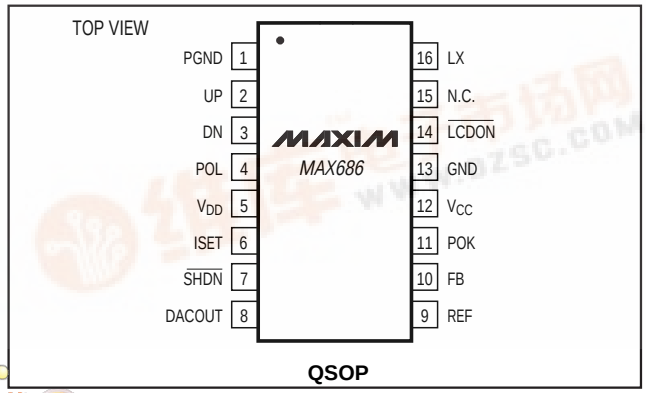
An $\overline{\text{LCDON}}$ output allows the LCD bias voltage to be automatically disabled when the display logic voltage is removed, protecting the display. The MAX686 has a +2.7V to +5.5V input voltage range for the IC, and a +0.8V to +27.5V input voltage range for the inductor. Typical quiescent supply current is 65µA. Shutdown current is 1.5µA.

The MAX686 offers high-level integration to save space, reduce power consumption, and increase battery life, making it an excellent choice for battery-powered portable equipment. The MAX629 is similar to the MAX686, except that it does not contain a built-in DAC. Both devices have evaluation kits to facilitate designs.

Applications

Positive or Negative LCD Bias
Personal Digital Assistants
Notebook Computers
Portable Data-Collection Terminals
Palmtop Computers
Varactor Tuning Diode Bias

Pin Configuration



Features

- ♦ **Internal 500mA, 28V N-Channel Switch (no external FET required)**
- ♦ **Adjustable Output Voltage to +27.5V or -27.5V**
- ♦ **6-Bit DAC-Controlled Output Voltage**
- ♦ **Up to 90% Efficiency**
- ♦ **Small 16-Pin QSOP Package (Same size as 8-pin SO)**
- ♦ **Power-OK Indicator**
- ♦ **65µA Quiescent Current**
- ♦ **1.5µA Shutdown Current**
- ♦ **Up to 300kHz Switching Frequency**

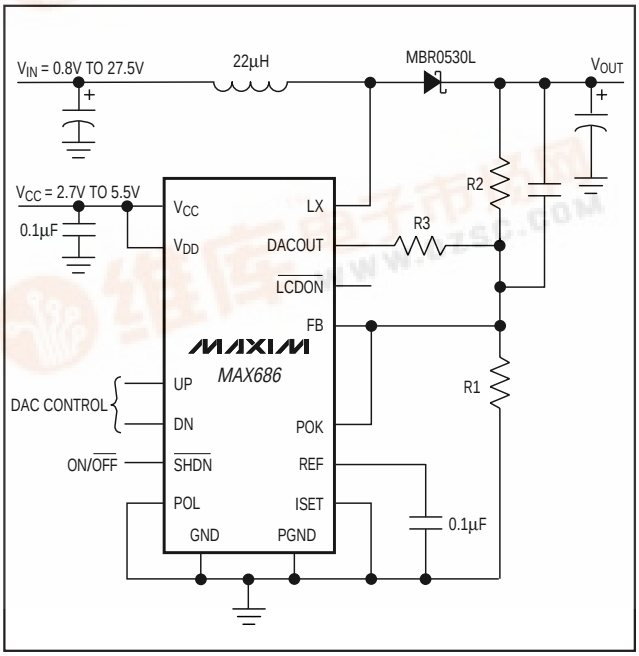
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX686C/D	0°C to +70°C	Dice*
MAX686EEE	-40°C to +85°C	16 QSOP

**Dice are specified at T_A = +25°C, DC parameters only.*

Functional Diagram appears at end of data sheet.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Voltage
- V_{CC}, ISET, POK, POL, $\overline{SHDN}$, UP, DN, V_{DD} to GND .....-0.3V to +6V
- FB, REF, DACOUT to GND.....-0.3V to (V_{CC} + 0.3V)
- PGND to GND .....-0.3V to +0.3V
- LX, $\overline{LCDON}$ to GND.....-0.3V to +30V

Current
- LX (sinking) 600mA
- $\overline{LCDON}$ (sinking).....10mA

Continuous Power Dissipation (T_A = +70°C)
- QSOP (derate 8.30mW/°C above +70°C).....667mW

Operating Temperature Ranges
- MAX686C/D .....0°C to +70°C
- MAX686EEE.....-40°C to +85°C

Storage Temperature Range .....-65°C to +160°C

Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} = V_{IN} = +5V, C_{REF} = 0.1µF, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V_{CC}, V_{DD}		2.7		5.5	V
Input Voltage	V_{IN}	Voltage applied to L1	0.8		V_{OUT}	V
Supply Current	I_{CC} + I_{DD}	POL = GND, V_{FB} = 1.3V, I_{DACOUT} = 0mA		65	125	µA
Shutdown Current	I_{SHDN}	$\overline{SHDN}$ = GND		1.3	4	µA
V_{CC} Undervoltage Lockout	V_{LOCK}	Rising or falling	2.10	2.5	2.65	V
V_{CC} Undervoltage Lockout Hysteresis				100		mV
V_{CC} DAC Reset Threshold	V_{RESET}		0.5	1.5	2.1	V
Line Regulation		Boost configuration, V_{OUT} = 27.5V, I_{LOAD} = 5mA, V_{CC} = V_{DD} = 2.7V to 5.5V		0.1		%/V
Load Regulation		Boost configuration, V_{OUT} = 27.5V, I_{LOAD} = 0mA to 5mA		0.01		%/mA
LX						
LX Voltage Range	V_{LX}				28	V
LX Switch Current Limit	I_{LX}	ISET = V_{CC}	0.42	0.50	0.58	A
		ISET = GND	0.21	0.25	0.29	
LX On-Resistance	R_{LX}	V_{CC} = V_{DD} = 5V, I_{LX} = 100mA		0.6	1.2	Ω
		V_{CC} = V_{DD} = 3.3V, I_{LX} = 100mA		0.8	1.6	
LX Leakage Current	I_{LXLEAK}	V_{LX} = 28V			1.5	µA
Maximum LX On-Time	t_{ON}		8	10	12	µs
Minimum LX Off-Time	t_{OFF}	POL = GND, V_{FB} > 1.2V	0.8	1	1.2	µs
		POL = V_{CC}, V_{FB} < 0.15V	2.8	3.5	4.2	
		POL = GND, V_{FB} < 0.8V	4	5	6	
		POL = V_{CC}, V_{FB} > 0.4V	4	5	6	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{DD} = V_{IN} = +5V, C_{REF} = 0.1µF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE AND FB INPUT						
REF Output Voltage	V_{REF}	V_{CC} = V_{DD} = 2.7V to 5.5V, no load	1.225	1.250	1.275	V
REF Load Regulation		I_{REF} = 0µA to 25µA, C_{REF} = 0.1µF		1	10	mV
		I_{REF} = 0µA to 50µA, C_{REF} = 0.47µF		1.5		
FB Set Point	V_{FB}	POL = GND	1.225	1.250	1.275	V
		POL = V_{CC}	-15	0	15	mV
FB Input Bias Current	I_{FB}				±50	nA
POWER OK COMPARATOR, $\overline{LCDON}$ OUTPUT						
POK Threshold	V_{POK}	V_{POK} rising	1.100	1.125	1.150	V
POK Input Current	I_{POK}				±50	nA
POK Hysteresis				12		mV
$\overline{LCDON}$ Sink Current	$I_{\overline{LCDON}}$	$V_{\overline{LCDON}}$ = 0.4V, V_{POK} = 1.25V	2	6		mA
$\overline{LCDON}$ Leakage Current		$V_{\overline{LCDON}}$ = 28V, V_{POK} = GND		0.02	1	µA
DAC OUTPUT (Notes 2, 3)						
Full-Scale Output Voltage	V_{FS}	-50µA < I_{DACOUT} < 0µA	V_{REF} - 0.015	V_{REF}	V_{REF} + 0.015	V
Zero-Scale Output Voltage	V_{ZS}	0µA < I_{DACOUT} < 20µA	0		15	mV
Resolution			6			bits
Mid-Scale Accuracy	MSA	Mid-scale = V_{REF} x 32/63	-2		2	%
Differential Nonlinearity	DNL	Guaranteed monotonic	-1		1	LSB
Output Resistance in Shutdown	R_{DACOUT}			1.5		kΩ
LOGIC INPUTS: POL, ISET, UP, DN, $\overline{SHDN}$						
Input Low Level	V_{IL}	2.7V < V_{CC} = V_{DD} < 5.5V			0.7	V
Input High Level	V_{IH}	2.7V < V_{CC} = V_{DD} < 5.5V	2.4			V
Input Bias Current	I_{BIAS}				±1	µA
Pulse Width High	t_{PWH}	UP, DN, T_A = +25°C	1			µs
Pulse Width Low	t_{PWL}	UP, DN, T_A = +25°C	1			µs
Pulse Separation	t_{PWS}	UP, DN, T_A = +25°C	1			µs

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{DD} = V_{IN} = +5V, C_{REF} = 0.1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V_{CC}, V_{DD}		2.7		5.5	V
Input Voltage	V_{IN}	Voltage applied to L1	0.8		V_{OUT}	V
Supply Current	I_{CC} + I_{DD}	POL = GND, VFB = 1.3V, I_{DACOUT} = 0mA			125	µA
Shutdown Current	I_{SHDN}	$\overline{SHDN}$ = GND			4	µA
V_{CC} Undervoltage Lockout	V_{LOCK}	Rising or falling	2.10		2.65	V
LX						
LX Voltage Range	V_{LX}				28	V
LX Switch Current Limit	I_{LX}	ISET = V_{CC}	0.4		0.6	A
		ISET = GND	0.2		0.3	
LX On-Resistance	R_{LX}	V_{CC} = V_{DD} = 5V, I_{LX} = 100mA			1.2	Ω
		V_{CC} = V_{DD} = 3.3V, I_{LX} = 100mA			1.6	
LX Leakage Current	I_{LXLEAK}	V_{LX} = 28V			1.5	µA
Maximum LX On-Time	t_{ON}		7.5		12.5	µs
Minimum LX Off-Time	t_{OFF}	POL = GND, V_{FB} > 1.2V	0.7		1.3	µs
		POL = V_{CC}, V_{FB} < 0.15V	2.8		4.2	
		POL = GND, V_{FB} < 0.8V	3.8		6.2	
		POL = V_{CC}, V_{FB} > 0.4V	3.8		6.2	
REFERENCE AND FB INPUT						
REF Output Voltage	V_{REF}	V_{CC} = V_{DD} = 2.7V to 5.5V, no load	1.22		1.28	V
REF Load Regulation		I_{REF} = 0µA to 25µA, C_{REF} = 0.1µF			10	mV
FB Set Point	V_{FB}	POL = GND	1.22		1.28	V
		POL = V_{CC}	-15		15	mV
FB Input Bias Current	I_{FB}				±50	nA
POWER OK COMPARATOR, $\overline{LCDON}$ OUTPUT						
POK Threshold	V_{POK}	V_{POK} rising	1.05		1.20	V
POK Input Current	I_{POK}				±50	nA
$\overline{LCDON}$ Sink Current	$I_{\overline{LCDON}}$	$V_{\overline{LCDON}}$ = 0.4V, V_{POK} = 1.25V	2			mA
DAC OUTPUT (Notes 2, 3)						
Full-Scale Output Voltage	V_{FS}	-50µA < I_{DACOUT} < 0µA	V_{REF} - 0.02		V_{REF} + 0.02	V
Zero-Scale Output Voltage	V_{ZS}	0µA < I_{DACOUT} < 20µA	0		15	mV
Resolution			6			Bits
Mid-Scale Accuracy	MSA	Mid-scale = V_{REF} x 32/63	-3		3	%
LOGIC INPUTS: POL, ISET, UP, DN, $\overline{SHDN}$						
Input Low Level	V_{IL}	2.7V < V_{CC} = V_{DD} < 5.5V			0.7	V
Input High Level	V_{IH}	2.7V < V_{CC} = V_{DD} < 5.5V	2.4			V
Input Bias Current	I_{BIAS}				±1	µA

Note 1: The MAX686 requires a supply voltage at V_{CC} = V_{DD} between +2.7V and +5.5V; however, the voltage that supplies the inductor can vary from +0.8V to +27.5V, depending on circuit operating conditions.

Note 2: The DAC output is set to its midpoint value at power-on.

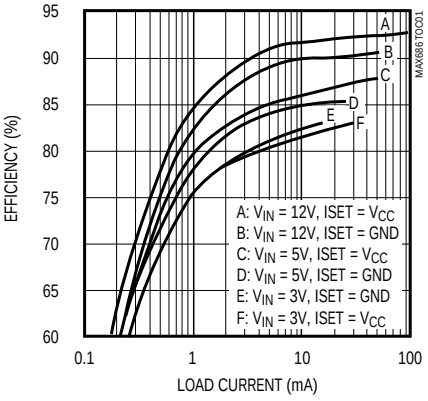
Note 3: The DAC setting is guaranteed to remain valid as long as V_{CC} is greater than the V_{CC} DAC Reset Threshold.

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

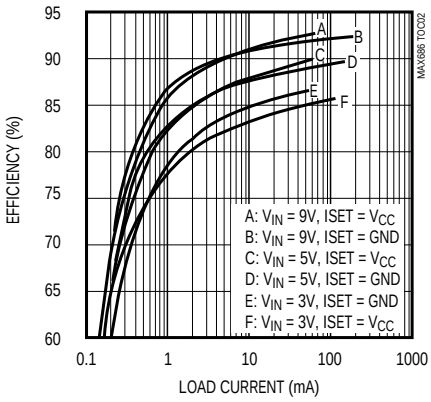
Typical Operating Characteristics

(Circuits of Figures 1 and 2, $V_{CC} = V_{DD} = V_{IN} = +5V$, L1 = 22µH, $\overline{SHDN} = V_{CC}$, $C_{REF} = 0.1\mu F$, $T_A = +25°C$, unless otherwise noted.)

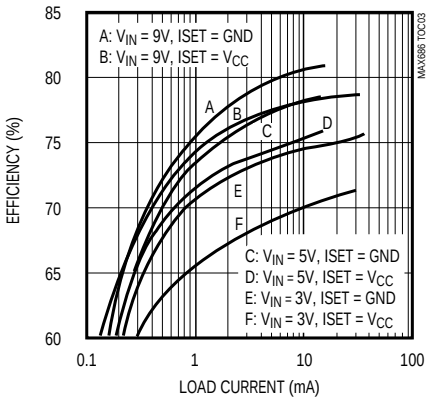
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = +24V)



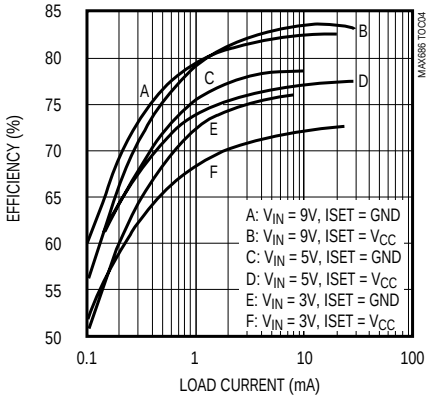
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = +12V)



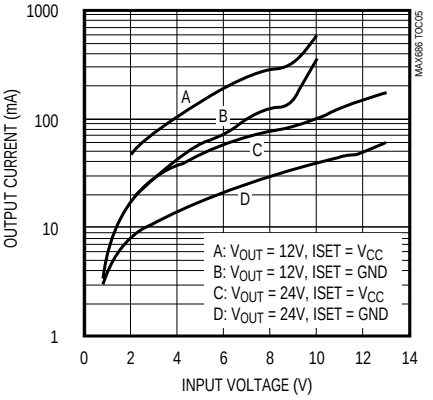
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = -12V)



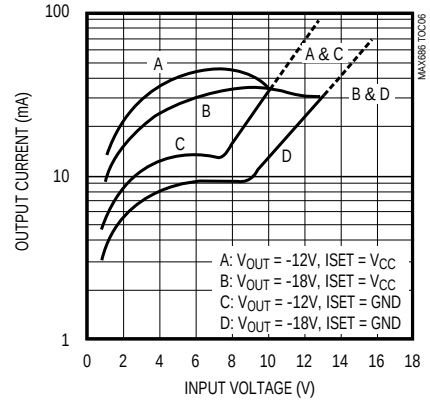
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = -18V)



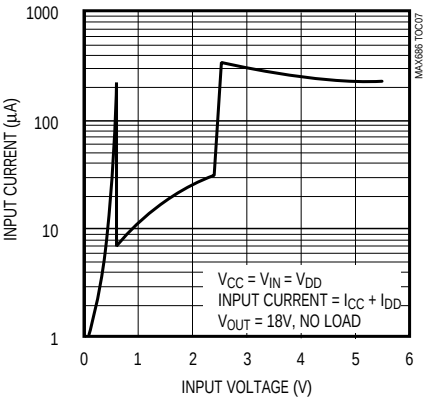
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE (V_{OUT} = +12V, +24V)



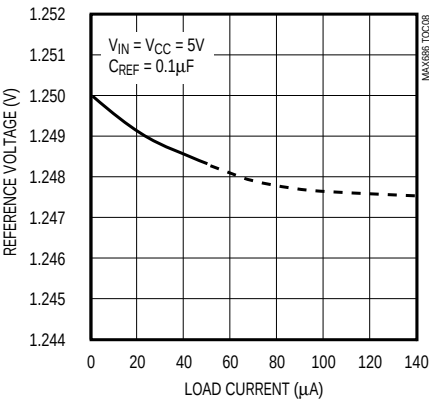
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE (V_{OUT} = -12V, -18V)



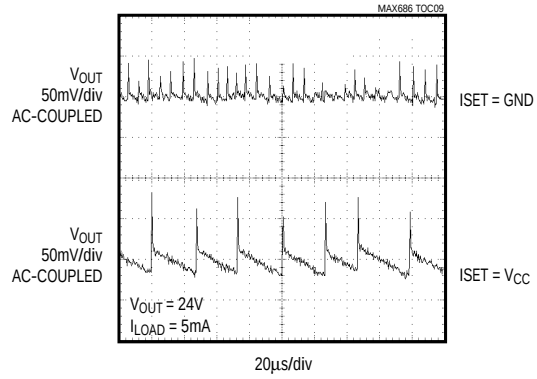
INPUT CURRENT vs. INPUT VOLTAGE



REFERENCE VOLTAGE vs. LOAD CURRENT



OUTPUT VOLTAGE RIPPLE

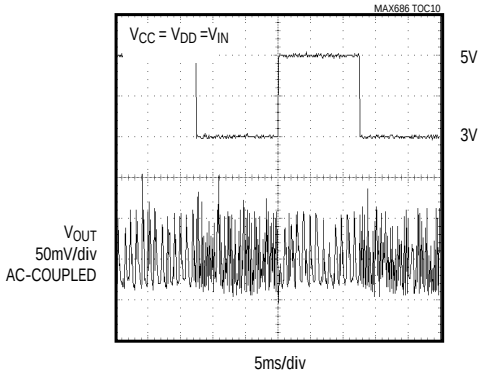


DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

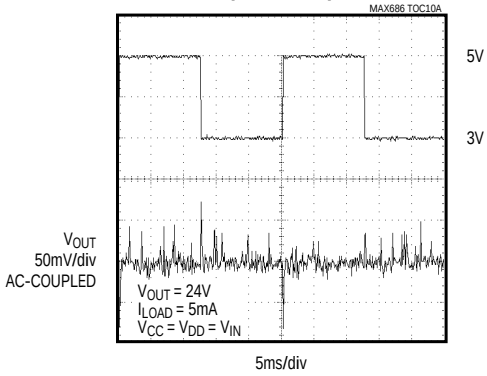
Typical Operating Characteristics (continued)

(Circuits of Figures 1 and 2, $V_{CC} = V_{DD} = V_{IN} = +5V$, L1 = 22µH, $\overline{SHDN} = V_{CC}$, $C_{REF} = 0.1\mu F$, $T_A = +25°C$, unless otherwise noted.)

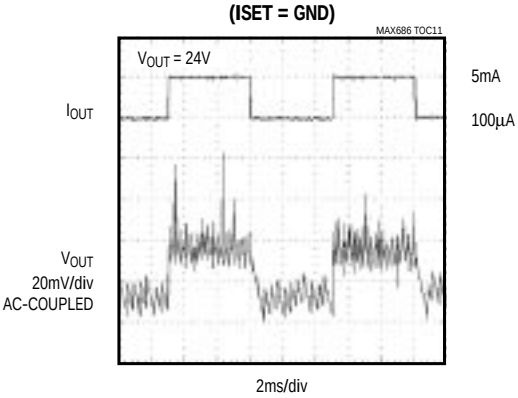
LINE-TRANSIENT RESPONSE (ISET = V_{CC})



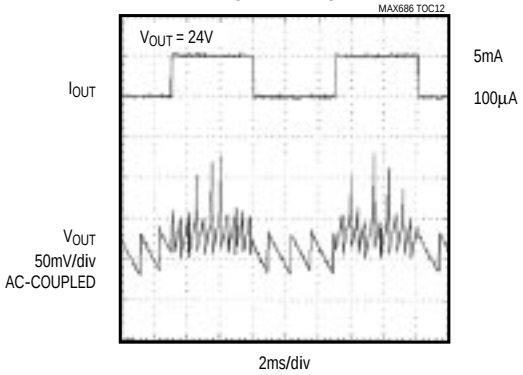
LINE-TRANSIENT RESPONSE (ISET = GND)



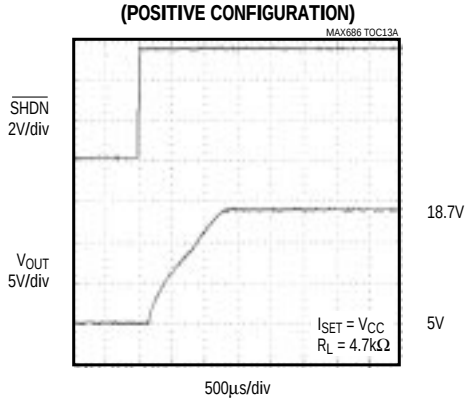
LOAD-TRANSIENT RESPONSE (ISET = GND)



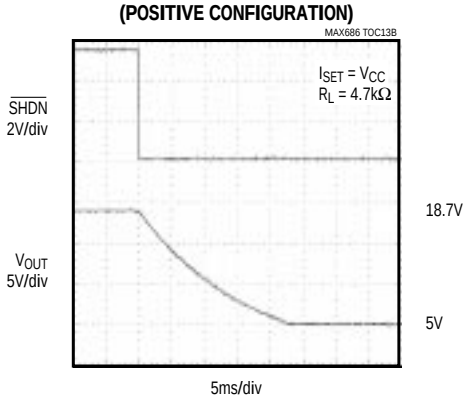
LOAD-TRANSIENT RESPONSE (ISET = V_{CC})



POWER-UP RESPONSE (POSITIVE CONFIGURATION)



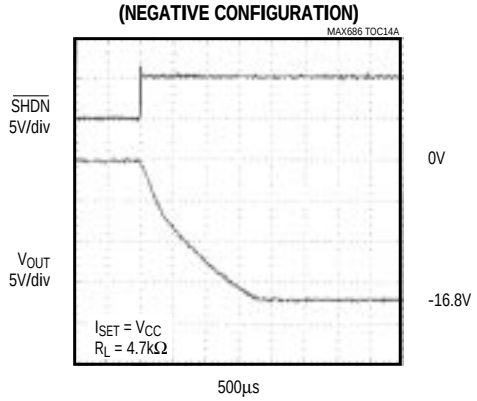
POWER-DOWN RESPONSE (POSITIVE CONFIGURATION)



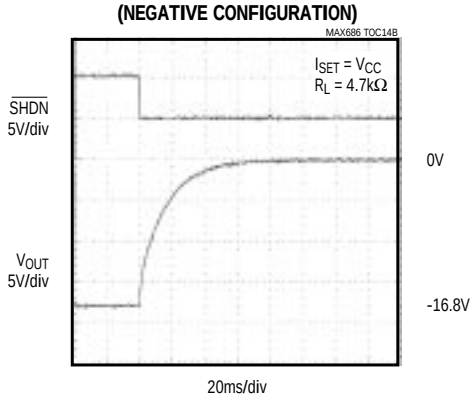
Typical Operating Characteristics (continued)

(Circuits of Figures 1 and 2, V_{CC} = V_{DD} = V_{IN} = +5V, L1 = 22µH, $\overline{SHDN}$ = V_{CC}, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

POWER-UP RESPONSE (NEGATIVE CONFIGURATION)



POWER-DOWN RESPONSE (NEGATIVE CONFIGURATION)



Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground. Connect to GND.
2	UP	Increment Output Voltage Input. Increments the DAC on each rising edge such that $\|V_{OUT}\|$ increases.
3	DN	Decrement Output Voltage Input. Decrements the DAC on each rising edge such that $\|V_{OUT}\|$ decreases.
4	POL	Polarity Input. Changes polarity and threshold of FB to allow regulation of either positive or negative output voltages. POL also changes the polarity of the DAC output such that increasing codes always increases the magnitude of the output voltage. Set POL = GND for positive output voltage, or set POL = V_{CC} for negative output voltage.
5	V_{DD}	Gate-Drive Supply for Internal MOSFET. Connect to V_{CC}.
6	ISET	Set LX Current Limit. Sets the peak current limit for the internal switch. Connect to V_{CC} for 500mA current limit. Connect to GND for 250mA current limit.
7	$\overline{SHDN}$	Shutdown Input. A logic low on $\overline{SHDN}$ places the MAX686 in shutdown mode. Connect to V_{CC} for normal operation.
8	DACOUT	DAC Output Voltage
9	REF	Reference Output. Bypass with a 0.1µF ceramic capacitor to GND.
10	FB	Feedback Input. Connect to an external voltage divider to set the MAX686 output voltage. See the section *Setting the Output Voltage with the DAC*.
11	POK	Power-OK Sense Input/Power-OK Comparator Input. When the voltage applied to POK is greater than 1.125V, $\overline{LCDON}$ is low. Connect to a resistive voltage divider monitoring V_{IN} or V_{OUT}.
12	V_{CC}	IC Power-Supply Input
13	GND	Ground
14	$\overline{LCDON}$	Power-OK Comparator Open-Drain Output. Connect to external switch to turn LCD power on or off. See the section *Controlling the LCD Using POK and $\overline{LCDON}$*.
15	N.C.	No Connection. Not internally connected.
16	LX	Drain of Internal 28V, 500mA N-Channel Switch

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

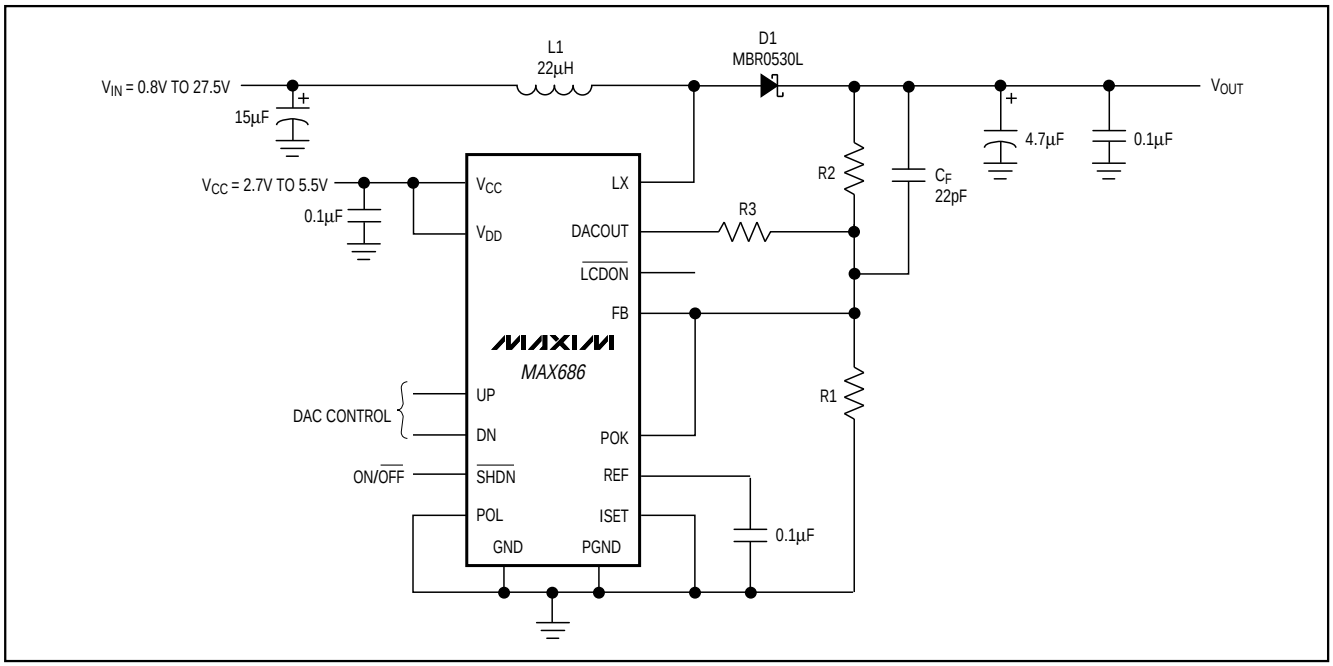


Figure 1. Boost Configuration: Positive Output Voltage

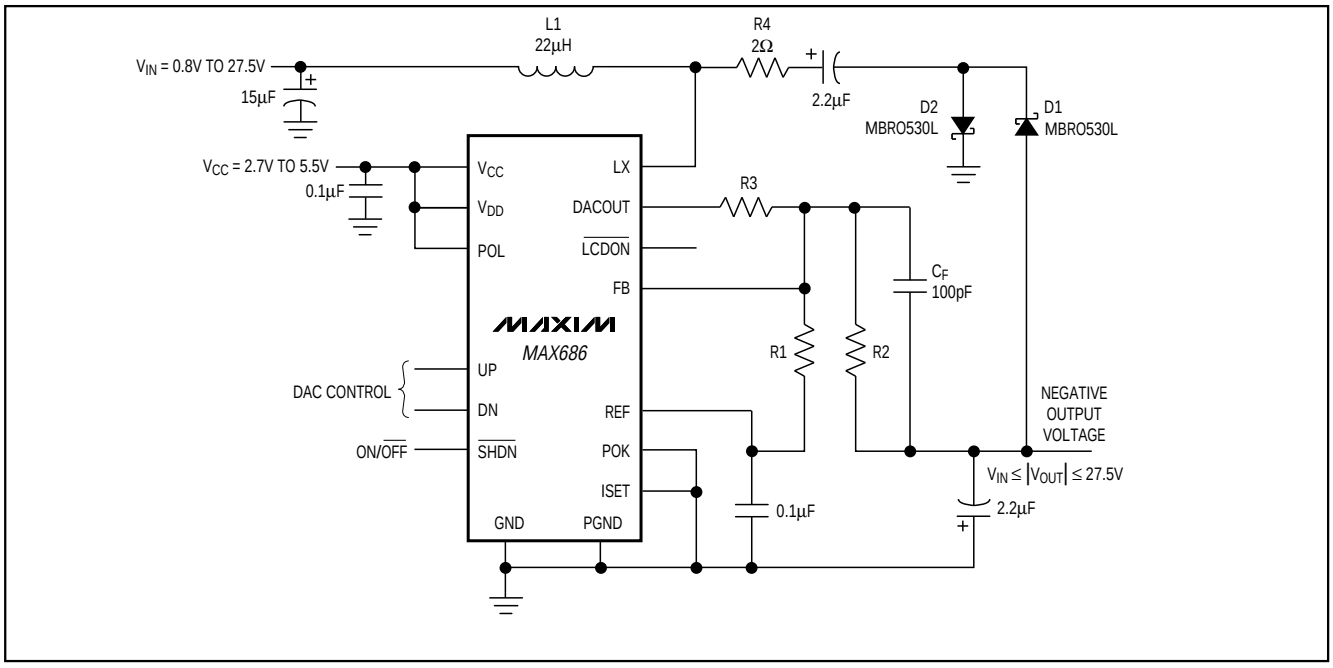


Figure 2. Negative Output Voltage Application Circuit

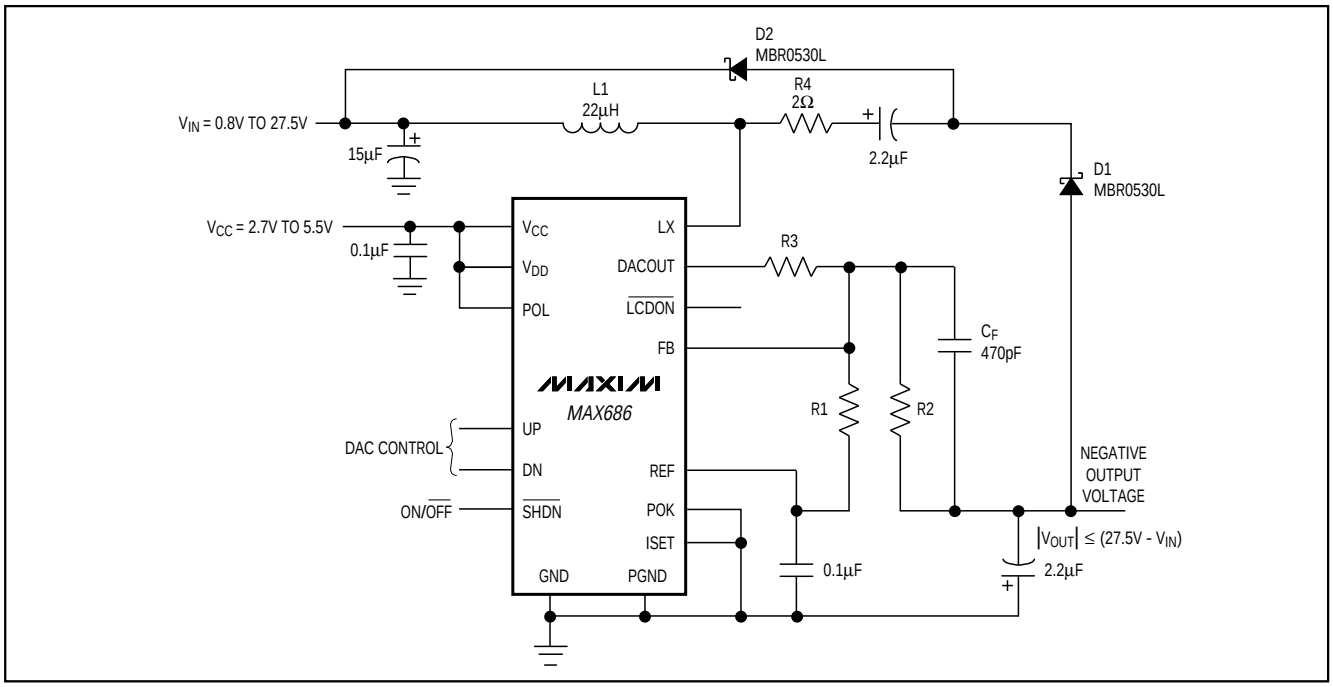


Figure 3. Alternative Negative Output Voltage Application Circuit

Detailed Description

The MAX686 is a step-up converter that contains an internal N-channel MOSFET switch to convert a +0.8V to +27.5V battery voltage to a higher positive or a negative voltage. Figure 1 shows the MAX686 configured to produce a positive output voltage. Figure 2 shows the MAX686 configured with one additional diode and capacitor to produce a negative output voltage. Figure 3 shows an alternative method for developing negative output voltages. Set the output voltage with an external resistor-divider network. Adjust the output voltage with the internal digital-to-analog converter (DAC). The MAX686's current-limited pulse-frequency-modulation (PFM) control scheme has programmable current limiting and provides high efficiency over a wide range of load conditions.

Boost Control Scheme (POL = GND)

A combination of peak current limiting and a pair of one-shots controls the MAX686 switching. During the on-cycle, the internal switch closes, and current through the inductor ramps up until either the fixed 10µs maximum on-time expires (at low input voltages) or the switch peak current limit is reached. The peak current limit is selectable to either 500mA (ISET = V_{CC}) or 250mA (ISET = GND) (see the section *Setting the Peak Inductor Current Limit*).

After the on-cycle terminates, the switch turns off, and the inductor charges the output capacitor through the diode. If the output is out of regulation after the minimum off-time has transpired, another on-cycle begins. If the output is within regulation when the minimum off-time transpires, the off-cycle extends until the output falls out of regulation, at which point an on-cycle starts.

The MAX686 regulates the voltage on FB (V_{FB}) to 1.25V. When the output is well below regulation (V_{FB} is less than 1V and the switch current limit is exceeded), the MAX686 operates in initial power-up mode, and the minimum off-time increases to 5µs to provide soft-start. The switching frequency, which depends on the load, the input voltage, and the output voltage, can be as high as 300kHz.

Inverting Control Scheme (POL = V_{CC})

In inverting operation, the MAX686 regulates the voltage on FB (V_{FB}) to 0V, and the error amplifier's polarity is reversed. The minimum off-time changes to 3.5µs for negative output voltages. When the output is well below regulation (V_{FB} is 0.25V or more and the switch current limit is exceeded), initial power-up is assumed, and the minimum off-time increases to 5µs to provide soft-start.

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

Power-OK Comparator

POK is the input to the power-OK comparator. The comparator drives an internal N-channel MOSFET. The MOSFET's open-drain output, $\overline{LCDON}$, can drive an external PNP transistor or P-channel MOSFET, switching a positive V_{OUT} to the LCD (Figures 6 and 7). When the voltage at POK exceeds 1.125V (power OK), $\overline{LCDON}$ goes low, turning on the external PNP transistor. When the voltage at POK drops below 1.125V (power not OK), the external PNP transistor turns off, cutting off power to the LCD display. This feature ensures that the LCD display is not damaged due to improper voltage levels. During shutdown or undervoltage lockout, $\overline{LCDON}$ is high impedance.

Shutdown Mode

When $\overline{SHDN}$ is low, the MAX686 enters shutdown mode, in which the control circuit, POK comparator, DAC output buffer, reference, and internal biasing circuitry turn off. The DAC setting is stored as long as V_{CC} remains above the DAC reset threshold. Supply current drops to 1.5µA. $\overline{SHDN}$ is a logic-level input; connect it to V_{CC} for normal operation.

The output voltage in shutdown mode depends on the output voltage polarity. In the positive output voltage configuration (Figure 1), the output is directly connected to the input through the diode (D1) and the inductor (L1). When the device is in shutdown mode, the output voltage falls to one diode drop below the input voltage, and any load connected to the output may still conduct current. In the negative output voltage configuration (Figures 2 and 3), there is no DC path between the input and the output, and the output falls to GND in shutdown mode.

Internal DAC

The MAX686 contains an internal 6-bit counter and DAC to control the output voltage digitally (see the section *Setting the Output Voltage with the DAC*). The UP and DN input pins drive an internal up/down counter that directly controls the DAC. To increase the magnitude of V_{OUT} in the boost configuration, apply a rising edge to UP. This decreases the DAC output voltage one step and correspondingly increases V_{OUT}. Conversely, to decrease the magnitude of V_{OUT}, apply a rising edge to DN. This increases the DAC output voltage one step and correspondingly decreases V_{OUT}. The UP and DN control direction reverses for a negative output to maintain the same control direction of the absolute magnitude of the output voltage. Upon power-up, the DAC code internally goes to mid-scale. The DAC's internal counter does not roll over once it reaches full scale or zero. Therefore, additional rising edges to make the counter roll over are ignored, preventing unexpected undervoltages or overvoltages.

Internal Reference

The MAX626's 1.25V internal reference is accurate to ±2% over temperature. It can source up to 50µA of current and should be bypassed with at least a 0.1µF capacitor. See the *Bypass Capacitors* section.

Design Procedure

Setting the Output Voltage with the DAC

For either positive or negative output voltage applications, set the MAX686's output voltage using three external resistors (R1, R2, and R3) as shown in Figures 1, 2, and 3. Since the input bias current at FB has a 50nA maximum value, large resistors can be used in the feedback loop without a significant loss of accuracy. Select R1 to be in the 10kΩ to 220kΩ range and calculate R2 and R3 using the applicable equations from the following subsections.

Setting the Minimum Positive Output Voltage

The minimum output voltage is set with the resistor-divider (R1-R2, Figure 1) from V_{OUT} to FB. The minimum output voltage occurs when $V_{DACOUT} = V_{FB} = 1.25V$. Therefore, R3 has no effect on the minimum output voltage. Choose R1 to be 120kΩ so that the current in the divider is about 10µA. Then determine R2 as follows:

$$R2 = R1 \times (V_{OUT(MIN)} - V_{FB}) / V_{FB}$$

For example, if $V_{OUT(MIN)} = 12.5V$:

$$R2 = 120k\Omega \times (12.5 - 1.25) / (1.25) = 1.08M\Omega$$

Mount R1 and R2 close to the FB pin to minimize parasitic capacitance.

Setting the Maximum Positive Output Voltage

The DAC is adjustable from 0V to 1.25V in 64 steps, and 1LSB = 1.25V / 63 = 19.8mV. Calculate R3 to adjust V_{OUT} with DACOUT (Figure 1).

For $V_{OUT(MAX)} = 25V$ and $V_{OUT(MIN)} = 12.5V$, determine R3 as follows:

$$R3 = R2 \times (V_{FB}) / (V_{OUT(MAX)} - V_{OUT(MIN)})$$

$$= 1.08M\Omega \times (1.25) / (25 - 12.5) = 108k\Omega$$

The general form for V_{OUT} as a function of the DAC output (V_{DACOUT}) is:

$$V_{OUT} = V_{OUT(MIN)} + (V_{FB} - V_{DACOUT}) \times R2 / R3$$

At power-up, the DAC resets to mid-scale where $V_{DACOUT} = 0.635V$. Therefore, the output voltage after power-up is:

$$V_{OUT(MID)} = V_{OUT(MIN)} + (1.25 - 0.635) \times R2 / R3 = 18.65V$$

Note that for a positive output voltage, V_{OUT} increases as V_{DACOUT} decreases. $V_{OUT(MAX)}$ corresponds to V_{DACOUT} = 0V, and $V_{OUT(MIN)}$ corresponds to V_{DACOUT} = 1.25V.

Setting the Minimum Negative Output Voltage

For a negative output voltage, the FB threshold voltage (V_{FB}) is 0V, and R1 is placed between FB and REF (Figures 2 and 3). Again, choose R1 to be 120kΩ so that the current in the divider is about 10µA. Then determine R2 as follows:

$$R2 = R1 \times |V_{OUT} / V_{REF}|$$

For example, if $V_{OUT(MIN)}$ = -12.5V:

$$R2 = 120k\Omega \times |(-12.5) / (1.25)| = 1.2M\Omega$$

Setting the Maximum Negative Output Voltage

Assume $V_{OUT(MAX)}$ = -25V and $V_{OUT(MIN)}$ = -12.5V, then determine R3 and $V_{OUT(MID)}$ as follows:

$$R3 = R2 \times (V_{FB} - V_{DACOUT(MAX)}) / (V_{OUT(MAX)} - V_{OUT(MIN)})$$

$$= 1.2M\Omega \times (0 - 1.25) / (-25 - -12.5) = 120k\Omega$$

For a negative output voltage,

$$V_{OUT} = V_{OUT(MIN)} + (V_{FB} - V_{DACOUT}) \times R2 / R3.$$

At power-up, the DAC resets to mid-scale where V_{DACOUT} = 0.635V. Therefore, the output voltage after reset is:

$$V_{OUT(MID)} = -12.5 + (0 - 0.635) \times (1.2M) / (120k) = -18.85V$$

Note that for a negative output voltage, $|V_{OUT}|$ increases as V_{DACOUT} increases. $|V_{OUT(MAX)}|$ corresponds to V_{DACOUT} = 1.25V, and $|V_{OUT(MIN)}|$ corresponds to V_{DACOUT} = 0V.

Setting the Output Voltage without the DAC

The MAX686 may be used without the DAC to control the output voltage. For either positive or negative output voltage applications, set the MAX686's output voltage using only two external resistors (R1 and R2) as shown in Figure 1, 2, or 3. Since the input bias current at FB has a 50nA maximum value, large resistors can be used in the feedback loop without a significant loss of accuracy. Select R1 to be in the 10kΩ to 220kΩ range and calculate R2 using the applicable equations from the following subsections.

Setting the Positive Output Voltage

Use the circuit of Figure 1, connecting POL to GND and omitting R3. Connecting POL to GND sets the threshold voltage at FB to V_{REF}. Choose the value of R1 in the 10kΩ to 220kΩ range and calculate R2 as follows:

$$R2 = R1 \times (V_{OUT} / V_{REF} - 1)$$

where V_{REF} = 1.25V.

Setting the Negative Output Voltage

For negative output voltages, configure R1 and R2 as shown in Figures 2 and 3, connecting POL to V_{CC} and omitting R3. Connecting POL to V_{CC} sets the FB threshold voltage to GND for negative output voltages. Choose R1 in the 10kΩ to 220kΩ range and calculate R2 as follows:

$$R2 = R1 \times |V_{OUT}| / V_{REF}$$

where V_{REF} = 1.25V.

Figures 2 and 3 demonstrate two possible methods of generating a negative voltage with the MAX686. In Figure 3, D2 connects to the input supply (V_{IN}). This connection features the best output ripple performance, but $|V_{OUT}|$ must be limited to values less than -27.5V - V_{IN}. If the application requires a larger negative voltage, use the method of Figure 2, connecting D2 to GND. This method allows a maximum output voltage of -27.5V, but $|V_{OUT}|$ must be greater than V_{IN}.

Setting the Peak Inductor Current Limit

External current-limit selection provides added control over the MAX686's output performance. A higher current limit increases the amount of energy stored in the inductor during each cycle, which provides higher output current capability. For higher output current applications, choose the 500mA current-limit option by connecting ISET to V_{CC}. When the load requires lower output current, the 250mA current limit provides several advantages. First, a smaller inductor saves board area and cost. Second, smaller energy transfers per cycle reduce output ripple for a given capacitor. Connecting ISET to GND selects the 250mA current-limit option. Connecting ISET to V_{CC} selects the 500mA current-limit option. Refer to the *Typical Operating Characteristics* for efficiency and load current graphs at each ISET current setting.

Selecting Inductors

The MAX686's high switching frequency allows for the use of a small inductor. The 22µH inductor shown in Figures 1, 2, and 3 is recommended for most applications, although values between 10µH and 47µH are acceptable. Use inductors with a ferrite core or equivalent; powder iron cores are not recommended for use with high switching frequencies. The inductor's incremental saturation rating must exceed the selected current limit. For highest efficiency, use an inductor with a low DC resistance (under 200mΩ). See Table 1 for a list of inductor suppliers.

DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch

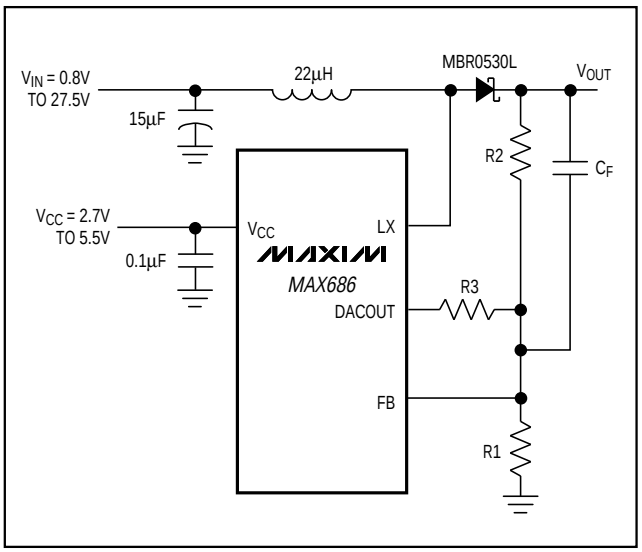


Figure 4. Feed-Forward Capacitor

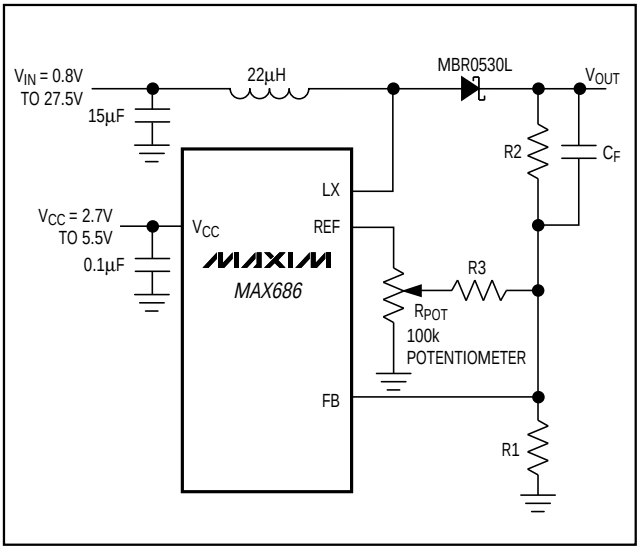


Figure 5. Using a Potentiometer to Adjust Output Voltage

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
CAPACITORS		
AVX: TPS series	(803) 946-0690	(803) 626-3123
Matsuo: 267 series	(714) 969-2491	(714) 960-6492
Sprague 595D series	(603) 224-1961	(603) 224-1430
DIODES		
Motorola: MBR0530L	(602) 303-5454	(602) 994-6430
Nihon; EC11 FS1 series	(805) 867-2555	(805) 867-2698
INDUCTORS		
Coilcraft: DO1608 and DT1608 series	(847) 639-6400	(847) 639-1469
Murata-Erie: LQH4 series	(814) 237-1431	(814) 238-0490
Sumida: CD43, CD54, and CD74 series	(847) 956-0666	(847) 956-0702
TDK: NLC565050 series	(847) 390-4373	(847) 390-4428

Selecting Diodes

The MAX686's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5818 or MBR0530L, are recommended. Make sure that the diode's peak current rating exceeds the peak current set by ISET and that its breakdown voltage exceeds the output voltage. Schottky diodes are preferred due to their low forward voltage. However, ultra-high-speed silicon rectifiers are also acceptable. Table 1 lists Schottky diode suppliers.

Selecting Capacitors

Output Filter Capacitors

The primary selection criterion for the output filter capacitor is low equivalent series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. These requirements can be balanced by appropriately selecting the current limit, as discussed in the *Setting the Peak Inductor Current Limit* section. Table 1 lists some low-ESR capacitor suppliers.

Bypass Capacitors

Although the output current of many MAX686 applications may be relatively small, the input supply must be able to source current transients equal to the ISET current limit. The input bypass capacitor reduces the peak currents drawn from the voltage source and reduces noise caused by the MAX686's switching action. The input source impedance determines the size of the capacitor required at the input (V_{IN}). As with the output filter capacitor, low ESR is the primary consideration. A 15µF, low-ESR capacitor is adequate for most applications, although smaller bypass capacitors may also be acceptable in light-load applications. Bypass the IC separately with a 0.1µF ceramic capacitor placed as close as possible to the V_{CC} and GND pins.

Bypass REF to GND with a 0.1µF ceramic capacitor for REF currents up to 25µA. REF can source up to 50µA of current for external loads. For 25µA ≤ I_{REF} ≤ 50µA, bypass REF with a 0.47µF capacitor.

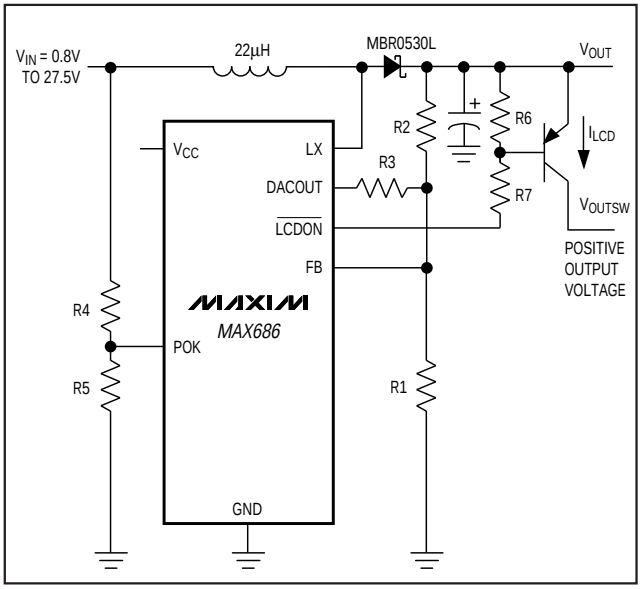


Figure 6. Using the POK for Input Voltage Monitoring

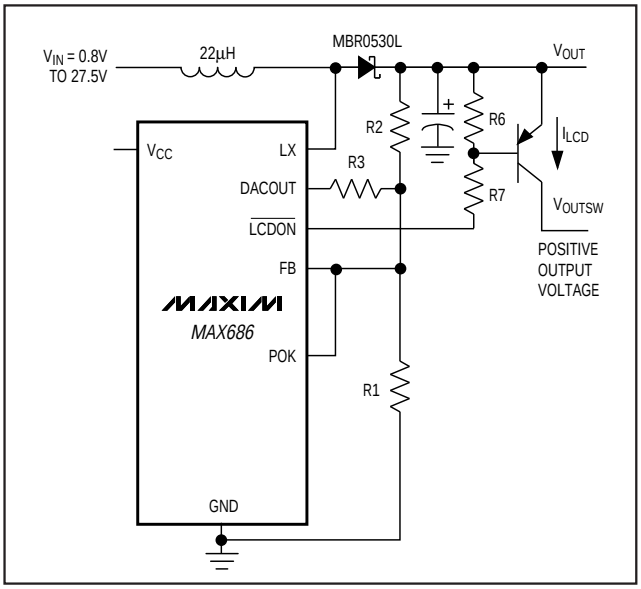


Figure 7. Using the POK for Output Voltage Monitoring

Feed-Forward Capacitors

Parallel a feed-forward capacitor (C_F) across R2 to compensate the feedback loop and ensure stability (Figure 4). Use values up to 100pF for most applications. Choose the lowest capacitor value that ensures stability; high capacitance values may degrade line regulation.

Applications Information

Using a Potentiometer to Adjust the Output Voltage

The output can be adjusted with a potentiometer instead of the DAC (Figure 5). Choose R_{POT} = 100kΩ and connect it between REF and GND. Connect R3 to the potentiometer's wiper instead of to DACOUT. Use the same design equations for adjusting the output voltage with the DAC.

Controlling the LCD Using POK and LCDON

When the voltage at POK is greater than 1.125V (typical), the open-drain LCDON output pulls low. LCDON can withstand up to 27.5V to control an external PNP transistor to switch on the MAX686's positive output (Figures 6 and 7). A PFET can also be used, but a resistor-divider must be used in conjunction with it, so that the PFET does not exceed its V_{GS} rating. Three useful applications of this feature are as follows:

- *An off-switch driver to ensure that a positive boosted output goes to 0V during shutdown.* Connect POK to SHDN. Without this switch, the positive output falls to one diode drop below the input voltage (V_{IN}) in shutdown. LCDON is not needed for negative outputs, which already fall to 0V in shutdown.
- *An input-sensing cutoff for positive outputs.* Connect POK to a voltage divider to sense the input voltage. The output switches on only when the input reaches the set level (Figure 6).
- *An output-sensing cutoff for positive outputs.* Connect POK to the feedback voltage divider to sense the output voltage. The output switches on only when it reaches 90% of the set voltage (Figure 7).

For positive output voltage sensing, connect POK directly to FB to monitor the output voltage (Figure 7). The POK threshold is 10% less than the set voltage at FB. Therefore, when the output voltage drops 10% below its set value, the POK circuit turns off the external PNP transistor, disconnecting the load.

For input voltage sensing, a resistor-divider (R4-R5, Figure 6) from VIN to POK controls the open-drain output LCDON, which pulls low when V_{POK} > 1.125V. Choose R5 = 100kΩ. For example, if the minimum battery voltage is 5.3V, then determine R4 as follows:

$$R4 = R5 \times [(V_{IN} / V_{POK}) - 1]$$
$$= 100k \times [(5.3 / 1.125) - 1] = 371k\Omega$$

LCDON typically drives a low-cost PNP transistor (such as a 2N2907 or equivalent), switching a positive VOUT to the LCD. Choose a PNP with low V_{CESAT} at the required load current. R7 limits the base current in the PNP, and

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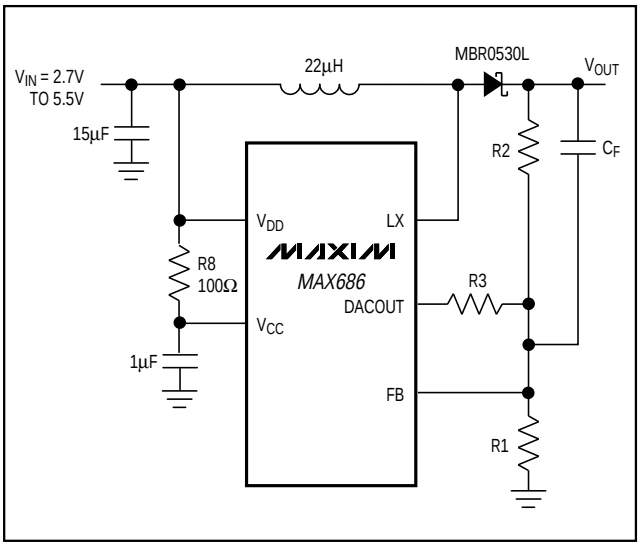


Figure 8. Using a Common Supply-Voltage Source

R6 turns it off when $\overline{LCDON}$ goes high. R6 and R7 can be the same value. Choose R7 such that the minimum base current is greater than 1/50 of the collector current. For example, assume $V_{OUT(MIN)}$ = 12.5V and I_{LCD} = 10mA and then determine R7 as follows:

$$R7 \leq 50 \times (12.5 - 0.7) / 10mA = 59k\Omega$$

Remember that the LCD voltage, V_{OUTSW}, is the regulated output voltage minus the drop across the PNP switch (300mV typ).

Connecting V_{IN} to V_{CC}

The MAX686 (V_{CC}, V_{DD}) and the inductor (V_{IN}) can be powered from the same source as long as the +5.5V V_{CC} maximum limit is not violated. To ensure stability, connect V_{IN} and V_{DD} directly to the source, connect V_{CC} to the source through a 100Ω resistor (R8), and bypass V_{CC} with a 1µF ceramic capacitor as shown in Figure 8. Since the supply current is very small, the voltage drop across R8 is insignificant and does not degrade performance. The RC isolates V_{CC} from the switching noise created by the inductor and internal power switch.

Although, in many cases, the MAX686 and the inductor are powered from the same source, it is often advantageous in battery-powered applications to power the MAX686 IC (V_{CC}, V_{DD}) from an available regulated supply and to power the inductor (V_{IN}) directly from a battery. The MAX686 requires a +2.7V to +5.5V supply at V_{CC}, but the inductor can be powered from voltages as low as 0.8V, significantly increasing usable battery life.

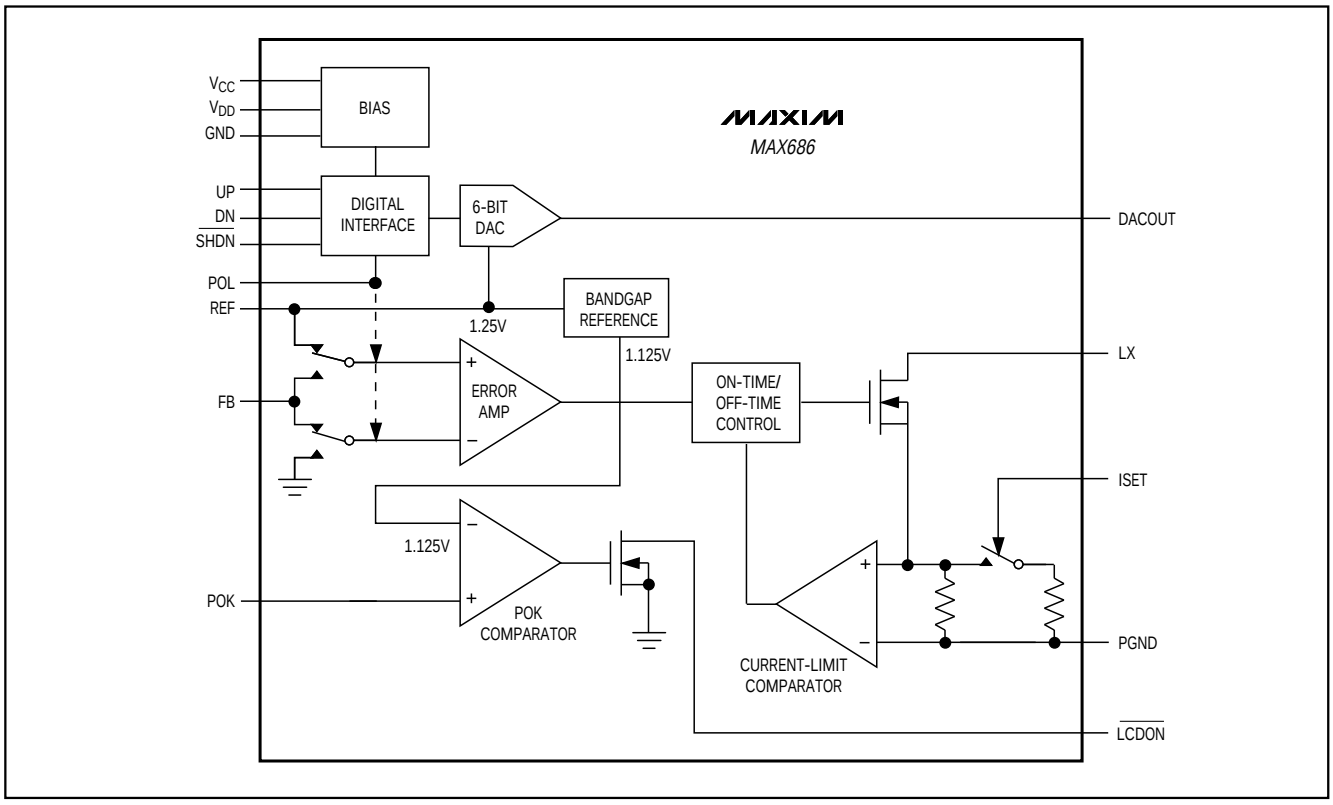
Layout Considerations

Proper PC board layout is essential due to high current levels and fast switching waveforms that radiate noise. It is recommended that initial prototyping be performed using the MAX686 evaluation kit or equivalent PC board-based design. Breadboards or proto-boards should never be used when prototyping switching regulators.

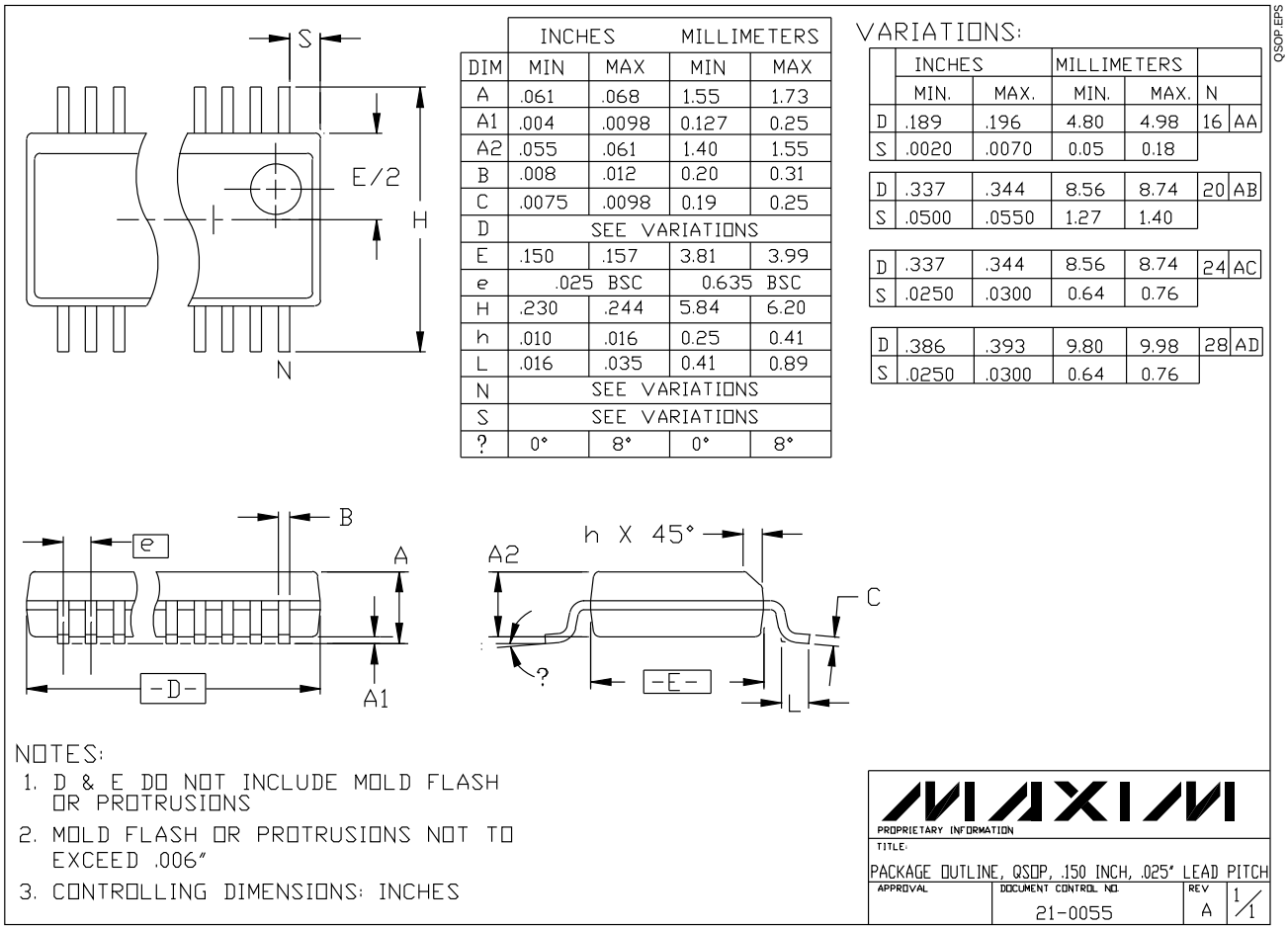
Connect the GND pin, the input bypass-capacitor ground lead, and the output filter-capacitor ground lead to a single point (star ground configuration) to minimize ground noise and improve regulation. Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise, with preference given to the feedback circuit, the ground circuit, and LX. Place R1 and R2 as close to the feedback pin as possible. Place the bypass capacitors as close to the pins as possible.

Refer to the MAX686 evaluation kit data sheet for an example of proper board layout.

Functional Diagram



DAC-Controlled Boost/Inverter LCD Bias Supply with Internal Switch



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
?	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.27	1.40		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.64	0.76		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.64	0.76		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"
3. CONTROLLING DIMENSIONS: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, QSOP, .150 INCH, .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV A | 1/1

Chip Information

TRANSISTOR COUNT: 1325

SUBSTRATE CONNECTED TO GND