MITEL SEMICONDUCTOR

# SA4828

## 3-Phase Pulse Width Modulation Engine

Advance Information

DS4204-2.4 January 1999

The SA4828 PWM engine has been designed to provide waveforms for the control of variable speed AC induction motors, static and uninterruptible power supplies and other forms of electronic equipment which require precise power waveform generation.

The six digital PWM outputs control the six power semiconductors in a three phase inverter bridge, usually via an external isolated gate driver stage.

Information contained within the PWM sequences controls the wave shape, frequency, direction and amplitude of the output waveform and also the phase relationship between each of the outputs. Parameters such as the carrier (switching) frequency, pulse underlap and pulse deletion times may be defined during initialisation of the device to allow the SA4828 to be used with all power semiconductors, irrespective of switching times. The carrier frequency may be selected up to 24kHz to allow silent ultrasonic operation.

The device operates as a stand-alone microprocessor peripheral and it may be controlled by virtually any microprocessor or microcontroller with little or no additional logic. Configuration pins are provided to allow the device to be adapted for most data bus formats, including multiplexed and non-multiplexed data busses and $\overline{RD}/\overline{WR}$ or $R/\overline{W}$ control formats. Microprocessor overhead is kept to a minimum since the device requires intervention only when a change is made to the running conditions. Steady-state operation imposes no microprocessor overhead.

The PWM implementation is fully digital, giving predictable accuracy and temperature stability in hostile environments which are common to motor drive applications. An internal ROM holds the power waveforms in compressed form. Fully digital operation also provides for operation at or around zero speed, enabling DC injection braking to be implemented.

Rotational frequency is defined to 16 bits, giving a resolution better than 0.05 rpm for a two pole motor running at 3000rpm.

The effective rms amplitude of each of the three phases may be controlled individually if required. This allows compensation of unbalanced loads which is particularly useful with static inverter and uninterruptible power supplies. In addition the independent amplitude control can be used to create two phase output for use in single phase induction motor controllers.

Three power waveforms are provided to cover various applications: pure sinusoid, Triplen and Deadbanded Triplen for reduced switching losses.

The SA4828 is implemented on sub-micron CMOS technology for low power consumption. It is available with an Industrial temperature range, and in either DIL or SOIC plastic packages.

Note:- For simplicity reference is made throughout to "motor" but comments can equally apply to power supply inverters.

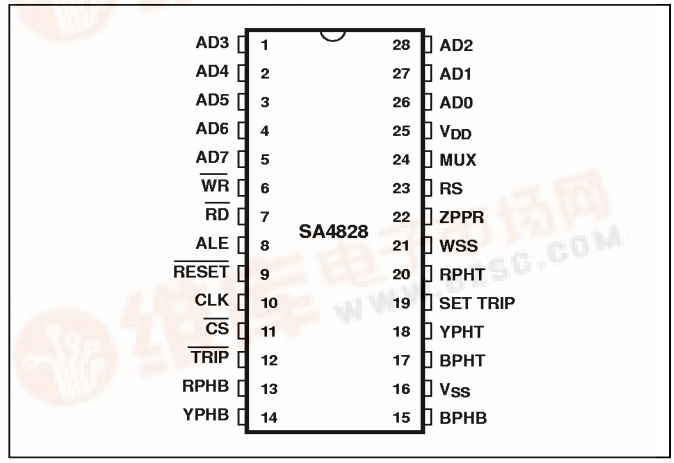



*Fig.1 Pin connections (top view)*

## FEATURES

- Fully Digital Operation
- Configurable Microprocessor Interface
- Power Frequency Range up to 4kHz
- 16-Bit Speed Control Resolution
- Carrier Frequency Selectable up to 24kHz
- Three Selectable Power Waveforms held in Internal ROM
- Selectable Minimum Pulse Width and Underlap Time
- Separate Amplitude Registers for Unbalanced Load Compensation
- Deadbanding Technique to Reduce Losses in Power Semiconductors
- Watchdog Timer
- Boot-strapped Driver Precharge

## APPLICATIONS

- Three Phase Induction Motor Speed Controllers
- Uninterruptible Power Supplies
- Static Inverter Power Supplies
- Power Waveform Generators

## ORDERING INFORMATION

**SA4828/IG/DP1S** 28 lead plastic dual-in-line package, industrial temp range.

**SA4828/IG/MP1S** 28 lead plastic small-outline package, industrial temp range.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{DD}$ | 7V |
| Voltage on any pin | $V_{SS}$ –0.5V to $V_{DD}$ +0.5V |
| Storage temperature | –55°C to 150°C |
| Operating temperature (industrial) | –40°C to 85°C |

The temperature ranges quoted apply to all package types. Many package types are available and extended temperature ranges can be offered for some. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the devices at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

All characteristics are quoted for $V_{DD}$ = 5V ± 10% and $T_{amb}$ = 25˚C unless otherwise stated.

| Characteristic | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2 | - | - | V | - |
| Input low voltage | $V_{IL}$ | - | - | 0.8 | V | - |
| Input low current | $I_{IL}$ | | | | | $V_{IN}$ = $V_{SS}$, $V_{DD}$ = 5.5V |
| SET TRIP inputs | | –1.0 | - | 1.0 | µA | |
| RS, MUX inputs | | –25 | - | –66 | µA | |
| All other inputs | | - | - | 10 | µA | |
| Input high current | $I_{IH}$ | | | | | $V_{IN}$ = $V_{DD}$= 5.5V |
| SET TRIP inputs | | 22 | - | 66 | µA | |
| RS, MUX inputs | | –1.0 | - | 1.0 | µA | |
| All other inputs | | - | - | 10 | µA | |
| Output high voltage | $V_{OH}$ | 4.0 | 4.5 | - | V | $I_{OH}$ = –12mA. Phase outputs and $\overline{TRIP}$ |
| Output low voltage | $V_{OL}$ | - | 0.2 | 0.4 | V | $I_{OH}$ = 12mA. Phase outputs and $\overline{TRIP}$ |
| Output high voltage | $V_{OH}$ | 4.0 | 4.5 | - | V | $I_{OH}$ = –2mA. All other outputs |
| Output low voltage | $V_{OL}$ | - | 0.2 | 0.4 | V | $I_{OH}$ = 2mA. All other outputs |
| Supply current (static) | $I_{DD\ (static)}$ | - | - | 500 | µA | All outputs open circuit |
| Supply current (dynamic) | $I_{DD\ (dynamic)}$ | - | (TBD) | (TBD) | µA | $f_{CLK}$ = 25MHz |
| Supply voltage | $V_{DD}$ | 4.5 | 5.0 | 5.5 | V | - |
| Clock frequency | $f_{CLK}$ | - | - | 25 | MHz | - |
| Clock duty cycle | $D_{CLK}$ | 40 | - | 60 | % | - |
| SET TRIP = 0 → outputs tripped | $t_{TRIP}$ | $3/f_{CLK}$ | - | $4/f_{CLK}$ | µs | $f_{CLK}$ = in MHz |
| → $\overline{TRIP}$ = 0 | | $3/f_{CLK}$ | - | $4/f_{CLK}$ | µs | $f_{CLK}$ = in MHz |

Note 1: For microprocessor interface timings, see figs. 4 - 7.

## PIN DESCRIPTIONS

| Pin No. | Name | Type | Function | Pin No. | Name | Type | Function |
|---|---|---|---|---|---|---|---|
| 1 | AD3 | I | Address/Data | 15 | BPHB | O | Blue Phase (Bottom Switch) |
| 2 | AD4 | I | Address/Data | 16 | $V_{SS}$ | P | 0V Power Supply |
| 3 | AD5 | I | Address/Data | 17 | BPHT | O | Blue Phase (Top Switch) |
| 4 | AD6 | I | Address/Data | 18 | YPHT | O | Yellow Phase (Top Switch) |
| 5 | AD7 | I | Address/Data (MSB) | 19 | SET TRIP | I | Set Output Trip; |
| 6 | $\overline{WR}$ (R/$\overline{W}$) | I | Write Strobe (Read/$\overline{Write}$) | | | | active high; internal pull down |
| 7 | $\overline{RD}$ (DS) | I | Read Stobe (Data Strobe) | 20 | RHPT | O | Red Phase (Top Switch) |
| 8 | ALE (AS) | I | Address Latch Enable (Address Strobe) | 21 | WSS | O | Waveform Sampling Sync. |
| 9 | $\overline{RESET}$ | I | Hardware Reset; active low | 22 | ZPPR | O | Zero Phase Pulse (Red Phase) |
| 10 | CLK | I | Clock Input | 23 | RS | I | Register Select; internal pull up |
| 11 | $\overline{CS}$ | I | Chip Select; active low | 24 | MUX | I | Bus Select; internal pull up |
| 12 | $\overline{TRIP}$ | O | Trip Status; low = tripped | 25 | $V_{DD}$ | P | Positive Power Supply |
| 13 | RPHB | O | Red Phase (Bottom Switch) | 26 | AD0 | I | Address/Data (LSB) |
| 14 | YPHB | O | Yellow Phase (Bottom Switch) | 27 | AD1 | I | Address/Data |
| | | | | 28 | AD2 | I | Address/Data |

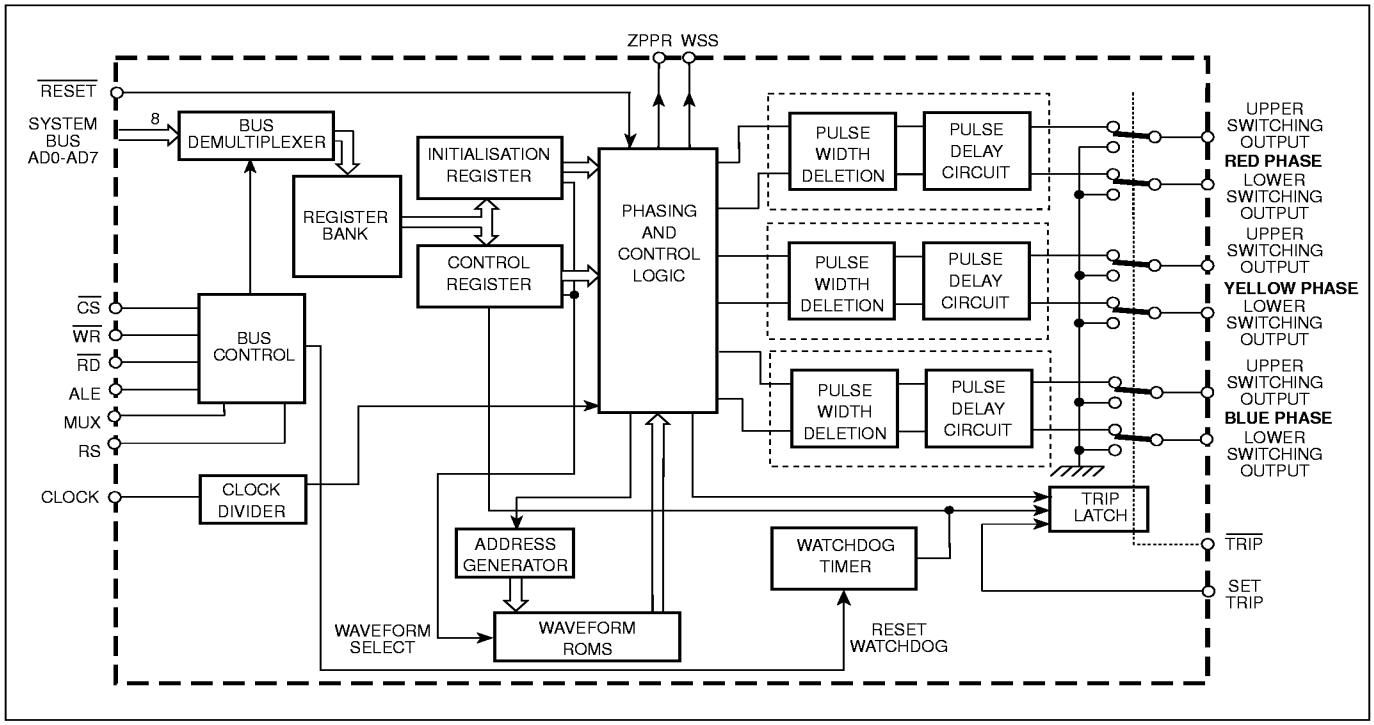



*Fig. 2 SA4828 internal block diagram*

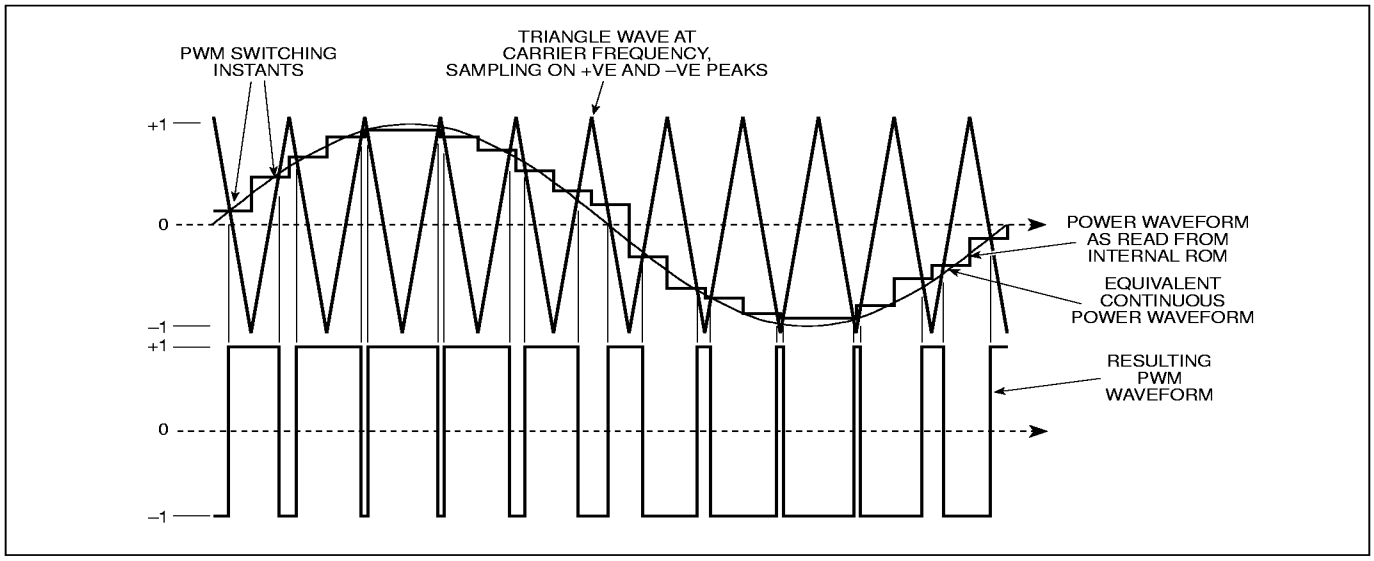



*Fig.3 Asynchronous PWM generation with uniform or 'double-edged' regular sampling as used on the SA4828*

## FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the stored power waveform, as illustrated in Fig. 3. Three standard waveforms exist so that the device may be adapted to particular applications.

In general, a pulse width modulation signal is derived by comparing a signal waveform (in this case the power waveform) with a saw-tooth or triangular carrier waveform of significantly higher frequency. The intersections between the two waveforms in the time domain define the location of transitions in the digital output train and hence the width of the output pulses. The width of the pulses are directly proportional to the magnitude of the power waveform, thus the larger the magnitude, the longer the 'ON' pulse.

The SA4828 uses a digital implementation of this technique which avoids drift problems associated with the use of analogue circuitry. A triangular waveform is synthesised using an up/down counter and a digital comparator used to compare this with the power waveform. The power waveform is sampled regularly at every peak and every trough of the carrier waveform allowing both edges of the PWM output pulse to move in time, hence the term 'double-edged regular sampling.' (A saw-tooth carrier waveform would result in one fixed edge and one moving edge for each PWM pulse).

The power waveform is stored digitally in on-chip ROM (1536 samples per 360˚). The power frequency is controlled by the rate at which the ROM is addressed - a rate which is not related to the carrier frequency on the SA4828, hence the term 'asynchronous method of PWM generation'. The waveform values obtained from the ROM may also be scaled to produce variable voltage amplitude.

Fig. 3 shows the triangular carrier waveform together with the stepped waveform which results from sampling the output of the ROM at the peaks and troughs of the carrier. (A continuous power waveform is also shown for reference). It can be seen that the PWM edges of the waveform (Fig. 3) are obtained at the points where the carrier and the sampled power waveform intersect.

The carrier (switching) frequency is selectable up to 24kHz (assuming a 24.576MHz clock input) enabling ultrasonic switching in noise critical applications.

Power frequency ranges of up to 4kHz are possible with the actual output frequency resolved to 16-bits within the chosen range. This allows for precise motor speed control and smooth frequency changing. Because the SA4828 implementation is entirely digital, operation at (or around) 0Hz is possible without stability or temperature problems. The output phase sequence may be changed to allow both forward and reverse motor operation.

PWM output pulses can be tailored to the inverter characteristics by defining minimum allowable pulse width and the pulse delay (underlap) time without the need for external circuitry. This gives cost savings in terms of the power semiconductor ratings and the size of heatsink required.

Power amplitude control is also provided via three 8-bit registers. By default one register is used to define the amplitude of all three phases. However, by setting the Amplitude Control (AC) bit in the Initialisation Register, the amplitude of each phase may be controlled individually. This allows unbalanced load compensation which is of particular use in static inverter and uninterruptible power supplies and the generation of 2 phase supplies for single phase motors.

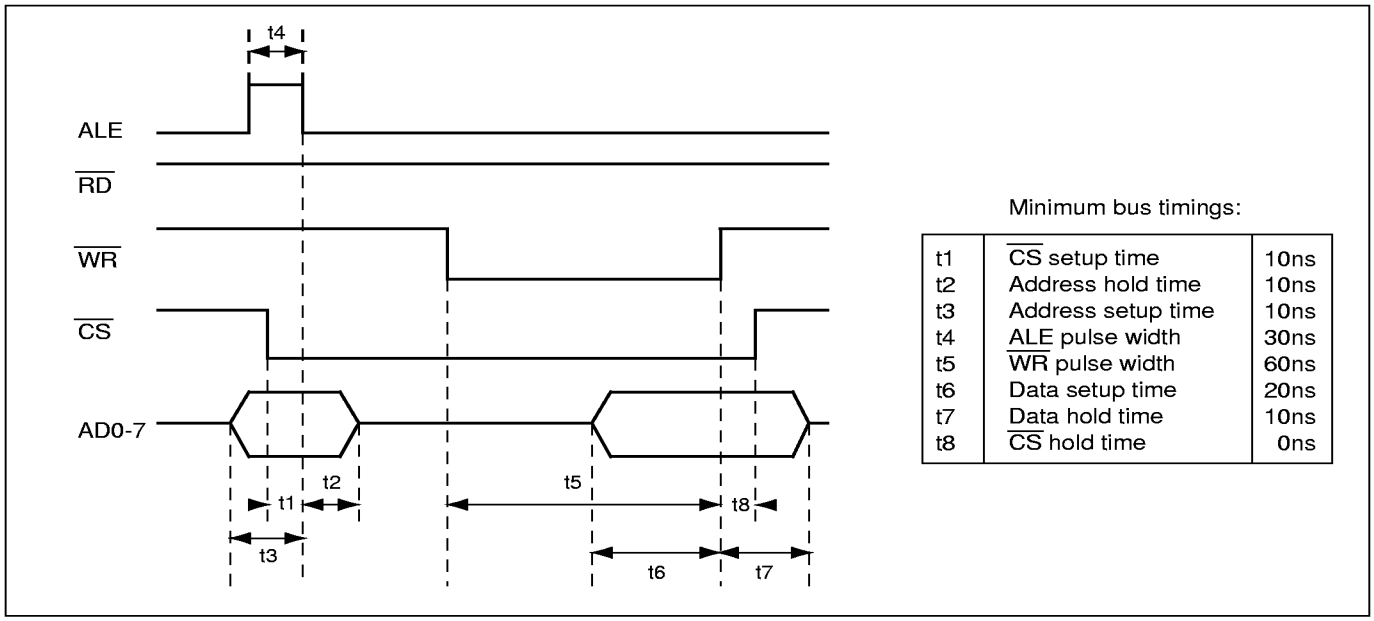
To ensure a robust solution, a trip input allows the PWM outputs to be shut down immediately, overriding microprocessor control in the event of an emergency. This circumvents the delay which a microprocessor interrupt service cycle would inevitably introduce.

A Watchdog Timer function is included. This is intended as a safeguard to trip the device outputs in the event that communications with a controlling processor are lost.

## MICROPROCESSOR INTERFACE

The SA4828 has a parallel write-only interface which is connected to the microprocessor/microcontroller by means of a configurable data bus. This ensures compatibility with virtually all microprocessors/ microcontrollers irrespective of bus width and format and with little or no additional logic.

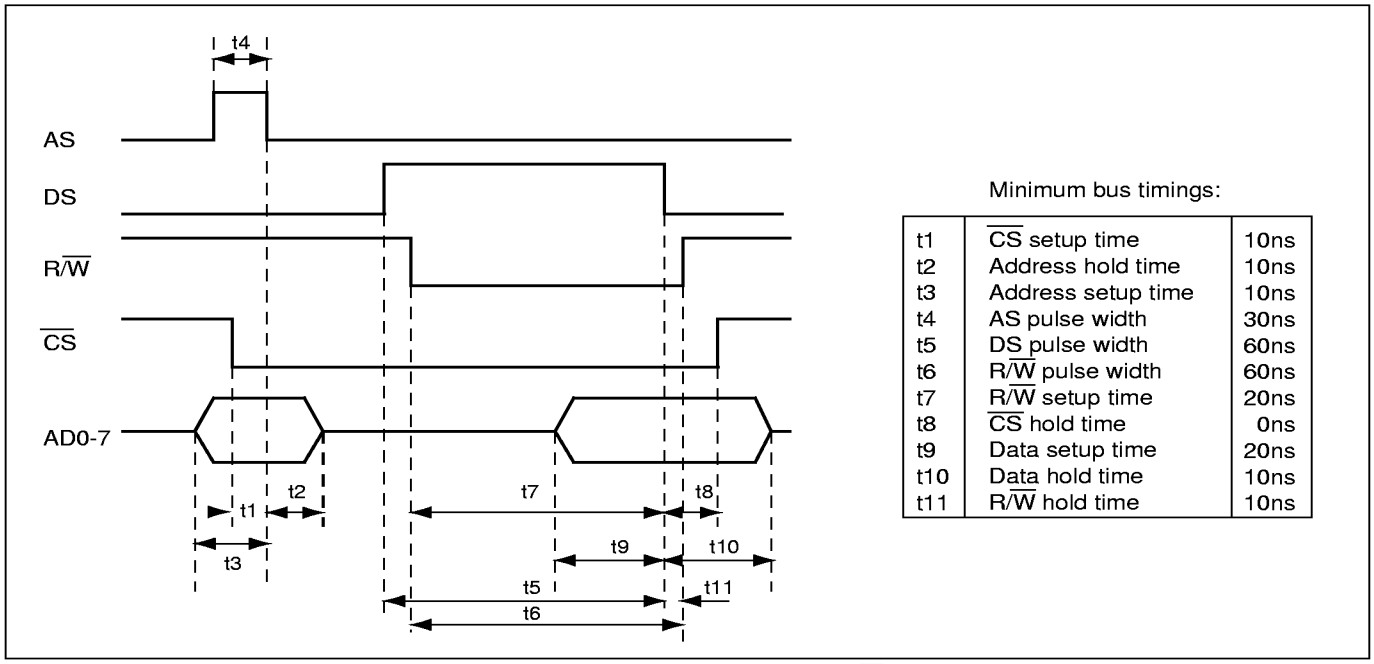
Most data bus formats may be categorised as either having a multiplexed address/ data bus or separate address and data buses. Similarly, most microprocessors have either a $\overline{WR}/\overline{RD}$ or a R/$\overline{W}$ structure. The SA4828 has been designed to operate




Minimum bus timings:

| | | |
|---|---|---|
| t1 | CS setup time | 10ns |
| t2 | Address hold time | 10ns |
| t3 | Address setup time | 10ns |
| t4 | ALE pulse width | 30ns |
| t5 | WR pulse width | 60ns |
| t6 | Data setup time | 20ns |
| t7 | Data hold time | 10ns |
| t8 | CS hold time | 0ns |

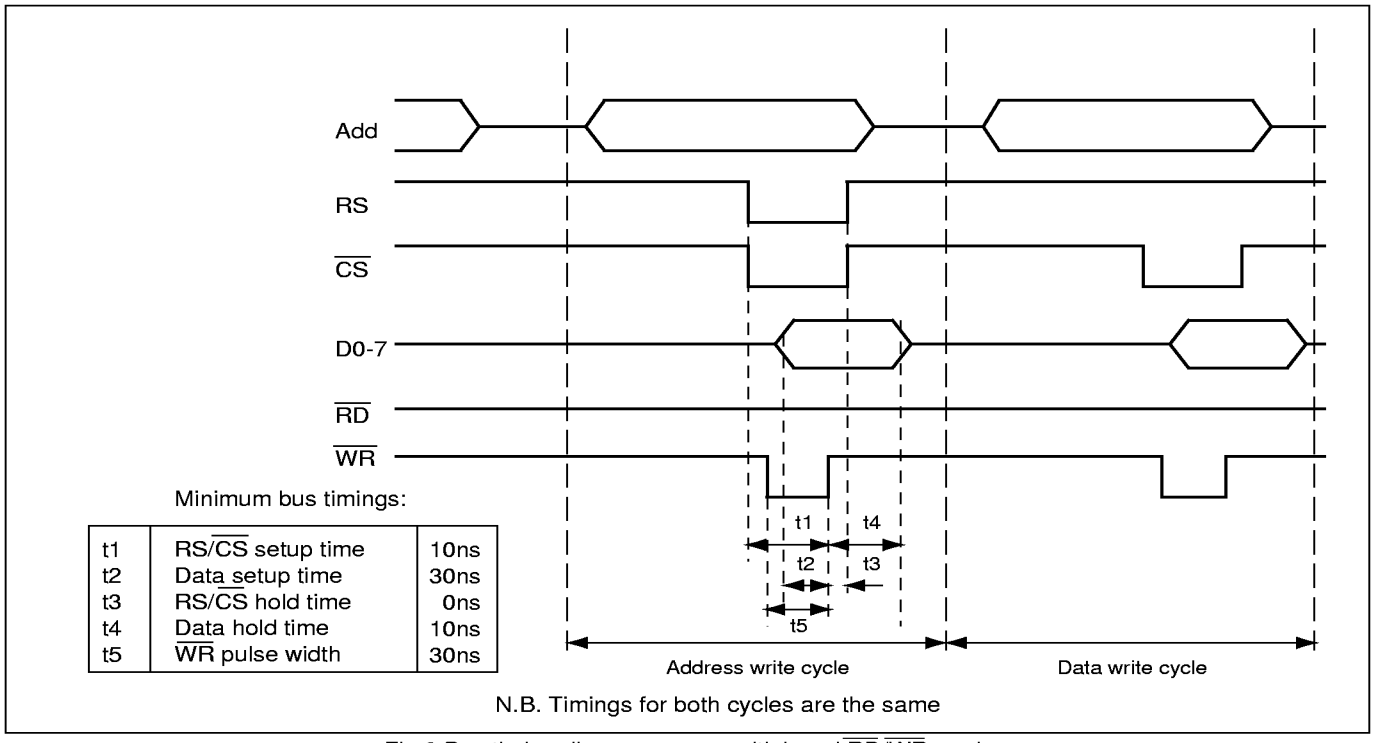
*Fig.4 Bus timing diagram - multiplexed RD/WR mode*




Minimum bus timings:

| | | |
|---|---|---|
| t1 | CS setup time | 10ns |
| t2 | Address hold time | 10ns |
| t3 | Address setup time | 10ns |
| t4 | AS pulse width | 30ns |
| t5 | DS pulse width | 60ns |
| t6 | R/W pulse width | 60ns |
| t7 | R/W setup time | 20ns |
| t8 | CS hold time | 0ns |
| t9 | Data setup time | 20ns |
| t10 | Data hold time | 10ns |
| t11 | R/W hold time | 10ns |

*Fig.5 Bus timing diagram - multiplexed R/W mode*

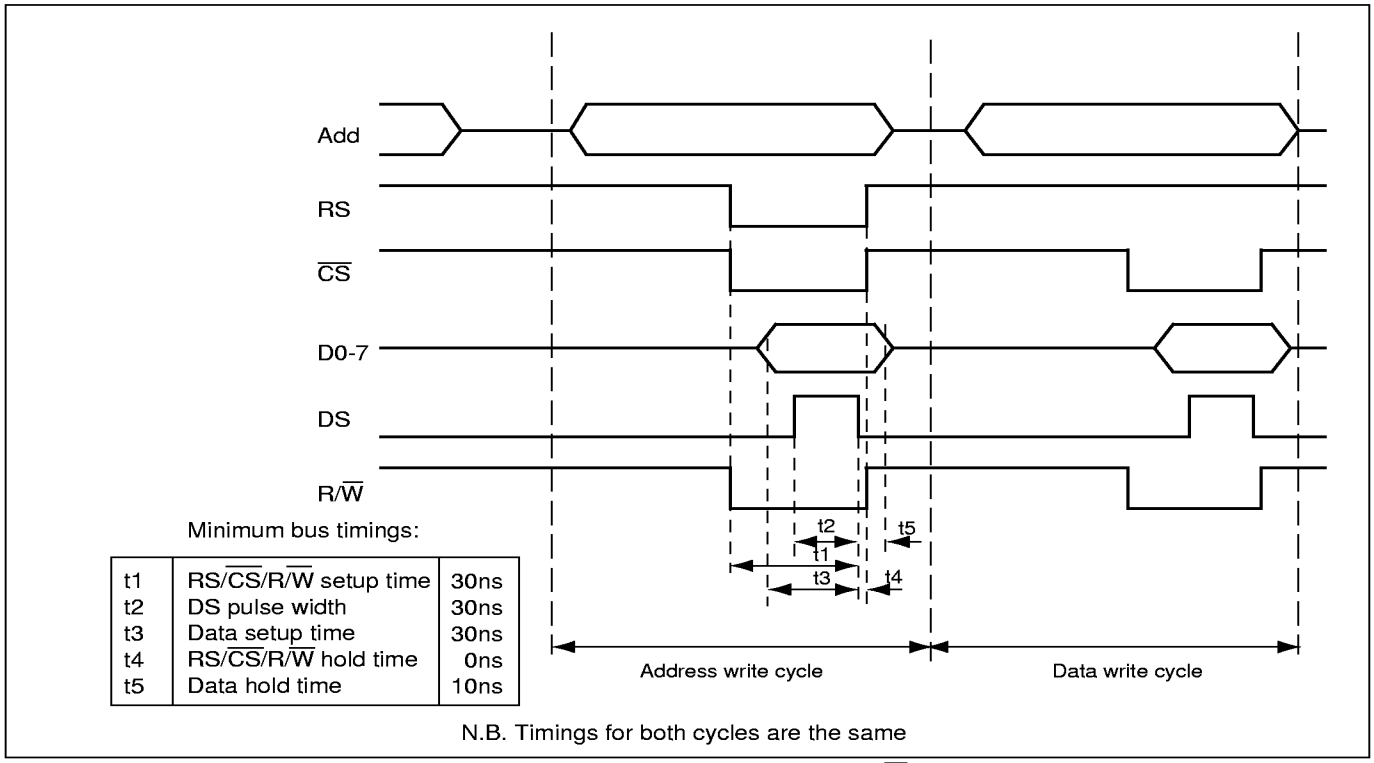



Minimum bus timings:

| | | |
|---|---|---|
| t1 | RS/CS setup time | 10ns |
| t2 | Data setup time | 30ns |
| t3 | RS/CS hold time | 0ns |
| t4 | Data hold time | 10ns |
| t5 | WR pulse width | 30ns |

N.B. Timings for both cycles are the same

*Fig.6 Bus timing diagram - non-multiplexed RD/WR mode*




Minimum bus timings:

| | | |
|---|---|---|
| t1 | RS/CS/R/W setup time | 30ns |
| t2 | DS pulse width | 30ns |
| t3 | Data setup time | 30ns |
| t4 | RS/CS/R/W hold time | 0ns |
| t5 | Data hold time | 10ns |

N.B. Timings for both cycles are the same

*Fig.7 Bus timing diagram - non-multiplexed R/W mode*

with any combination of these four categories.

A configuration pin, MUX, is used to differentiate between multiplexed and non-multiplexed buses. This pin is held at a low logic level for non-multiplexed operation and is either pulled to a high logic level or left floating for multiplexed operation (by virtue of an internal pull-up resistor).

A further signal, named Register Select (RS) is used while in non-multiplexed bus mode to define whether the incoming byte is address (0) or data (1). It is pulled high via an internal resistor so that it need not be connected in multiplexed mode. It is ordinarily connected to an address line in non-multiplexed mode.

In addition to these signals, the SA4828 automatically adjusts itself to the format of the bus control signals. During each write cycle, an internal detection circuit determines whether the $\overline{RD}/\overline{WR}$ or R/$\overline{W}$ format is being used and automatically adapts the SA4828 to suit. A chip select ($\overline{CS}$) pin is also provided to allow the device to share the same bus as other peripherals.

The interface operates as follows:

(i) Multiplexed mode

Connect MUX to $V_{DD}$ or leave open-circuit. RS is don't care so leave open-circuit or connect to either rail.

The incoming address is latched into the address register during each write cycle on the falling edge of ALE (provided $\overline{CS}$ set-up and hold times are adhered to). Within the same cycle, the data is latched into the temporary registers on the rising edge of $\overline{WR}$ ($\overline{RD}/\overline{WR}$ format) or the falling edge of DS (R/$\overline{W}$ format). This is shown diagramatically in Figs. 4 and 5.

(ii) Non-Multiplexed mode

Connect MUX to $V_{SS}$. Connect RS to any suitable address bit (usually A0). Connect ALE to $V_{SS}$.

This means that any write operation which clears A0 will write the address into the SA4828 and any which sets it will write the corresponding data.

To write to the device in this mode, first perform a write operation to the device such that RS=0 and the data is equal to the required address. As $\overline{WR}$ returns high ($\overline{RD}/\overline{WR}$ format) or DS returns low (R/$\overline{W}$ format) the information is written into the SA4828 address register. Next write the data itself with RS=1. As $\overline{WR}$ returns high (or DS returns low) the data is written into the temporary register dictated by the SA4828 address register.

When RS is connected to the least significant address line, this gives an equivalent memory map of just two locations, the upper one being 'Data' and the lower being 'Address'.

Operation in this mode is shown diagramatically in Figs. 6 and 7.

Industry standard microprocessors such as the 8051, 6805, 68000 and TMS320 may be used with little or no additional circuitry. Since the microprocessor interface is fully static, bus operation may be emulated using port pins- allowing operation with microcontrollers which have no data bus such as the PIC, ST6 and Z86C series.

## CONTROLLING THE SA4828

The SA4828 is controlled by loading data into two 48-bit registers via the microprocessor interface. These are the Initialisation Register and the Control Register. Data is initially loaded into a series of Temporary Registers which are then transferred simultaneously to either of the two registers by means of a dummy write operation.

The Initialisation Register sets up the basic operating parameters associated with the motor and inverter. This would normally be loaded prior to motor operation (i.e. before the PWM outputs are activated) and is not normally updated during motor operation.

The Control Register is used to control the PWM outputs (and hence the motor) during operation. For example, speed, forward/reverse, start and stop. Typically, this register will be written to many times during motor operation in order to achieve motor acceleration etc.

The addressing of the SA4828 registers is shown in table 1.

| AD3 | AD2 | AD1 | AD0 | Register | Comment |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | R0 | Temporary register |
| 0 | 0 | 0 | 1 | R1 | Temporary register |
| 0 | 0 | 1 | 0 | R2 | Temporary register |
| 0 | 0 | 1 | 1 | R3 | Temporary register |
| 0 | 1 | 0 | 0 | R4 | Temporary register |
| 0 | 1 | 0 | 1 | R5 | Temporary register |
| 1 | 1 | 1 | 0 | R14 | Transfers initialisation data |
| 1 | 1 | 1 | 1 | R15 | Transfers control data |

*Table 1 SA4828 register addressing*

Since the width of the microprocessor interface is restricted to 8 bits, data is initially loaded into a series of six Temporary Registers, named R0, R1....R5. This data is then transferred simultaneously to either the Initialisation or Control Register. New data is only acted upon once it has been transferred.

Transfer of data takes place by performing a write operation to a 'dummy' register. Writing to Temporary Register 14 transfers the data to the Initialisation Register. Similarly, writing to Temporary Register 15 transfers the data to the Control Register. The data written to Registers 14 and 15 is irrelevant since these are not physically implemented registers, but the write cycle must be completed in order to transfer the data.

## INITIALISATION REGISTER FUNCTIONS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **R0** | FRS2 | FRS1 | FRS0 | X | X | CFS2 | CFS1 | CFS0 |
| **R1** | X | PDT6 | PDT5 | PDT4 | PDT3 | PDT2 | PDT1 | PDT0 |
| **R2** | X | X | PDY5 | PDY4 | PDY3 | PDY2 | PDY1 | PDY0 |
| **R3** | X | X | AC | O | O | X | WS1 | WS0 |
| **R4** | WD15 | WD14 | WD13 | WD12 | WD11 | WD10 | WD9 | WD8 |
| **R5** | WD7 | WD6 | WD5 | WD4 | WD3 | WD2 | WD1 | WD0 |

*Table 2 Initialisation register allocation*

The Initialisation Register data is loaded in 8-bit bytes into Temporary Registers R0-R5. It may be transferred to the Initialisation Register by writing 'dummy' data to Temporary Register R14.

Note that don't care (X) bits should always be written to ensure code compatibility in the event of future augmentations.

Under normal operation, the contents of this register will be defined during the power up sequence. These parameters are particular to the inverter circuitry used and therefore changing these parameters during motor operation is not recommended. Modifications should be made by first inhibiting the PWM outputs using the $\overline{INH}$ bit in the Control Register, or by asserting the hardware reset.

### Carrier Frequency (CFS)

| R0 | FRS2 | FRS1 | FRS0 | X | X | CFS2 | CFS1 | CFS0 |
|---|---|---|---|---|---|---|---|---|

CARRIER FREQUENCY WORD (3-BIT)
CFS2 = MSB
CFS0 = LSB

Defines the frequency of the triangular waveform to which the power waveform is compared - see Fig. 3. Choice of carrier frequency is largely dependent upon the power semiconductors used in the inverter. Slower devices such as bipolar transistors require a lower carrier frequency whilst fast devices such as MOSFETs and IGBTs may be used at much higher carrier frequencies.

High carrier frequencies are advantageous since they increase waveform resolution, but with increased switching losses in the power semiconductors. Carrier frequencies in excess of about 18kHz are beyond the range of human hearing which helps to eliminate audible noise.

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in table 3.

| CFS word | 111 | 110 | 101 | 100 | 011 | 010 | 001 | 000 |
|---|---|---|---|---|---|---|---|---|
| Value of *n* | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

*Table 3 Values of clock division ratio n*

The carrier frequency, $f_{CARR}$, is then given by:

$$f_{CARR} = \frac{f_{CLK}}{512 \times 2^{n+1}}$$

where $f_{CLK}$ = clock input frequency.

### Power Frequency Range (FRS)

| R0 | FRS2 | FRS1 | FRS0 | X | X | CFS2 | CFS1 | CFS0 |
|---|---|---|---|---|---|---|---|---|

FREQUENCY RANGE WORD (3-BIT)
FRS2 = MSB
FRS0 = LSB

In order to optimise the frequency resolution of the SA4828, the required range of power frequencies may be selected using this parameter. Within the selected range, the frequency may be set with 16-bit resolution. It is recommended that the next higher power frequency range than the maximum required motor frequency is used.

The power frequency range defines the maximum limit of the power frequency. The actual operating power frequency is controlled by the 16-bit Power Frequency Select (PFS) word in the Control Register but it may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency ($f_{CARR}$) and a multiplication factor *m*, determined by the 3-bit FRS word. The value of *m* is determined as shown in Table 4.

| FRS word | 110 | 101 | 100 | 011 | 010 | 001 | 000 |
|---|---|---|---|---|---|---|---|
| Value of *m* | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

*Table 4 Values of clock division ratio m*

The power frequency range, $f_{RANGE}$, is then given by:

$$f_{RANGE} = \frac{f_{CARR} \times 2^{m}}{384}$$

where $f_{CARR}$ = carrier frequency

### Pulse Delay Time (Underlap) (PDY)

| R2 | X | X | PDY5 | PDY4 | PDY3 | PDY2 | PDY1 | PDY0 |
|---|---|---|---|---|---|---|---|---|

PULSE DELAY WORD (6-BIT)
PDY5 = MSB
PDY0 = LSB

For each output phase there are two PWM control signals-controlling the upper and lower switches in the inverter. In theory, these two control signals are always complementary. However, due to the finite and non-equal turn-on and turn-off times of power semiconductors, it is necessary to provide a short time during which both outputs are off in order to avoid a transient short through the two devices.

The length of this 'underlap' period is dependent upon the technology of the power semiconductors. Again, slow devices such as bipolar transistors require a longer underlap time whilst faster devices require a shorter time.

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an amount. The pulse delay time is a function of the carrier waveform frequency and PDY, defined by the 6-bit pulse delay time select word. The value of pdy is selected as shown in table 5.

| PDY word | 111111 | 111110 | ...etc... | 000000 |
|---|---|---|---|---|
| Value of *PDY* | 63 | 62 | ...etc... | 0 |

*Table 5 Values of PDY*

The pulse delay time, $t_{pdy}$, is then given by:

$$t_{pdy} = \frac{63 - PDY}{f_{CARR} \times 512}$$

where $f_{CARR}$ = carrier frequency.

Fig.8 shows the effect of pulse delay on a pure PWM waveform.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig.2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by $t_{pd} - t_{pdy}$.

### Pulse Deletion Time (PDT)

| R2 | X | PDT6 | PDT5 | PDT4 | PDT3 | PDT2 | PDT1 | PDT0 |
|---|---|---|---|---|---|---|---|---|

PULSE DELETION WORD (7-BIT)
PDT6 = MSB
PDT0 = LSB

Pure PWM pulse trains contain pulses which vary in duty cycle from 0% to 100%. Therefore pulse widths may become very small indeed. In practice short pulses have no useful purpose since the power semiconductors cannot fully turn on/off within their active period. Such pulses only increase the power dissipation in the power devices.

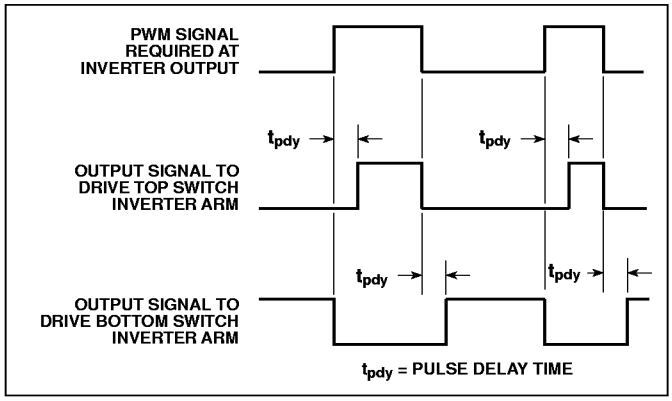



*Fig.8 Effect of pulse delay on PWM pulse train*

Therefore, a minimum pulse width may be defined. All pulses shorter in duration than this are eliminated from the PWM train, whether they are low-going or high-going.

To eliminate short pulses the true PWM train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the Initialisation Register. If a pulse (either positive or negative) is greater in duration than the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, $t_{pd}$, is a function of the carrier wave frequency and PDT, defined by the 7-bit pulse deletion time word. The value of PDT is selected as shown in Table 6.

| **PDT word** | 1111111 | 1111110 | ...etc... | 0000000 |
|---|---|---|---|---|
| **Value of *PDT*** | 127 | 126 | ...etc... | 0 |

*Table 6 Values of PDT*

The pulse deletion time, $t_{pd}$, is then given by:

$$t_{pd} = \frac{127 - PDT}{f_{CARR} \times 512}$$

where $f_{CARR}$ = carrier frequency.

Fig. 9 shows the effect of pulse deletion on a pure PWM waveform.

## Waveform Selection

Three waveforms are included as standard with the SA4828. A pure sine wave is available for applications where waveform purity is important such as static inverter power supplies, uninterruptible power supplies and for driving single or two phase induction motors.

For three phase induction motor control a Triplen waveform is included which provides maximum utilisation of the inverter DC link voltage using a harmonic injection technique. Also for motor control, a Deadbanded Triplen waveform may be selected which in addition to providing DC link voltage boost, acts to reduce the number of switching events in the power semiconductors in order to reduce the switching losses. A symmetrical technique is used to ensure that each power semiconductor benefits to the same degree.

| R3 | X | X | AC | 0 | 0 | X | WS1 | WS0 |
|---|---|---|---|---|---|---|---|---|

WAVEFORM SELECTION BITS

Two bits, WS0 and WS1, in Temporary Register 3 are used to define the power waveform, according to Table 7:

| WS1 | WS0 | Waveform |
|---|---|---|
| 0 | 0 | Sinusoid (default) |
| 0 | 1 | Triplen (harmonic injection) |
| 1 | 0 | Deadbanded Triplen (switching loss reduction) |
| 1 | 1 | Reserved |

*Table 7 Waveform selection*

The waveforms may be described by the following mathematical relationships and are shown graphically in Fig. 10:

Sinusoid:

$f(t) = A \sin(\omega t)$ where $A$ = amplitude, $\omega$ = angular displacement

Triplen:

| f(t) | Valid |
|---|---|
| $f(t) = A(2.\sin(\omega t + 30^\circ) - 1$ | $0^\circ \le \omega t < 60^\circ$ |
| $f(t) = A$ | $60^\circ \le \omega t \le 120^\circ$ |
| $f(t) = A(2.\sin(\omega t - 30^\circ) - 1$ | $120^\circ \le \omega t < 180^\circ$ |
| $f(t) = A(2.\sin(\omega t + 30^\circ) + 1$ | $180^\circ \le \omega t < 240^\circ$ |
| $f(t) = -A$ | $240^\circ \le \omega t \le 300^\circ$ |
| $f(t) = A(2.\sin(\omega t - 30^\circ) + 1$ | $300^\circ \le \omega t < 360^\circ$ |

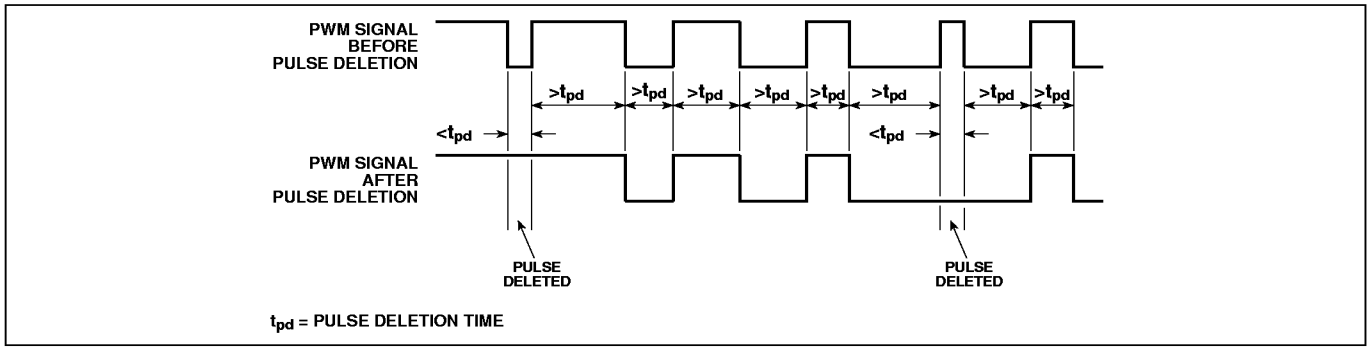



*Fig.9 The effect of the pulse delay deletion circuit*

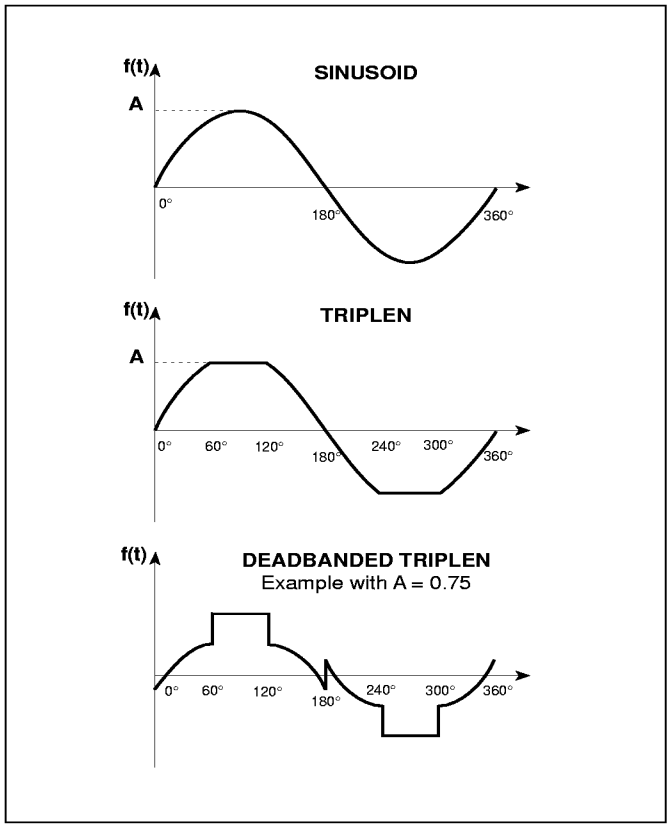



*Fig.10 Waveforms implemented in SA4828*

Deadbanding:
Below are the modulating functions for the Deadbanded Triplen waveform. These have been normalised and scaled to give a peak line voltage (phase to phase) of 2A. All the 3 phases are shown for clarity, f(t), g(t) and h(t).

| Function | Valid |
|---|---|
| $f(t) = 2A.\ sin(\omega t + 30^\circ) - 1$<br>$g(t) = -1$<br>$h(t) = 2A.\ sin(\omega t + 90^\circ) - 1$ | $0^\circ < \omega t \leq 60^\circ$ |
| $f(t) = 1$<br>$g(t) = 1 + 2A.\ sin\ (\omega t - 150^\circ)$<br>$h(t) = 1 + 2A.\ sin(\omega t + 150^\circ)$ | $0^\circ < \omega t \leq 120^\circ$ |
| $f(t) = 2A.\ sin(\omega t - 30^\circ) - 1$<br>$g(t) = 2A.\ sin(\omega t - 90^\circ) - 1$<br>$h(t) = -1$ | $120^\circ < \omega t \leq 180^\circ$ |
| $f(t) = 1 + 2A.\ sin(\omega t + 30^\circ)$<br>$g(t) = 1$<br>$h(t) = 1 + 2A.\ sin(\omega t + 90^\circ)$ | $180^\circ < \omega t \leq 240^\circ$ |
| $f(t) = -1$<br>$g(t) = 2A.\ sin(\omega t - 150^\circ) - 1$<br>$h(t) = 2A.\ sin(\omega t + 150^\circ) - 1$ | $240^\circ < \omega t \leq 300^\circ$ |
| $f(t) = 1 + 2A.\ sin(\omega t - 30^\circ) - 1$<br>$g(t) = 1 + 2A.\ sin(\omega t - 90^\circ) - 1$<br>$h(t) = 1$ | $300^\circ < \omega t \leq 360^\circ$ |

Line output voltages appearing across the load are:
Vfg = f(t) – g(t)
Vgh = g(t) – h(t)
Vhf = h(t) – f(t)

The line voltage waveforms are sinusoidal.

## Amplitude Control (AC)

| R3 | X | X | AC | 0 | 0 | X | WS1 | WS0 |
|---|---|---|---|---|---|---|---|---|

AMPLITUDE CONTROL BIT

This is a single bit, AC in Temporary register 3, which controls the amplitude control mode for each of the three phases. When the AC bit is cleared the red Amplitude byte in the Control Register is used to define the amplitude of all three phases. When the AC bit is set, the individual Amplitude bytes, Red, Yellow and Blue in the Control Register are used to define the amplitudes of the respective phases.

## Watchdog Timer (WD)

| R4 | WD15 | WD14 | WD13 | WD12 | WD11 | WD10 | WD9 | WD8 |
|---|---|---|---|---|---|---|---|---|
| R5 | WD7 | WD6 | WD5 | WD4 | WD3 | WD2 | WD1 | WD0 |

WATCHDOG COUNTER WORD (16-BIT)
WD15 = MSB
WD0 = LSB

The Watchdog Timer consists of a 16-bit programmable counter, which is decremented at a sub-multiple of the $f_{CLK}$ frequency. If the counter is allowed to reach its terminal condition (time-out), then the PWM outputs are set to the off (low) state and the $\overline{TRIP}$ output asserted low.

Initialisation temporary registers R4 and R5 are used to transfer the initial data for the 16-bit Watchdog programmable counter. Register R4 is the most significant byte (MSB). The programmable counter is reset to its initial value every time a write is made to the Control register.

The time-out period $t_{wd}$, is given by the formula:

$$t_{wd} = \frac{\text{TIM x } 1024}{f_{CLK}}$$

Where TIM is the equivalent decimal value of the 16-bit binary number loaded to registers R4 and R5, 0 < TIM < 65535. This gives a time-out range of 41µs < $t_{wd}$ < 2.68s at 25MHz master clock.

When the Watchdog times out a $\overline{TRIP}$ condition is activated, (see SET TRIP). This state can only be cleared by application of a Reset signal, (either hardware or software).

The Watchdog Timer function is always disabled following a hardware or software reset. It is enabled by setting the WTE bit in the Control Register to an active logic 1 level. If the Watchdog function is not required the WTE bit should be set to logic 0.

## CONTROL REGISTER FUNCTIONS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **R0** | PFS7 | PFS6 | PFS5 | PFS4 | PFS3 | PFS2 | PFS1 | PFS0 |
| **R1** | PFS15 | PFS14 | PFS13 | PFS12 | PFS11 | PFS10 | PFS9 | PFS8 |
| **R2** | RST | X | X | X | WTE | $\overline{CR}$ | $\overline{INH}$ | $\overline{F}$/R |
| **R3** | RAMP7 | RAMP6 | RAMP5 | RAMP4 | RAMP3 | RAMP2 | RAMP1 | RAMP0 |
| **R4** | BAMP7 | BAMP6 | BAMP5 | BAMP4 | BAMP3 | BAMP2 | BAMP1 | BAMP0 |
| **R5** | YAMP7 | YAMP6 | YAMP5 | YAMP4 | YAMP3 | YAMP2 | YAMP1 | YAMP0 |

*Table 8 Control register allocation*

The Control Register data is loaded in 8-bit bytes into Temporary Registers R0-R5. It may be transferred to the Control Register by writing 'dummy' data to Temporary Register R15.

Note that don't care (X) bits should always be written to logic 0 to ensure code compatibility in the event of future product augmentations.

### Power Frequency (PFS)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **R0** | PFS7 | PFS6 | PFS5 | PFS4 | PFS3 | PFS2 | PFS1 | PFS0 |
| **R1** | PFS15 | PFS14 | PFS13 | PFS12 | PFS11 | PFS10 | PFS9 | PFS8 |

POWER FREQUENCY WORD (16-BIT)
PFS15 = MSB
PFS0 = LSB

The power frequency is selected as a proportion of the power frequency range (defined in the Initialisation Register) by the 16-bit power frequency select word, PFS, allowing the power frequency to be defined in 65536 equal steps. As the PFS word spans the two temporary registers R0 and R1 it is essential, when changing the power frequency, that both these registers are updated before writing to R15.

The power frequency ($f_{POWER}$) is given by:

$$f_{POWER} = \frac{f_{RANGE}}{65536} \times PFS$$

where PFS = decimal value of the 16-bit PFS word and $f_{RANGE}$ = power frequency range set in the Initialisation Register.

### Power Frequency Amplitude (RAMP, YAMP, BAMP)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **R3** | RAMP7 | RAMP6 | RAMP5 | RAMP4 | RAMP3 | RAMP2 | RAMP1 | RAMP0 |
| **R4** | BAMP7 | BAMP6 | BAMP5 | BAMP4 | BAMP3 | BAMP2 | BAMP1 | BAMP0 |
| **R5** | YAMP7 | YAMP6 | YAMP5 | YAMP4 | YAMP3 | YAMP2 | YAMP1 | YAMP0 |

AMPLITUDE WORDS (3x 8-BIT)
RAMP7, BAMP7, YAMP7 = MSB
RAMP0, BAMP0, YAMP0 = LSB

This defines the effective rms amplitude of the output PWM signals. In a motor application this allows the voltage/frequency (flux) relationship to be defined.

The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the internal ROM by the value of the 8-bit amplitude select words (RAMP, YAMP and BAMP).

The percentage amplitude control for each phase is given by:

$$\text{Power Amplitude (\%)}, A_{POWER} = \frac{A}{255} \times 100$$

where $A$ = integer value of 8-bit amplitude select word.

Note that the Amplitude Control (AC) bit in the Initialisation Register determines whether the Red Amplitude register value is used for all three phases, or if they are controlled independently.

### Forward/Reverse ($\overline{F}$/R)

| R2 | RST | X | X | X | WTE | $\overline{CR}$ | $\overline{INH}$ | $\overline{F}$/R |
|---|---|---|---|---|---|---|---|---|

FORWARD/REVERSE BIT

The phase sequence of the three-phase PWM output waveforms is controlled by the Forward/Reverse bit $\overline{F}$/R.

The actual effect of changing this bit from 0 (forward) to 1 (reverse) is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it. The required output waveforms are all continuous with time during a forward/reverse change.

In the forward mode the output phase sequence is red-yellow-blue and in the reverse mode the sequence is blue-yellow-red.

### Output Inhibit ($\overline{INH}$)

| R2 | RST | X | X | X | WTE | $\overline{CR}$ | $\overline{INH}$ | $\overline{F}$/R |
|---|---|---|---|---|---|---|---|---|

OUTPUT INHIBIT BIT

When active (i.e., low) the output inhibit bit $\overline{INH}$ sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released it forces the phase bottom outputs to be driven high for a whole carrier cycle before the phase top outputs are enabled.

### Counter Reset ($\overline{CR}$)

| R2 | RST | X | X | X | WTE | $\overline{CR}$ | $\overline{INH}$ | $\overline{F}$/R |
|---|---|---|---|---|---|---|---|---|

COUNTER RESET BIT

This facility allows the internal power frequency phase counter to be set to 0° (red phase) while Counter Reset ($\overline{CR}$) is low. Normal frequency control is suspended; the red phase outputs have 50% duty cycle and yellow and blue phases have duty cycles corresponding to +120° and –120° respectively.

### Watchdog Timer Enable (WTE)

| R2 | RST | X | X | X | WTE | $\overline{CR}$ | $\overline{INH}$ | $\overline{F}$/R |
|---|---|---|---|---|---|---|---|---|

WATCHDOG ENABLE BIT

The Watchdog Timer Enable bit WTE enables the watchdog function when set to an active high level. When WTE is set to a low level the Watchdog function is disabled. The 16-bit Watchdog counter forms part of the Initialisation Register.

### Software Reset

| R2 | RST | X | X | X | WTE | CR | INH | F/R |
|---|---|---|---|---|---|---|---|---|

SOFTWARE RESET BIT

The software reset bit RST provides a facility to reset the device from the microprocessor interface instead of using the RESET pin. When active (high), the chip is put into the same state as that when RESET is asserted except that the RST bit is not itself forced low. The reset condition may be cleared by writing '0' to the RST bit using the microprocessor interface, or by toggling the RESET pin.

## HARDWARE INPUT/OUTPUT FUNCTIONS

### Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry might be used to activate this input.

When the SET TRIP input is taken to a logic high, the output trip latch is activated. This results in the TRIP output and the six PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the RST input.

It is essential that when not in use SET TRIP is tied low and isolated from potential sources of noise; on no account should it be left floating.

SET TRIP is latched internally at the master clock rate in order to reduce noise sensitivity.

### Output Trip Status (TRIP output)

The TRIP output indicates the status of the output trip latch and is active low.

### Reset Operation (RESET input)

Operation of the Hardware Reset, RESET (active low); or Software Reset, RST (active high); performs the following functions:

1. All PWM outputs are forced low (if not already low) thereby turning off the drive switches.
2. All internal counters, (including the Watchdog Timer), are reset. (This corresponds to zero degrees for the red phase output.)
3. The trailing edge of reset sets the TRIP output high - assuming that the SET TRIP input is inactive (i.e. low).

### Default/Reset Conditions

The following default conditions are imposed after a reset:

1. INH = 0. PWM outputs disabled.
2. CR = 0. Internal Counter Reset held active low.
3. WTE = 0. Watchdog Timer is disabled.
4. RST = 0. Software reset is deasserted (assertion of RESET only).

The status of all other bits in the Initialisation and Control Registers remain **unchanged.**

**Notes:**

1. After a reset operation, in order to enable the PWM outputs, the INH bit-1 and the CR bit-2 in Temporary Register R2 must be set to a logic "1" state, and a Write operation to register address R15 performed.
2. Following a reset sequence after power up, in order to prevent spurious operation, it is essential to write known values to the Initialisation and Control Registers before the INH bit is set to a logic "1" state. (See Fig.12 Programming example.)
3. Following any other reset sequence it should be noted that PFS and the AMP registers are not cleared and it may be desirable to write to these registers before INH and CR bits are set to logic 1.

### Zero Phase Pulse (ZPPR output)

The zero phase pulse output provides a signal at the same frequency as the power frequency with a 1 : 2 mark-space ratio. When in the forward mode of operation the falling edge of ZPPR corresponds to 0° for the red phase. In the reverse mode, the rising edge of ZPPR corresponds to 0° for the red phase.

### Waveform Sampling Synchronisation (WSS output)

The WSS output is derived from the LSB of the waveform ROM address generator and toggles once every ROM address. There are a total of 768 rising and 768 falling edges output over a complete power frequency cycle. Note that because the ROM is addressed at a rate controlled by a digital rate generator, the edges are not equispaced.

### Clock (CLK input)

The CLK input provides a timing reference used by the SA4828 for all timings related to the PWM outputs.

The microprocessor interface, however, derives all its timings from the microprocessor and therefore the microprocessor and the SA4828 may be run either from the same or from different clocks.

## SA4828 PROGRAMMING EXAMPLE

The following example assumes that a master clock of 24.576 MHz is used. This clock frequency will allow a maximum carrier frequency of 24 kHz and a maximum power frequency of 4 kHz.

### Initialisation Register Programming Example

A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10µs and an underlap of 5µs. The Triplen waveform is required and common amplitude control should be used across all three phases.

### 1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency.

Calculate the value of *n* that will give the required carrier frequency:

$$f_{CARR} = \frac{f_{CLK}}{512 \times 2^{n+1}}$$

$$\Rightarrow 2^{n+1} = \frac{f_{CLK}}{512 \times f_{CARR}} = \frac{24.576 \times 10^6}{512 \times 6 \times 10^3} = 8$$

$\Rightarrow \underline{n = 2}$

From Table 3, $n = 2$ corresponds to a 3-bit CFS word of 010 in temporary register R0.

### 2. Setting the power frequency range

Calculate the value of $m$ that will give the required power frequency:

$$f_{RANGE} = \frac{f_{CARR} \times 2^m}{384}$$

$$\Rightarrow 2^m = \frac{f_{RANGE} \times 384}{f_{CARR}} = \frac{250 \times 384}{6 \times 10^3} = 16$$

$$\Rightarrow \underline{m = 4}$$

From Table 4, $m = 4$ corresponds to a 3-bit FRS word of 100 in temporary register R0.

### 3. Setting the pulse delay time

Calculate the value of PDY that will give the required pulse delay time:

$$t_{pdy} = \frac{(63 - PDY)}{f_{CARR} \times 512}$$

$$\Rightarrow PDY = 63 - (t_{pdy} \times f_{CARR} \times 512)$$

$$\Rightarrow 63 - ((5 \times 10^{-6}) \times (6 \times 10^3) \times 512) = 47.64$$

However, the value of PDY must be an integer. As the purpose of the pulse delay is to prevent 'shoot-through' (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, assigning the value 47 to PDY gives a delay time of 5·2µs. From Table 5, PDY = 47 corresponds to a 6-bit PDY word of 101111 in temporary register R2.

### 4. Setting the pulse deletion time

In setting pulse deletion time (i.e., the minimum pulse width) account must be taken of the pulse delay time, as the actual minimum pulse width seen at the PWM outputs is equal to $t_{pd} - t_{pdy}$.

Therefore, the value of the pulse deletion time must, in this instance, be set 5.2µs longer than the minimum pulse length required.

Minimum pulse length required = 10µs

$\therefore t_{pd}$ to be set to 10µs + 5.2µs = 15.2µs

Now,

$$t_{pd} = \frac{127 - PDT}{f_{CARR} \times 512}$$

$$\Rightarrow PDT = 127 - (t_{pd} \times f_{CARR} \times 512)$$

$$\Rightarrow 127 - ((15.2 \times 10^{-6}) \times (6 \times 10^3) \times 512) = 80.30$$

Again, PDT must be an integer and so must be either rounded up or down – the choice of which will depend on the application. Choosing in this case the value 80 for PDT, gives a value of $t_{pd}$ of 15.3µs.

From Table 6, PDT = 80 corresponds to a value of PDT, the 7-bit word in temporary register R1 of 1010000.

### 5. Setting waveform select, amplitude control etc.

The Triplen waveform is selected by setting WS0 = 1 and WS1 = 0.

Common amplitude control is required across the three phases. This is selected by setting AC = 0. Hence Temporary Register R3 should be set to 00000001.

### 6. Setting Watchdog Timer Counter.

This function is disabled so temporary registers R4 and R5 can be set to all zero.

### Control Register Programming Example

The control register would normally be updated many times while the motor is running, but just one example is given here. It is assumed that the Initialisation Register has already been programmed with the parameters given in the previous example.

A power waveform of 100Hz is required with a PWM waveform amplitude of 80% of that stored in the ROM across all three phases. The phase sequence should be set to give forward motor rotation. The outputs should be enabled.

### 1. Setting the power frequency

The power frequency, $f_{POWER}$, can be selected to 16-bit accuracy (i.e 65536 equal steps) from 0Hz to $f_{RANGE}$ as defined in the Initialisation Register. In this case, with $f_{RANGE}$ = 250Hz, the power frequency can be adjusted in increments of 0·0038Hz.

$$f_{POWER} = \frac{f_{RANGE}}{65536} \times PFS$$

$$\Rightarrow PFS = \frac{f_{POWER} \times 65536}{f_{RANGE}} = \frac{100 \times 65536}{250} = 26214.4$$

PFS must be an integer, so assigning a value of 26214 gives $f_{POWER}$ = 99.998 Hz.The 16-bit binary equivalent of this value gives a PFS word of 0110011001100110 in temporary registers R0 and R1.

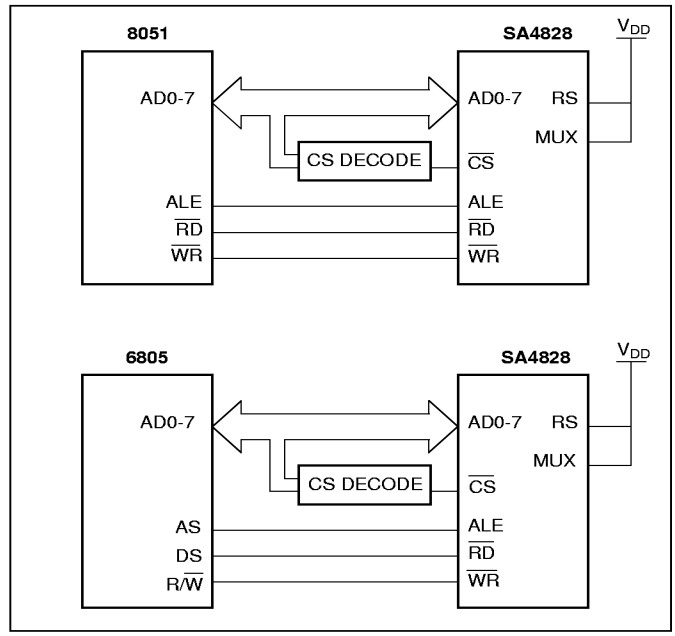



*Fig.11 Connection details for industry standard multiplexed architecture*

### 2. Setting the power waveform amplitude

$$A_{POWER}(\%) = \frac{A}{255} \times 100$$

$$\Rightarrow A = \frac{A_{POWER} \times 255}{100} = \frac{80 \times 255}{100} = 204$$

The 8-bit binary equivalent of this value gives a RAMP word of 11001100 in temporary register R3. YAMP and BAMP contents are don't care.

### 3. Setting forward/reverse, output inhibit etc.

Forward motor control is required (i.e., the phase sequence of the PWM outputs should be red-yellow-blue) therefore forward/reverse bit, $\overline{F}/R = 0$.

Output inhibit should be disabled (i e., the outputs should be active), therefore output inhibit bit, $\overline{INH} = 1$.

Watchdog Timer is disabled so WTE = 0, RST bit = 0 and $\overline{CR}$ bit = 1.

Hence Temporary Register R2 should be set to 00000110.

## APPLICATIONS INFORMATION

### Microprocessor Interfacing

### (i) Multiplexed data buses

Fig. 11 shows the connection details when interfacing industry standard microprocessors to the SA4828. The 8051 and 6805 series are given as examples.

Since the address is written into the SA4828 during each write cycle, this mode of operation is the simplest in terms of the required software. Fig. 12 shows a typical programming example when using multiplexed data buses.

### (ii) Non-multiplexed data buses

Fig. 13 shows the connection scheme for some industry standard microprocessors with non-multiplexed data busses. The 6802, 68000 and TMS320 series are given as examples.

Before each successive write operation with non-multiplexed data busses, it is essential that the address is specified using an extra write operation. Therefore, a write to a specific Temporary Register actually consists of two write cycles - the first defines the address and the second defines the data. To differentiate between them, the Register Select (RS) pin is used. This should be low for the first (address) cycle and high for the second (data) cycle. As shown in Fig. 13, this pin is usually tied to the least significant microprocessor address line.

Fig. 14 shows the flow diagram for each successive write operation to a Temporary Register.

### (iii) Using microcontroller port pins to emulate a data bus

Since the SA4828 is implemented in static logic, the bus timings have no maximum values. This allows the use of microcontrollers where port pins are used to emulate the function of a databus.

In order to minimise the number of port pins used, it is clearly better to emulate a multiplexed data bus. The control lines may be minimised as follows:

If there are no other peripherals connected to the 'bus' then $\overline{CS}$ may be tied to $V_{SS}$. Emulating the $\overline{RD}/\overline{WR}$ control structure means that the $\overline{RD}$ pin would be permanently high. It may therefore be tied to $V_{DD}$. RS is not relevant to multiplexed mode, so this pin may be tied to $V_{DD}$. MUX should also be tied to $V_{DD}$. Therefore, the necessary control may be achieved using just two signals - $\overline{WR}$ and ALE, giving ten port pins in total i.e. 8 address/data and 2 control. Fig. 15 shows this for a generic microcontroller and Fig. 16 shows a flow diagram for a single write cycle.

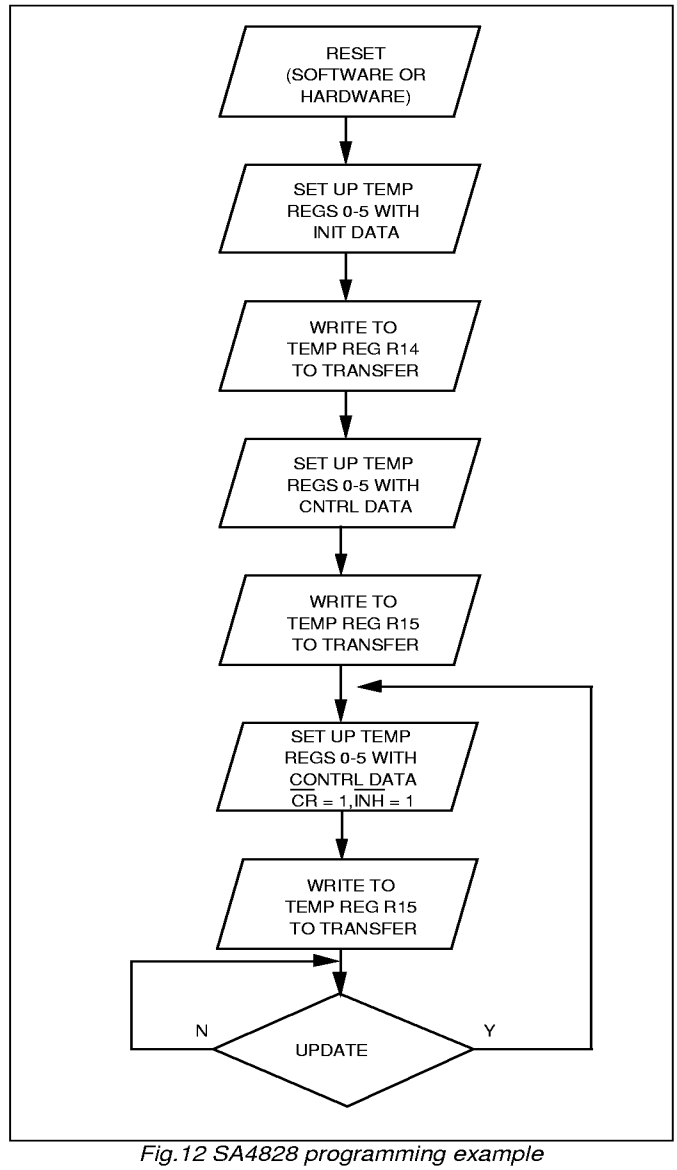



*Fig.12 SA4828 programming example*

### Circuit and Layout Considerations

The SET TRIP input forms a fast means of shutting down the inverter bridge by circumventing the latency associated with a microprocessor interrupt. It is recommended that the $\overline{TRIP}$ output is also linked to a microprocessor interrupt pin in order that the microprocessor is made aware of an incoming trip. It may then perform the necessary housekeeping following the inverter shut down.

Although the SET TRIP input has a debounce circuit built in, the debounce period is necessarily short so that the speed with which the system may be shut down in an emergency is not

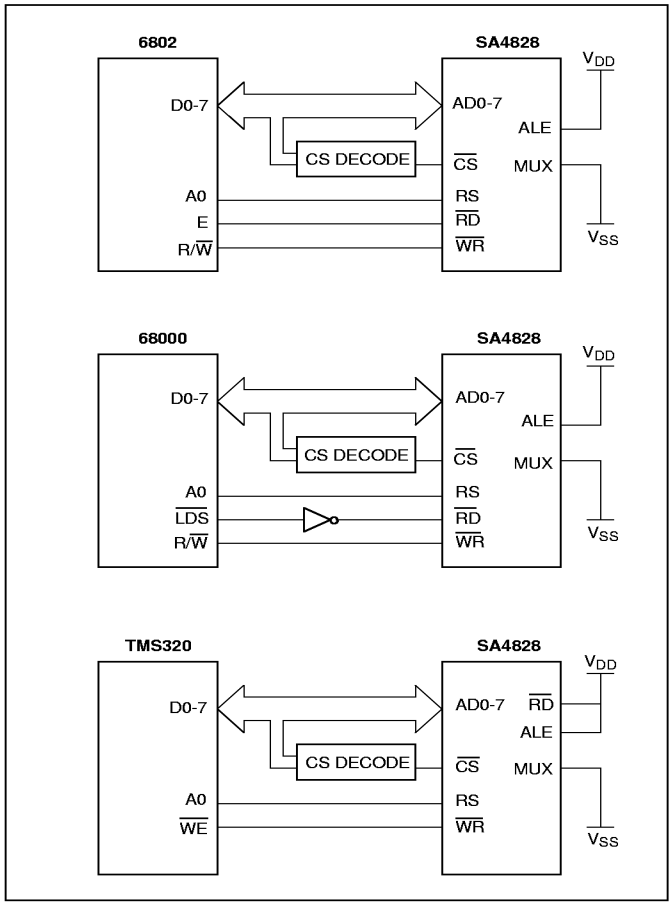



*Fig.13 Connection details for industry-standard non-multiplexed architectures*

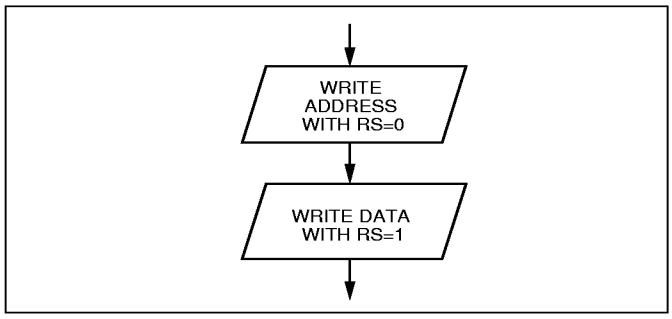



*Fig.14 Flow diagram for non-multiplexed write operation*

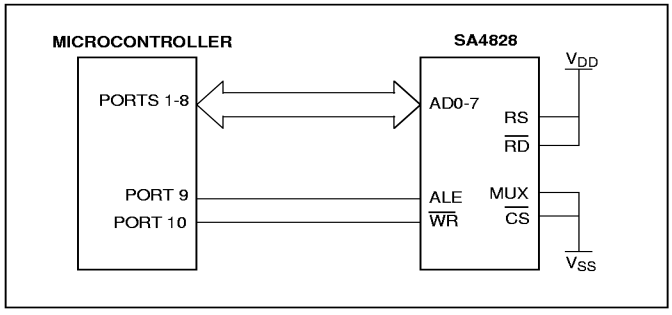



*Fig.15 Connection details for microcontroller interface to SA4828*

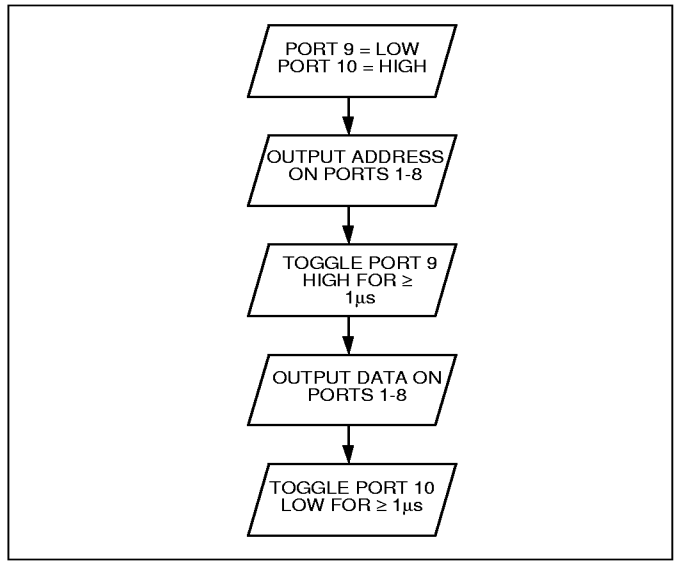



*Fig.16 Flow diagram - interfacing SA4828 to microcontroller*

compromised. It is therefore important to eliminate any possible sources of noise from the SET TRIP input. It may be advantageous to place decoupling capacitors close to the SET TRIP pin if nuisance trips are of concern.

The clock input (CLK) has a high impedance CMOS input and therefore presents very little load. However, when driving this pin from an unbuffered microprocessor crystal, the tracking capacitance may cause the oscillator to stop. It is therefore recommended that a CMOS Schmitt buffer is placed between the crystal and the CLK input of the SA4828 which is physically located as close to the crystal as possible.

The six PWM outputs each have a ±12mA drive capability, enabling them to directly drive optocouplers for isolation purposes. Small pulse transformers may also be driven directly, provided that due consideration is given to back emf generated at turn-off. In addition, the $\overline{\text{TRIP}}$ pin has a ±12mA drive capability to enable it to drive a status LED directly.

Fig. 17 shows a typical application of the SA4828 to a three phase variable speed motor drive.

## QUICK REFERENCE GUIDE TO ENHANCEMENTS

The following list gives a brief outline of the differences between the SA4828 and the SA828 series:-

- Microprocessor interface re-designed for compatibility with more micros.
- Register memory map changed to accommodate more registers.
- Frequency resolution extended to 16-bits.
- Optional independent control of amplitude for each phase.
- Software reset provision.
- Device powers up with the inhibit bit ($\overline{\text{INH}}$) active to force PWM outputs off.
- ZPPY and ZPPB outputs deleted.
- WSS output re-defined.
- Watchdog Timer added.
- Triplen and Deadbanded Triplen waveforms added.
- All waveform options are user selectable.
- All phase bottom outputs pulse high on deassertion of $\overline{\text{INH}}$ to charge boot-strap drive capacitors.

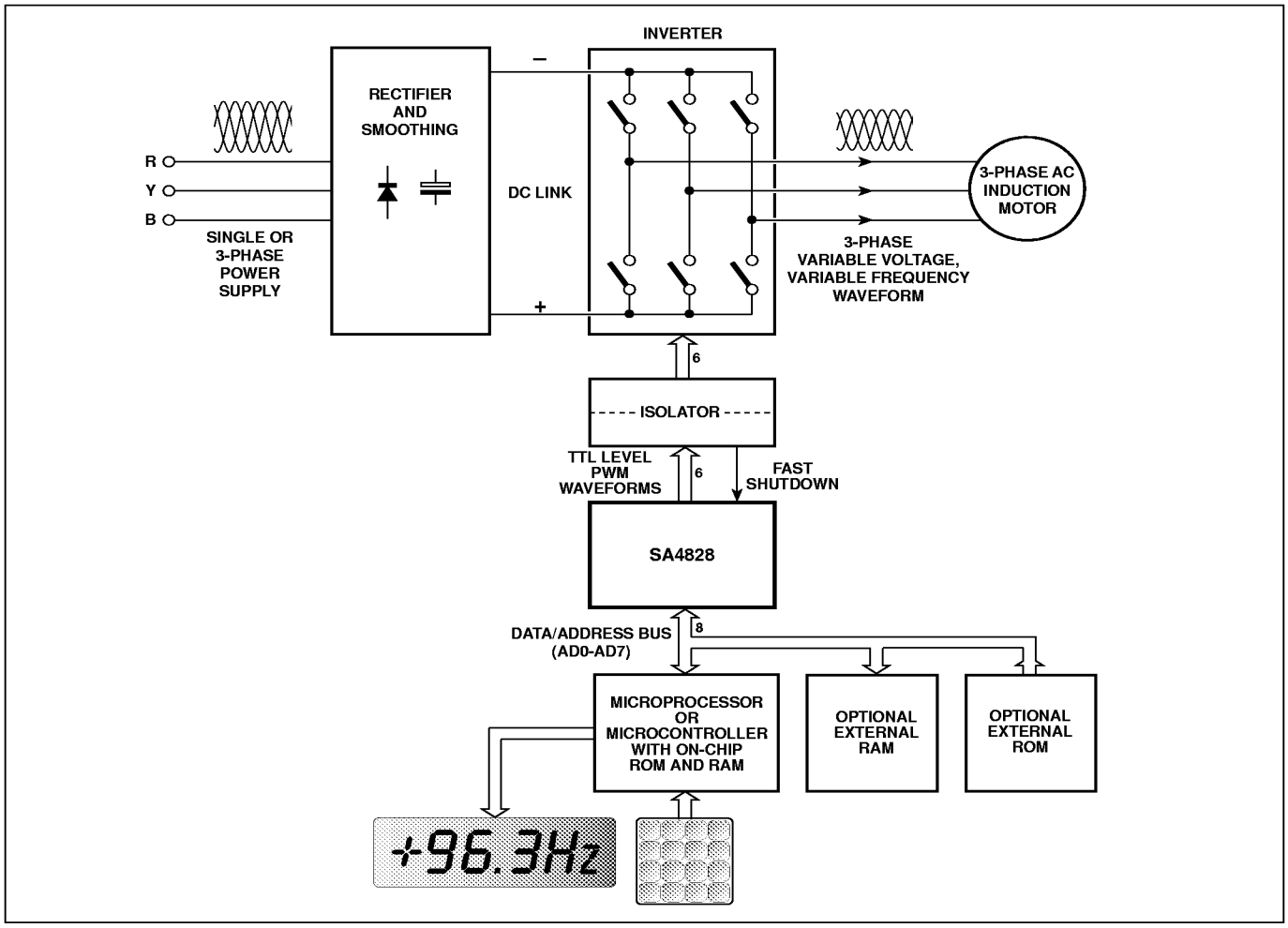
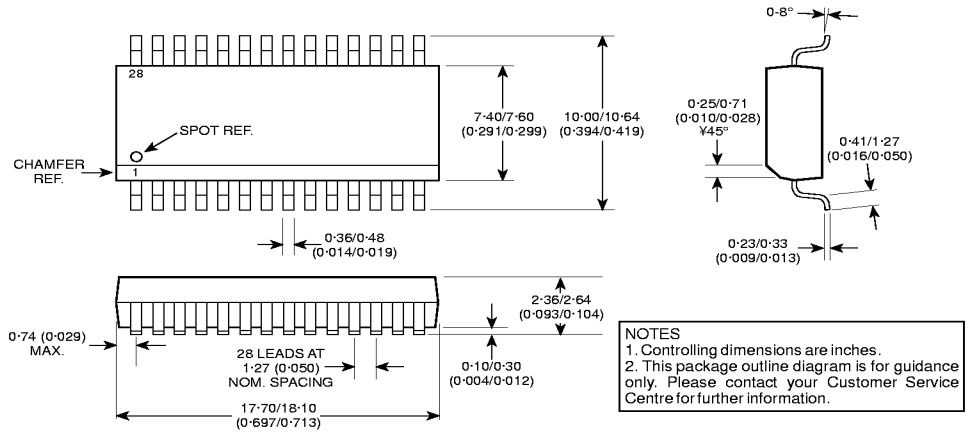


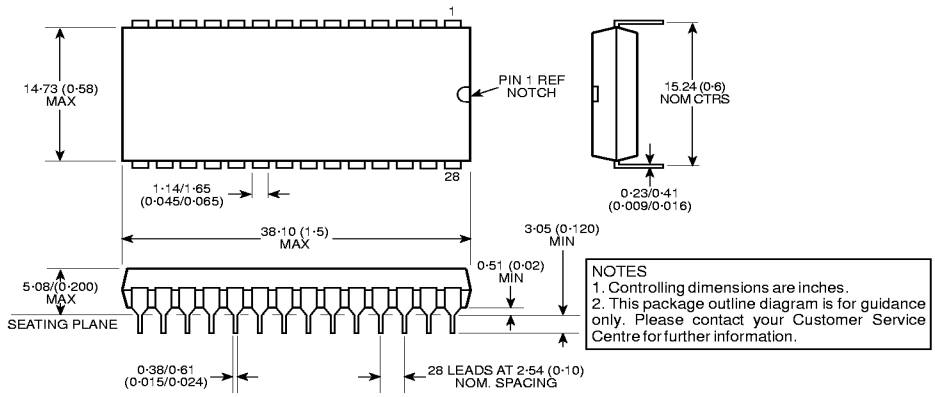

*Fig.17 A typical SA4828 application*

## PACKAGE DETAILS

Dimensions are shown in : mm (in). For further package information, please contact your local representative or nearest Customer Service Centre.




**28-LEAD MINIATURE PLASTIC DIL - MP28**




**28-LEAD PLASTIC DIL – DP28**

MITEL SEMICONDUCTOR

HEADQUARTERS POWER OPERATIONS
**MITEL SEMICONDUCTOR**
Doddington Road, Lincoln,
LN6 3LF, United Kingdom.
Tel: + 44 (0)1522 500500
Fax: + 44 (0)1522 500550

**Internet: http://www.mitelsemi.com**
**e-mail: power_solutions@mitel.com**
POWER PRODUCT CUSTOMER SERVICE CENTRES
- **FRANCE, BENELUX & SPAIN** Tel: + 33 (0)1 69 18 90 00 Fax : +33 (0)1 64 46 54 50
- **NORTH AMERICA** Tel: 011-800-5554-5554 Fax: 011-800-5444-5444
- **UK, GERMANY, REST OF WORLD** Tel: + 44 (0)1522 500500 Fax : + 44 (0)1522 500020

**ADVANCE INFORMATION** - The product design is complete and final characterisation for volume production is well in hand.
These are supported by agents and distributors in major countries world-wide.