Techwell, Inc.

TW9906 – Enhanced 3x10-bit Multi-Standard Comb Filter Video Decoder With YCbCr Input Support

Techwell Confidential. Information may change without notice.

Disclaimer

This document provides technical information for the user. Techwell, Inc. reserves the right to modify the information in this document as necessary. The customer should make sure that they have the most recent data sheet version. Techwell, Inc. holds no responsibility for any errors that may appear in this document. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Techwell, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

TW9906 – 3x10-bit Multi-Standard Comb Filter Video Decoder with YCbCr Component Input

Introduction and Features

Techwell's TW9906 is a high quality NTSC/PAL,/SECAM multi-standard video decoder plus YCbCr component inputs designed for multimedia applications.

TW9906 uses the mixed-signal 2.5V/3.3V CMOS technology to provide a low-cost and low-power integrated solution. Minimum external components are required due to its integrated analog front-end containing anti-aliasing filter, AGC, clamping, and three 10-bit high speed ADCs. For composite inputs, an adaptive comb filter and luma/chroma processing produce exceptionally high quality pictures using proprietary techniques. A high quality internal scaling engine offers arbitrarily filtered down scaling of the output video. Its VBI capability is enhanced with built-in VBI slicer, filter, FIFO and VBI data pass-through function to support common data services.

The main features of the TW9906 are

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM support with automatic format detection
- Advanced synchronization processing for VCR trick mode and weak signal
- Software selectable analog inputs allows any of the following combinations:
  - Up to five composite video inputs
  - Four composite, one S-video or one YCbCr input.
  - Two composite, two S-Video or two YCbCr inputs.
  - Three composite, one S-Video and one YCbCr input.
- Three 10-bit ADCs with clamping circuit and anti-aliasing filter.
- Fully programmable static or automatic gain control for the Y channel
- Programmable white peak control for the Y channel
- Adaptive 4H comb filter for the best image quality.
- PAL delay line for color phase error correction
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL and advanced synchronization processing for non-standard video signals
- Programmable hue, brightness, saturation, contrast, and sharpness
- Blue stretch
- Image enhancement with 2D peaking and CTI.
- Automatic color control and color killer
- IF compensation filter
- Detection of level of copy protection according to Macrovision standard
- YCbCr input supports 480i/576i and sub-sampled 480p/576p with auto-detection.

• Video Output

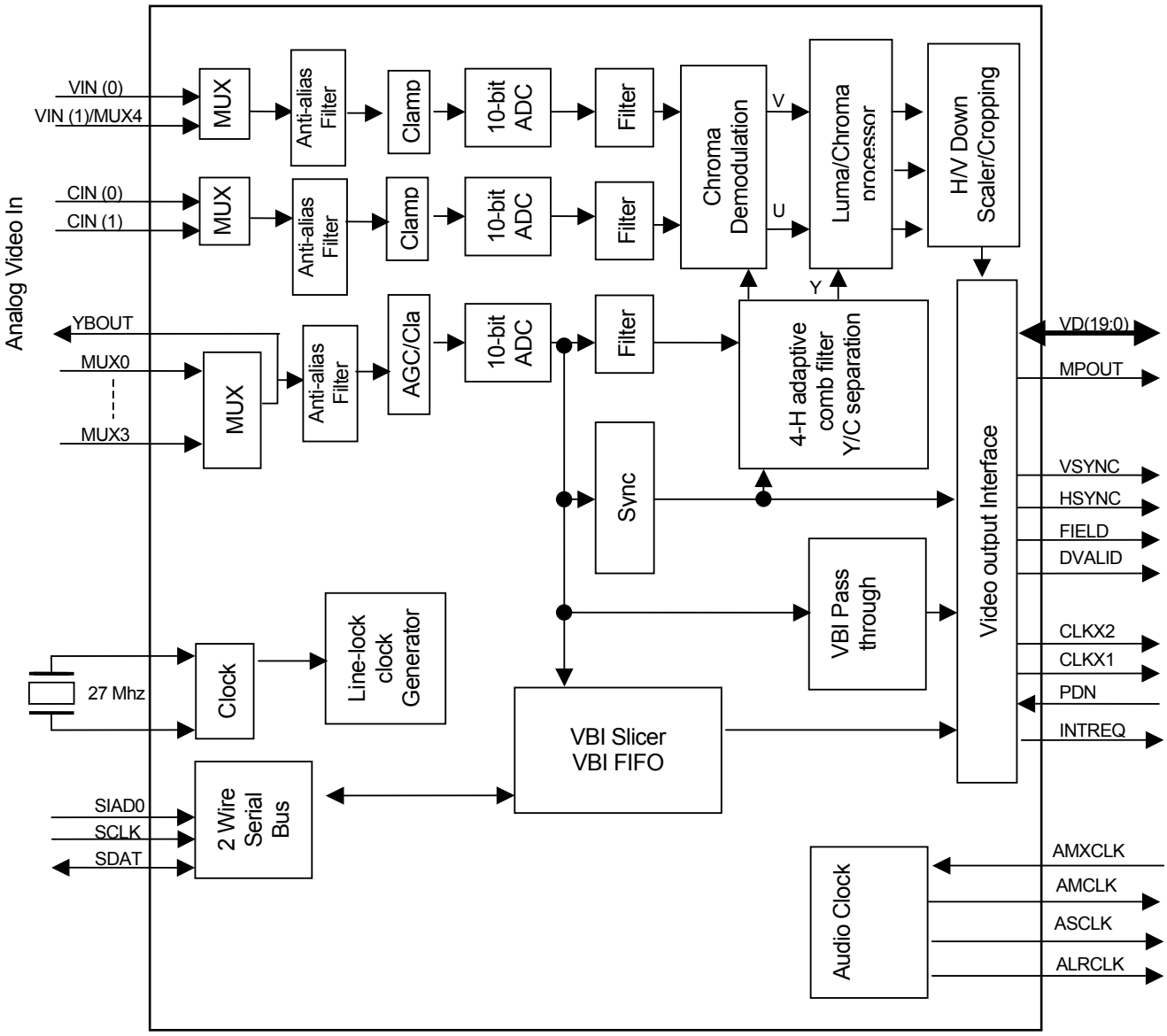
- Support both free-running and line-locked clock outputs
- Programmable output cropping
- High quality horizontal filtered scaling with arbitrary scale down ratio
- VMI 1.4 compatible 10-bit or 20-bit pixel interface
- ITU-R 601 or ITU-R 656 compatible output YCbCr(4:2:2) output format
- VBI slicer supporting industrial standard data services with data packet filter capability
- Built-in VBI FIFO for convenient access through host interface
- VBI data pass through, raw ADC data for Intercast™
- Field locked audio clock generator

• Miscellaneous

- Two wire MPU serial bus interface
- Power-down mode
- Typical power consumption 0.25W
- Single 27MHz crystal for all standards
- Supports 24.54MHz and 29.5MHz crystal for high quality square pixel format
- 3.3V / 5V tolerant I/O
- 2.5V / 3.3V Power Supply
- 80 pin TQFP package

Functional Description

Figure 1: TW9906 Block Diagram



Overview

Techwell's TW9906 is a high quality NTSC/PAL/SECAM video decoder that is designed for multimedia applications. It uses the mixed-signal 2.5V/3.3V CMOS technology to provide a low-power integrated solution.

The TW9906 analog front-end is equipped with three separate analog channels that enable it to accept all three possible analog video signal standards: composite, S-video or YCbCr component video. All channels include an analog multiplexer (MUX) for maximum flexibility in software controlled input selection. It is possible to connect up to five composite inputs at one time and allow the software to switch between them. Alternatively several combinations of composite inputs and S-Video component inputs may be switched under software control. (Four input channels of any format can be accommodated with but there is a maximum of 2 S-Video inputs or 2 component inputs.)

The front-end contains all the necessary circuits to simplify the system design. The built-in three high quality 10-bit analog-to-digital converters (ADCs) convert inputs into digital signals for processing.

The TW9906 uses proprietary adaptive 4H comb filter for chroma and luma separation to achieve high video quality. The image enhancement includes horizontal and vertical peaking, CTI and BCS control.

The advanced synchronization processing can produce stable pictures for non-standard signal such as those produced by VCR trick mode.

The high quality scaler uses multi-tap poly-phase decimation filter to accurately scale down the image with minimum phase error. It can be programmed to scale-down the output picture to an arbitrary ratio with cropping.

The TW9906 supports flexible pixel interface. It outputs YCbCr (4:2:2) data stream over 10-bit or 20-bit data path. It also supports both free-running clock and line-locked clock output.

A 2-wire serial MPU interface is used to simplify system integration. All the functions can be controlled through this interface.

Analog Front-end

The analog front-end converts analog video signals to the required digital format. There are three analog channels with clamping circuits and ADCs. The Y channel has 5-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). Its five inputs are identified as MUX0, MUX1, MUX2, MUX3 and MUX4(share the same pin with VIN1). The C channel has a 2-input multiplexer. Its two inputs are identified as CIN0 and CIN1. The V channel is similar to C channel. Its input is VIN0 and VIN1. Both the C and V channel are internally clamped to the zero level of the bipolar input source when enabled.

Video Source Selection

All analog signals should be AC-coupled to these inputs. The Y channel analog multiplexer selects one of the five inputs MUX[0-4]. MUX[0-4] can be connected to composite video inputs or the Y signal of an S-Video or component input. When decoding a S-Video input, the Y signal should connect to one of the MUX inputs and the C signal to CIN0 or CIN1.

When decoding a component input, in addition to the Y signal, the C signal should connect to CIN0 or CIN1, and V signals should be connect to VIN0 or VIN1 pins.

Software selectable analog inputs allow several possible input combinations:

1. Up to Five composite video inputs. 2. Four composite, one S-video or one component input. 3. Three composite, two S-Video inputs. 4. Three composite, one S-Video and one component input.

The input video signals in any certain channel maybe momentarily connected together through the equivalent of a 200 ohm resistor during multiplexer switching. Therefore, the multiplexer cannot be used for switching on a real-time pixel-by-pixel basis.

Clamping and Automatic Gain Control

All three analog channels have built-in clamping circuit that restore the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60 or a programmable level. Both C(Pb) and V(Pr) channel restores the back porch of the digitized video to a level of 128. This operation is automatic through internal feedback loop.

The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. A programmable white peak protection logic is included to prevent saturation in the case of abnormal proportion between sync and white peak level.

Analog to Digital Converter

TW9906 contains three 10-bit pipelined ADCs that consume less power than conventional flash ADC. The output of the Clamp and AGC connects to one ADC that digitizes the composite input or the Y signal of the S-Video input. The second ADC digitizes the C signal when decoding S-video signal. The third ADC digitizes the Pr(or V) signal when decoding the component input.

Sync Processing

The sync processor of TW9906 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

Horizontal sync processing

The horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal sync detector detects the presence of a horizontal sync tip by examining low-pass filtered input samples whose level is lower than a threshold. After sufficient low levels are detected, a horizontal sync is recognized. Additional logic is also used to avoid false detection on glitches.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide jitter free image output. From there, the PLL also provides orthogonal sampling raster for the down stream processor. The PLL has free running frequency that matches the standard raster frequency. It also has wide lock-in range for tracking any non-standard video signal.

Vertical sync processing

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. It achieves the functionality of a PLL without the complexity of a PLL. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. When the location of the detected vertical sync is inline with a horizontal sync, it indicates a frame start or the odd field start. Otherwise, it indicates an even field. The field logic can also be controlled to toggle automatically while tracking the input.

Color Decoding

Y/C separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is comb filter whenever it is permitted.

In the case of comb filter, the TW9906 separates luma (Y) and chroma (C) of a NTSC composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to good Y/C separation with small cross luma and cross color at both horizontal and vertical edges. Due to the 90-degree phase difference on adjacent lines of a PAL chroma signal, the 4H line memory are used to provide an excellent PAL comb filter performance.

Due to the line buffer used in the comb filter, there is always two lines processing delay in the output except the component input mode which has only one line delay.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

Color demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. The mixing frequency is equal to the sub-carrier frequency for NTSC and PAL. After the mixing, a low-pass filter is used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the mixing frequency is 4.286Mhz. After the mixer and low-pass filter, it yields the FM modulated chroma. The SECAM demodulation process therefore consists of low-pass filter, FM demodulator and de-emphasis filter. The filter characteristics are shown in filter curve section. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

During S-video operation, the Y signal bypasses the comb filter. The C(Pb) signal connects directly to the color demodulator. During component input operation, all the chroma processing and color demodulator blocks are bypassed.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. This color-burst amplitude is calculated and compared to standard amplitude. The chroma (Cx) signals are then increased or decreased in amplitude accordingly. The range of ACC control is –6db to +24db.

Low Color Detection and Removal

For low color amplitude signals, black and white video, or very noisy signals, the color will be "killed". The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmable hysteresis to prevent oscillation of the color killer function. The color killer function can be disabled by programming a low threshold value.

Automatic standard detection

The TW9906 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW9906 supports all common video formats as shown in Table 1.

Table 1. Video Input Formats Supported by the TW9906

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

Luminance Processing

The TW9906 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW9906 video decoder also performs a coring function. It can force all values below a certain level, programmed in the Coring Control Register, to zero. This is useful because human eyes are sensitive to variations in nearly black images. Changing levels near black to true black, can make the image appears clearer.

Sharpness

The TW9906 also provides a sharpness control function through control registers. It provides the control in 16 steps up to +12db. The center frequency of the enhancement curve is selectable by software control. It also provides a high frequency coring function to minimize the amplification of high frequency noise. The coring level is adjustable through the Coring Control register. The same function can also be used to soften the images. This can be used to provide noise reduction on noisy signal.

To further enhance the image, a programmable vertical peaking function is provided for up to +6db of enhancement. A programmable coring level can be adjusted to minimize the noise enhancement.

CTI

The TW9906 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

The Hue and Saturation

When decoding NTSC signals, TW9906 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Power Management

The TW9906 can be put into power-down mode in which its clock is turned off for most of the circuits. The Y, C(Pb) and V(Pr) path can be separately powered down.

Control Interface

The TW9906 registers are accessed via 2-WIRE SERIAL MPU interface. It operates as a slave device. Serial clock and data lines, SCL and SDA, transfer data from the bus master at a rate of 400 Kbits/s. The TW9906 has one serial interface address select pins to program up to two unique serial addresses TW9906. This allows as many as two TW9906 to share the same serial bus. Reset signals are also available to reset the control registers to their default values.

Down-scaling and Cropping

The TW9906 provides two methods to reduce the amount of output video pixel data, downscaling and cropping. The downscaling provides full video image at lower resolution. Cropping provides only a portion of the video image output. All these mechanisms can be controlled independently to yield maximum flexibility in the output stream.

TW9906 Down-Scaling

The TW9906 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses simple line dropping algorithm. Therefore, the use of non-integer vertical scaling ration is not recommended.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW9906 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60 Hz system and 768 pixels for 50 Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register, the 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

NTSC: $HSCALE = [720/N_{pixel\_desired}] * 256$

PAL: $HSCALE = [(720/N_{pixel\_desired})] * 256$

Where: $N_{pixel\_desired}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at SIF resolution, the HSCALE value can be found as:

$HSCALE = [(720/320)] * 256 = 576 = 0x0240$

However, to output a SQ compatible NTSC stream at SIF resolution, the HSCALE value should be found as:

$HSCALE = [(640/320)] * 256 = 512 = 0x200$

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW9906. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8-bit register VSCALE_LO. The maximum scaling ratio is 16:1. Following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

60Hz system: $VSCALE = [240/ N_{line\_desired}] * 256$

50Hz system: $VSCALE = [288/ N_{line\_desired}] * 256$

Where: $N_{line\_desired}$ is the number of active lines output per field.

The scaling ratios for some popular formats are listed in Table 2.

TW9906 Cropping

Cropping allows only subsection of a video image to be output. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the unscaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the unscaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858. The HDELAY should be set to 106 and HACTIVE set to 720. For PAL output at 13.5 MHz rate, the total number of pixels is 864. The HDELAY should be set to 108 and HACTIVE set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

Table 2 shows some popular video formats and its recommended register settings. The CCIR601 format refers to the sampling rate of 13.5 MHz. The SQ format for 60 Hz system refers to the sampling rate of 12.27 MHz, and the SQ format for 50 Hz system refers to the use of sampling rate of 14.75 MHz.

Scaling Ratio	Format	Total Resolution	Output Resolution	HSCALE values	VSCALE (frame)
1:1	NTSC SQ	780x525	640x480	0x0100	0x0100
	NTSC CCIR601	858x525	720x480	0x0100	0x0100
	PAL SQ	944x625	768x576	0x0100	0x0100
	PAL CCIR601	864x625	720x576	0x0100	0x0100
2:1 (CIF)	NTSC SQ	390x262	320x240	0x0200	0x0200
	NTSC CCIR601	429x262	360x240	0x0200	0x0200
	PAL SQ	472x312	384x288	0x0200	0x0200
	PAL CCIR601	432x312	360x288	0x0200	0x0200
4:1 (QCIF)	NTSC SQ	195x131	160x120	0x0400	0x0400
	NTSC CCIR601	214x131	180x120	0x0400	0x0400
	PAL SQ	236x156	192x144	0x0400	0x0400
	PAL CCIR601	216x156	180x144	0x0400	0x0400

Table 2. HSCALE and VSCALE value for some popular video formats.

Two Wire Serial Bus Interface

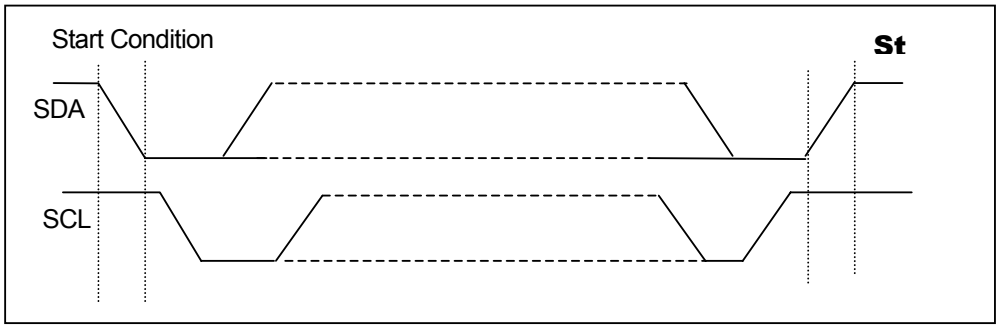


Figure 2. Definition of the serial bus interface bus start and stop

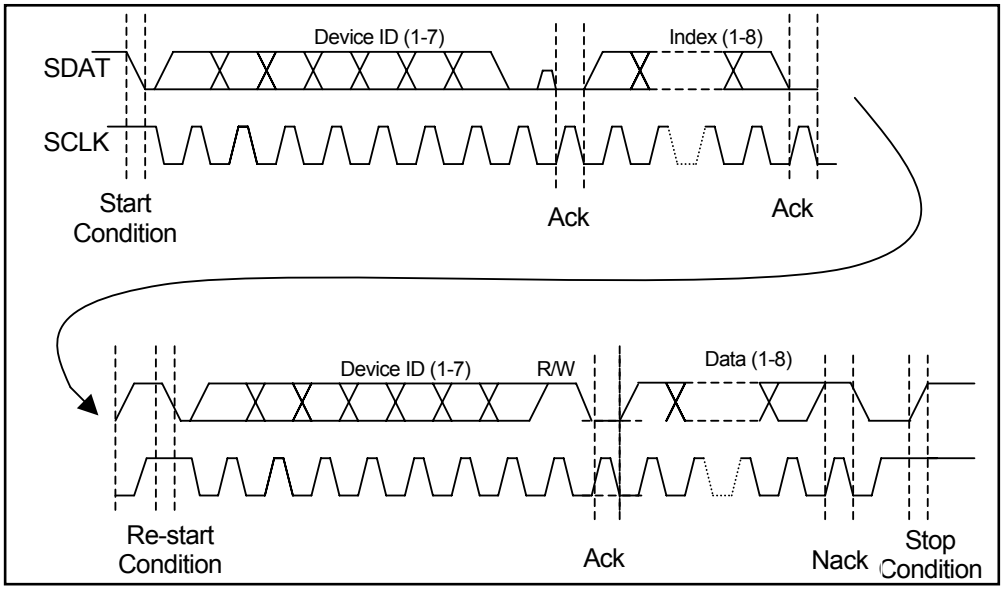


Figure 3. One complete register read sequence via the serial bus interface

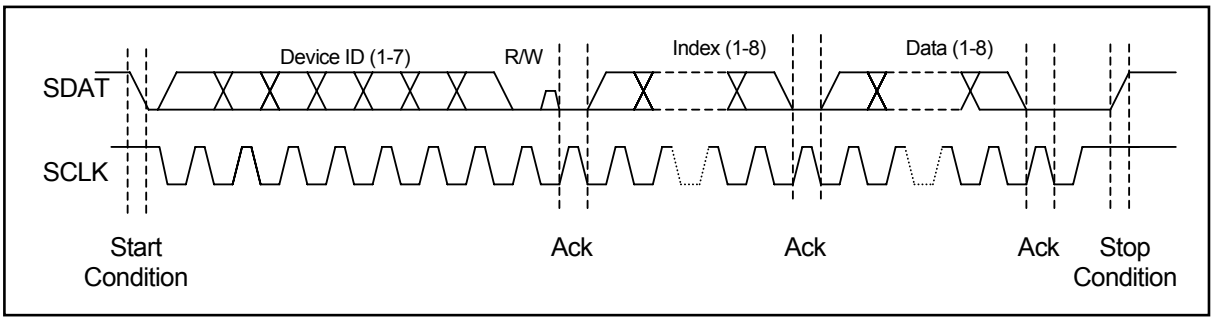


Figure 4. One complete register write sequence via the serial bus interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW9906 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation, the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW9906 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD0 (Serial Interface ADdress) pins either to VDD or VSS (See Table 3.). If the SIAD0 pin is tied to VDD, then the least significant bit of the 7-bit address is a "1". If the SIAD0 pin is tied to VSS then the least significant bit of the 7-bit address is a "0". The most significant 6-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDA from high to low, while SCL is high, this is defined to be a start condition (See Figure 2.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for the their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 3. (For the TW9906, the next byte is normally the index to the TW9906 registers and is a write to the TW9906 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of theTW9906, the master sends another 8-bits of data, the TW9906 loads this to the register pointed by the internal index register. The TW9906 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW9906 if they are in ascending sequential order. After each 8-bit transfer the TW9906 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW9906 the host will issue a stop condition.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	0	SIAD0	1=Read 0=Write

Table 3 TW9906 serial bus interface 7-bit slave address and read write bit

A TW9906 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 3). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and acknowledges the receipt of data

to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

Output Interface

ITU-R BT.656

ITU-R BT.656 defines strict EAV/SAV Code, video data output timing, H blanking timing, and V Blanking timing. In this mode, VD[19:10] pins are only effective and VCLK pin should be used for data clock signal. Table 4 shows EAV/SAV Code format. MSB of forth byte in EAV/SAV code must be "1" in ITU-R BT.656 standard. For that reason, VIPCFG Register bit must be set to "1".

Table 4. ITU-R BT.656 SAV and EAV code sequence

	VD19	VD18	VD17	VD16	VD15	VD14	VD13	VD12	VD11	VD10
1st byte	1	1	1	1	1	1	1	1	1	1
2nd byte	0	0	0	0	0	0	0	0	0	0
3rd byte	0	0	0	0	0	0	0	0	0	0
4th byte	*C	F	V	H	V XOR H	F XOR H	F XOR V	F XOR V XOR H	0	0
H = 0 - SAV, 1 – EAV V = 1 – blanking, 0 – elsewhere F = 0 – field 1, 1 – field 2										

*C is set by VIPCFG register bit.

For complete IRU-R BT.656 standard, following registers are required.

Table 5.ITU-R BT.656 Register set up.

Register	525 line system	625 line system
MODE	1	1
LEN	0	0
VDELAY	0x012	0x018
VACTIVE	0X0F4	0x120
HACTIVE	0x2D0	0x2D0
HA_EN	1	1
VIPCFG	1	1
NTSC656	1	0

ITU-R BT.656 for 525-line system has 244 video active lines in odd field and 243 vide active lines in even field. NTSC656 register bit controls this video active line length.

VIP (Video Interface Port)

Video port in VIP standard is the upgraded standard that has more functions in addition to ITU-R BT.656. Invalid data is set to 0x00 during the period from SAV to EAV if CTL656 register is set to "1" for this VIP application. In case of Vertical down Scaling mode, invalid line does NOT have EAV/SAV code by default setting. This mode is most popular in current VIP application. TW9906 also supports all line EAV/SAV output modes optionally. In this case, VSCTL register should be set to "1". All data will be 0x00 invalid data from SAV to EAV on invalid line in this mode. Starting position of vertical active output video line is programmable by VDELAY register. The number of active video lines is also programmable by VACTIVE register.

Control Signals

TW9906 outputs various control signals. VSYNC and FIELD are vertical timing control signals. HSYNC and DVALID are horizontal timing control signals. These control signals are mainly used on 601 mode (MODE register bit is set to "0".).

Vertical timing diagram

FIGURE 5 shows typical vertical timing for 60Hz/525 lines system. Figure 7 shows typical vertical timing for 50Hz/625 lines system. On Figure 7,VDELAY register is 19DEC(0x13) and VACTIVE register is 241DEC(0x0F1). Figure 8 shows typical NTSC-M setting. On Figure 8, VDEALY register is 24 decimal (0x18) and VACTIVE register is 286 decimal (0x11E). FIGURE 6 shows typical PAL-B setting. The leading edge of VACTIVE is controlled by VDELAY register value. The length of video active lines is controlled by VACTIVE register value. As shown on Figure 7 and 8, output video data stream has 2 lines vertical delay compared to input VIDEO line timing.

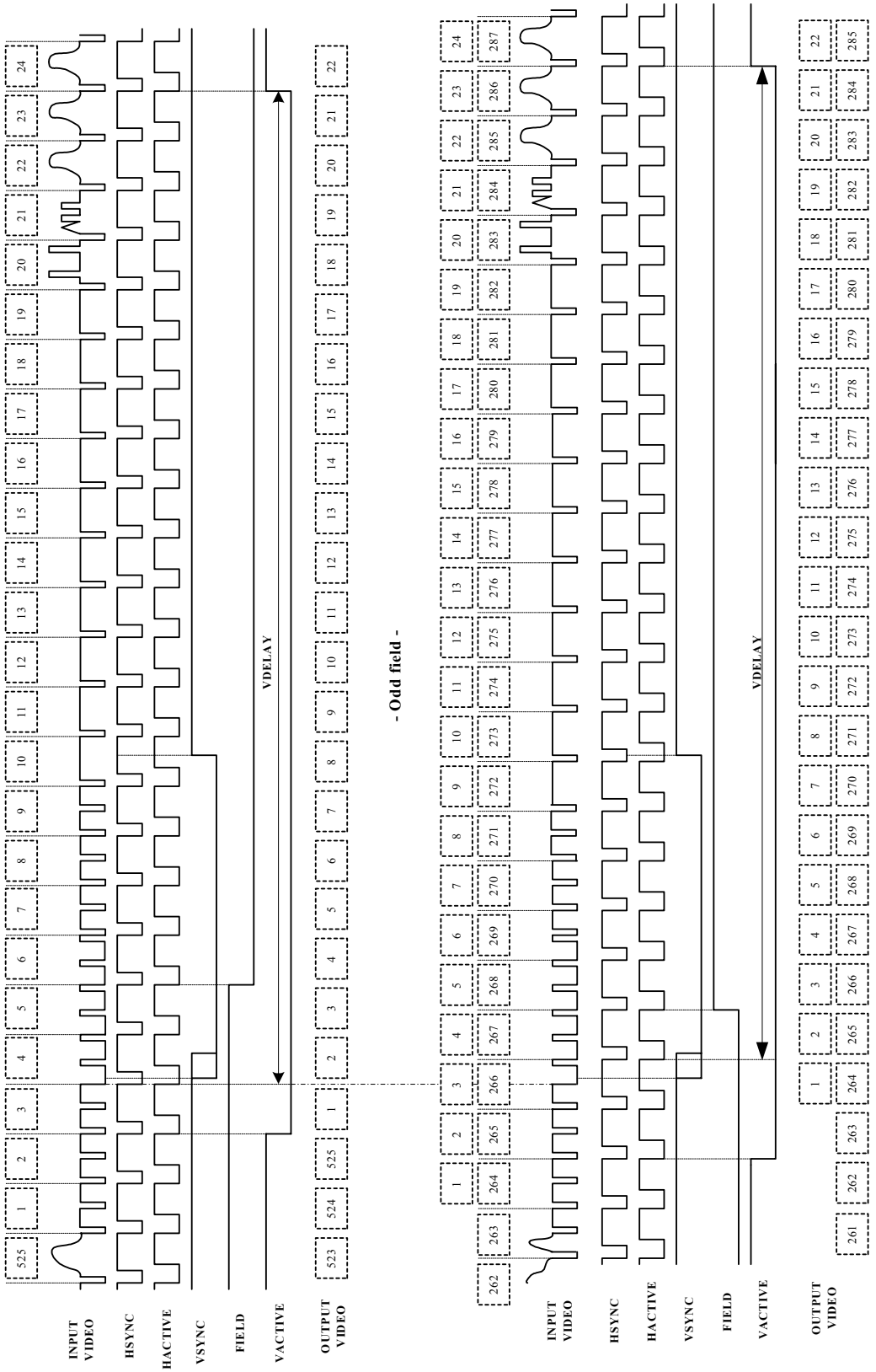


Figure 7.Vertical timing diagram for 60Hz/525 line system

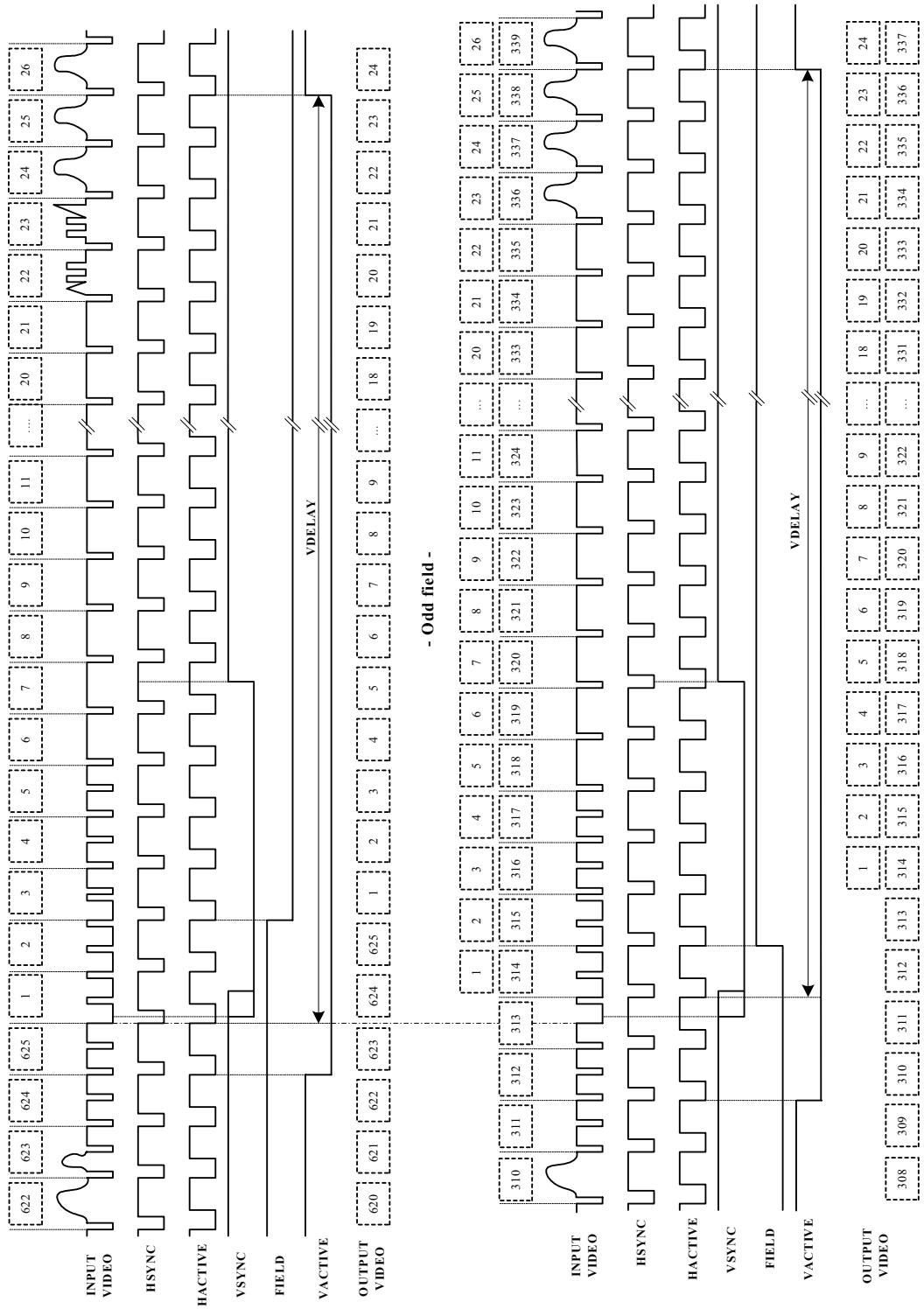


Figure 8. Vertical timing diagram for 50Hz/625 line system

HSYNC

The leading edge of HSYNC signal is synchronized to input Video horizontal sync timing. The start position of HSYNC signal is programmable by HSBEGIN register. The end position of HSYNC signal is also programmable by HSEND registers.

HACTIVE

HACTIVE signal is generated by video decoding process. The active clock period is equal to (HACTIVE register value x 2) clkx2 clock period.

VSYNC

The leading edge of VSYNC signal is synchronized to vertical sync pulse of input Video. The leading edge position of VSYNC signal is programmable by OVSDLY register on a per clkx2 clock basis. The trailing edge of VSYNC signal is in the middle of HSYNC “1” period in odd field and in the middle of HSYNC “0” period in even field. The trailing edge of VSYNC changed on line 10 in 525 lines system and on line 7 in 625-line system as default. This line number is programmable by OVSEND register on a per line basis.

FIELD

Figure 7 and Figure 8 show field signal output assuming default OFDLY register 2H.The line output timing of FIELD signal is programmable by OFDLY register value (1H to 6H). If OFDLY is set to 0H, FILED signal is synchronized to the leading edge of VSYNC signal. If OFDLY is set to 7H, FIELD signal is synchronized to the leading edge of VACTIVE signal. Default FIELD signal shows the ITU-R BT.656 field timing in 656 output video stream by OFDLY register 2H.

Horizontal Down Scaling Output

TW9906 generates Horizontal down scaling output data. Figure 9 shows 10 bit mode Horizontal Down Scaling output timing and Figure 10 shows 20 bit mode Horizontal Down Scaling output timing. As shown Figure 9 and Figure 10, Horizontal Down Scaled data are generated by continuous data stream. The trailing edge of DVALID signal changes with the trailing edge of HACTIVE signal. Data value from the leading edge of HACTIVE to the leading edge of DVALID is programmable by CNTL656 register. If CNTL656 is set to “1”, all Y and CbCr data will be 0x00. If CNTL656 is set to “0”, all Y data will be 0x10 and all CbCr data will be 0x80. VIP application normally uses 0x00 data as invalid data. Figure9 and Figure 10 show 360 active pixels output timing after horizontal downscaling.

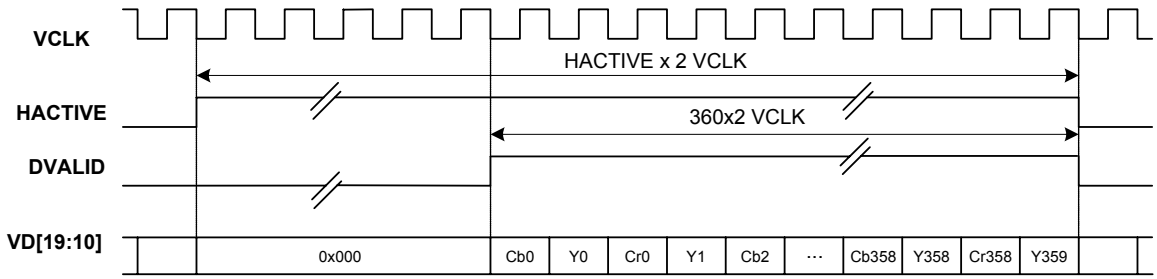


Figure 9. 10 bit mode Horizontal Down Scaling Output

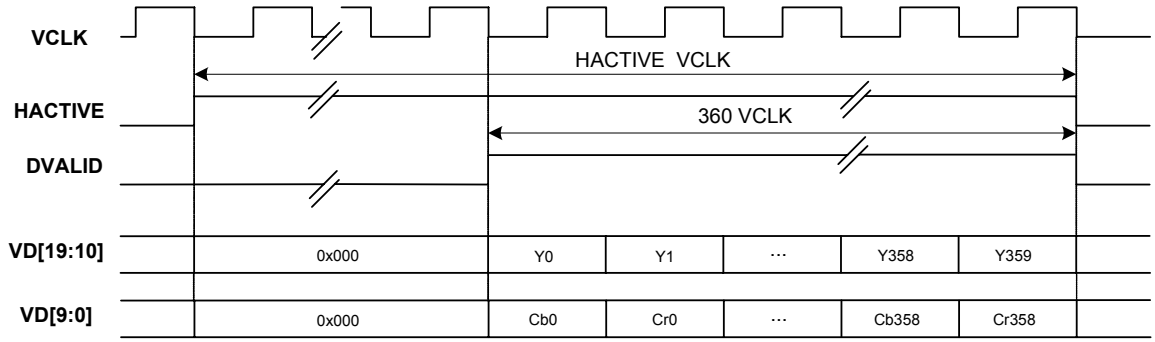


Figure 10. 20 bit mode Horizontal Down Scaling Output

Vertical Down Scaling Output

TW9906 generates Vertical Down Scaling output data. Figure 11 shows its timing. As shown on Figure 11, HACTIVE is NOT generated on invalid line as default (VSCTL is "0"). If VSCTL is set to "1", HACTIVE is generated on every lines during VACTIVE active period. DVALID is not generated on invalid lines in each setting. Invalid lines for Vertical down scaling are generated during VACTIVE active period. If MODE bit is set to "1" for VIP mode, EAV/SAV codes are not generated on those lines without HACTIVE signal. All CbCr data will be 80H and all Y data will be 10H the same as H-blanking data in ITU-R BT.656 data stream.

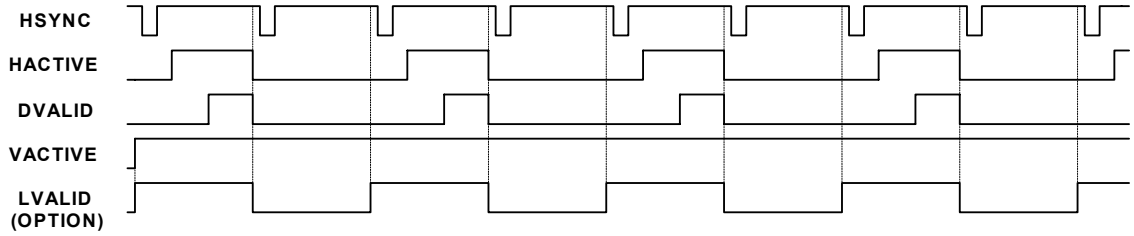


Figure 11. Vertical Down Scaling Output

VBI Data Processing

Raw VBI data output

TW9906 supports raw VBI data output. Raw VBI data output has the same vertical line delay timing as video output. Horizontal output timing is also programmable by VBIDELAY register. Raw VBI data is generated during HACTIVE active period (from SAV to EAV) as Video data output. Total pixel number of raw VBI data per line is twice as many as HACTIVE register value. If VBI EN register is set to “1”, all vertical blanking output while VACTIVE is inactive will be raw VBI data output. If VVBI registers are set to more than “1”, the VVBI number lines from top video active lines will also be raw VBI data output lines.

VBI Data Slicer

The following VBI standards are supported by VBI Data slicer. In TW9906, VBI Data slicing is controlled by registers LCTL6 to LCTL26. Registers LCTL6 to LCTL26, which control the slicing process itself, define what Data Type to be decoded. The Data Type can be specified on a line by line basis for line6 to line26 and for even and odd field depending on the detected TV system standard. The setting for LCTL26 is valid for the rest of the corresponding field. Normally, no text data 0H (video data) should be selected to render the VBI Data slicer inactive during active video. LCTL26 is useful for Full-Field Teletext mode in the case of NABTS. NABTS is 525 Teletext-C. Japan's MOJI is 525 Teletext-D. Didon Antiope is 625 Teletext-A. VBI Data slicer supports up to Physical layer, Link layer in ITU-R BT.653-2. Japan's EIAJ CPR-1204, shown as 525 WSS, has the same physical layer protocol as that of CGMS. The Default VBI Data Slicer is in power-down reset status. PdnSVBI register must be set to 1 for VBI Data Slicer goes into normal mode.

The sliced VBI data is embedded in the ITU-R BT.656 output stream, using the intervals between the End of Active Video (EAV) and the Start of Active Video (SAV) of each line, and formatted according to ITU-R BT.1364 Ancillary data packet Type 2. Data Type shows the register setting value in LCTLn registers.

VBI Standards

STANDARD TYPE	TV Systems (lines/freq)	Bit Rate (Mbits/s)	Modulation	Data Type
625 Teletext-B	625/50	6.9375	NRZ	1H
525 Teletext-B	525/60	5.727272	NRZ	1H
625 Teletext-C	625/50	5.734375	NRZ	2H
525 Teletext-C	525/60	5.727272	NRZ	2H
625 Teletext-D	625/50	5.6427875	NRZ	3H
525 Teletext-D	525/60	5.727272	NRZ	3H
625 CC	625/50	0.500	NRZ	4H
525 CC	525/60	0.503	NRZ	4H
625 WSS	626/50	5	Bi-phase	5H
525 WSS(CGMS)	525/60	0.447443	NRZ	5H
625 VITC	625/50	1.8125	NRZ	6H
525 VITC	525/60	1.7898	NRZ	6H
Gemstar 2x	525/60	1.007	NRZ	7H
Gemstar 1x	525/60	0.503	NRZ	8H
VPS	625/50	5	Bi-phase	9H
625 Teletext-A	625/50	6.203125	NRZ	AH

Sliced VBI Data output format

After 4 bytes of EAV code, sliced VBI ANC data packets are generated by following format DID, SDID, DC, IDI1, IDI2, CS, and BC. Two types of ANC packet format are supported. Following Tables show two types of ANC packet format. All sliced VBI ANC packet format can be changed by ANCMODE register. In following Tables, all type of sliced VBI ANC packet with ANCMODE=1 as examples. If ANCMODE=0, all type of sliced VBI ANC packet have format 0 type.

Sliced VBI ANC data packet format 0(ANCMODE=0)

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	1	0	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	NEP	EP	DC5	DC4	DC3	DC2	DC1	DC0	DC
7	Video line #[7:0]								IDI1. UDW1
8	0	0	0	Data Error	Macth1	Mach2	Video line #[9:8]		IDI2. UDW 2
9	Sliced VBI Data byte 1								Sliced VBI Data No.1. UDW3
10	Sliced VBI Data byte 2								Sliced VBI Data No.2. UDW4
11	Sliced VBI Data byte 3								Sliced VBI Data No.3 UDW5
12	Sliced VBI Data byte 4								Sliced VBI Data No.4. UDW6
13	Sliced VBI Data byte 5								Sliced VBI Data No.5. UDW7
.	.								
.	.								
4N+6	Sliced VBI Data byte last or FILLDATA								Sliced VBI Data Last or FILLDATA. UDW 4N
4N+7	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
4N+8	0	0	0	0	0	0	0	0	BC

EP is Even Parity of bits 5 to 0 in same 1 byte.
NEP is inverted EP in same 1 byte.

DID: 91h: Sliced data of VBI lines of field 1.
53h: Sliced data of lines 24 to end of field 1.
55h: Sliced data of VBI lines of field 2.
97h: Sliced data of lines 24 to end of field 2.

SDID[5:0]: 0h: Teletext(A,B,C,D)
1h: CC(525,625)
2h: WSS(525,625)
3h: VITC(525,6256)
4h: VPS(625 only),Gemstar2x(NTSC only)
5h: Gemstar1x(NTSC only)

DC[5:0]: The number of DWORDs beginning with byte9 through 4N+8.Each DWARD is 4 bytes.

IDI1: Transaction video line number[7:0]

IDI2: Bit1-0 - Transaction video line number[9:8]
Bit2 - Match 2 flag.
Bit3 - Match 1 flag.
Bit4 – 1 if an error was detected in teletext packet.0 if no error was detected.

CS: Sum of D7-D0 of UDW3 through UDW4N.

FILLDATA is FILLDATA register value. FILLDATA is inserted after last valid bytes to make 4N number byte stream sometimes.

Sliced VBI ANC data packet format 1(ANCMODE=1)

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	NEP	EP	DC5	DC4	DC3	DC2	DC1	DC0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	DT3	DT2	DT1	DT0	IDI2. UDW 2
9	Sliced VBI Data byte 1								Sliced VBI Data No.1. UDW3
10	Sliced VBI Data byte 2								Sliced VBI Data No.2. UDW4
11	Sliced VBI Data byte 3								Sliced VBI Data No.3 UDW5
12	Sliced VBI Data byte 4								Sliced VBI Data No.4. UDW6
13	Sliced VBI Data byte 5								Sliced VBI Data No.5. UDW7
.	.								
.	.								
4N+6	Sliced VBI Data byte last or FILLDATA								Sliced VBI Data Last or FILLDATA. UDW 4N
4N+7	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
4N+8	OP	0	BC5	BC4	BC3	BC2	BC1	BC0	BC

EP is Even Parity of bits 5 to 0 in same 1 byte.
NEP is inverted EP in same 1 byte.
{DID4, DID3, DID2, DID1, DID0} is DID register value.
{SDID5, SDID4, SDID3, SDID2, SDID1, SDID0} is SDID register value.
{DC5, DC4, DC3, DC2, DC1, DC0} is the number of DOWRD data length from UDW1 to UDW4N.On this table, {DC5, DC4, DC3, DC2, DC1, DC0} is N (decimal).
OP is Odd Parity of bits 6 to 0 in same 1 byte.
FID=0: odd field; FID=1: even field.
{LN8, LN7, LN6, LN5, LN4, LN3, LN2, LN1, LN0} is the line number of current sliced VBI data.
{DT3, DT2, DT1, DT0} is the Data Type shown on Table
NCS6 is inverted CS6.
{CS6, CS5, CS4, CS3, CS2, CS1, CS0} is the checksum value calculated from DID to UDW4N.
UDW1 to UDW4N are the User data words (UDW) shown on ITU-R BT.1364 ANC data packet type 2.
[BC5, BC4, BC3, BC2, BC1, BC0] is the number of valid bytes from UDW1 to UDW4N.
FILLDATA is FILLDATA register value. FILLDATA is inserted after last valid bytes to make 4N number byte stream sometimes.

Closed Captioning ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

525 Lines WSS (CGMS Copy Generation Management System) ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	1	IDI2. UDW 2
9	WSS[7:0]								UDW3
10	WSS[15:8]								UDW4
11	{0H,WSS[19:16]}								UDW5
12	CRCERRORCODE								UDW6
13	FILLDATA								UDW7
14	FILLDATA								UDW8
15	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
16	1	0	0	0	0	1	1	0	BC

1.CRCERRORCODE is optional byte. 41H means “this wss data has CRC Error”. 80H means no CRC error.

625 Line WSS (Wide-Screen Signaling) ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	1	IDI2. UDW 2
9	WSS[7:0]								UDW3
10	{00b,WSS[13:8]								UDW4
12	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
13	0	0	0	0	0	1	0	0	BC

625 Teletext-A ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	1	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
46	BYTE40								UDW40
47	HAMM84ERROR								UDW41
48	FILLDATA								UDW42
49	FILLDATA								UDW43
50	FILLDATA								UDW44
51	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
52	0	0	1	0	1	0	0	1	BC

1.FRAME CODE is E7H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

625 Teletext-B ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	1	0	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
50	BYTE44								UDW44
51	BYTE45								UDW45
52	HAMM84ERROR								UDW46
53	FILLDATA								UDW47
54	FILLDATA								UDW48
55	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
56	1	0	1	0	1	1	1	0	BC

1.FRAME CODE is 27H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

525 Teletext-B ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
30	BYTE36								UDW36
31	BYTE37								UDW37
32	HAMM84ERROR								UDW38
33	FILLDATA								UDW39
34	FILLDATA								UDW40
35	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
36	1	0	1	0	0	1	1	0	BC

1.FRAME CODE is 27H if it's received correctly.
3.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

625 Teletext-C and 525 Teletext-C ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	HAMM84ERROR								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

1.FRAME CODE is E7H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

625 Teletext-D and 525 Teletext-D ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	1	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	BYTE37								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

1.FRAME CODE is A7H if it's received correctly.

Line16 VPS (Video Program System) ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	1	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	1	IDI2. UDW 2
9	START CDDE1 (51H)								UDW3
10	START CODE2 (99H)								UDW4
11	BYTE3								UDW5
.	.								
.	.								
22	BYTE14								UDW16
23	BYTE15								UDW17
24	BI-PHASEERROR								UDW18
25	FILLDATA								UDW19
26	FILLDATA								UDW20
27	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
28	1	0	0	1	0	0	1	0	BC

1.START CODE1 is the first byte of Start Code by 5Mbps slicing.
2.START CODE2 is the second byte of Start Code by 5Mbps slicing.
4.BYTE3~BYTE15 are data bytes by 5/2 Mbps Bi-phase slicing.
5.BI-PHASEEROOR is Bi-phase coding error detection.80H means No error.41H means Bi-phase coding error is detected.

VITC (Vertical Interval Time Code) ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	0	IDI2. UDW 2
9	Bit[9:2] VITCFrame1								UDW3
10	Bit[19:12] VITCFrame2								UDW4
11	Bit[29:22] VITCSec1								UDW5
12	.Bit[39:32] VITCSec2								UDW6
13	.Bit[49:42] VITCMin1								UDW7
14	Bit[59:52] VITCMin2								UDW8
15	Bit[69:62] VITCHours1								UDW9
16	Bit[79:72] VITCHours2								UDW10
17	Bit[89:82] VITCCRC								UDW11
18	CRCERROR								UDW12
19	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
20	1	0	0	0	1	1	0	0	BC

1.CRCERROR is CRC Error information.41H means CRC Error is deteced.80H means no CRC error.

Gemstar 1X ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

Gemstar 2X ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	1	IDI2. UDW 2
9	FRAMECODE1								UDW3
10	FRAMECODE2								UDW4
11	Data Byte 1								UDW5
12	Data Byte 2								UDW6
13	Data Byte 3								UDW7
14	Data Byte 4								UDW8
15	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
16	0	0	0	0	1	0	0	0	BC

1.FRAMCODE1 is B9H if Frame Code is correctly received.
2.FRAMCODE2 is 05H if Frame Code is correctly received.

Sliced VBI RAM HOST Access

Host Interface has dedicated Sliced VBI RAM read function as follows.

S: Start bit, CA: 7bit Chip Address, 0x03 is Register0x03 Address number. RAD is SVBI RAM address 0xDF.RD1,RD2, RD3, RD4,…, RDn are read data from Sliced VBI RAM. Number n can be decided from SVBIWCOUNT register value.

S {CA,0} ACK {0x03} ACK {xxx1xxxx} ACK …set up AINC=1
S {CA,0} ACK {RAD} ACK …set up RAD for read Sub-Address
S {CA,1} ACK {RD1} ACK {RD2} ACK {RD3} ACK {RD4} ACK…..ACK {RDn} NAK
S {CA,0} ACK {0x03} ACK {xxx0xxxx} ACK ….set up AINC=0

Sliced VBI RAM Control

Sliced VBI data is stored into Sliced VBI RAM with ANC packet format as shown above. Stored ANC packet format is exactly same as Sliced VBI output format. If SVBIRAMMODE register is set to 0, only teletext data is stored into Sliced VBI RAM. If SVBIRAMMODE register is set to 1,all detected Sliced VBI data is stored into Sliced VBI RAM. If SVBIRAMRST register is set to 1,all data into Sliced VBI RAM are reset to 0x00. SVBIWCOUNT register shows the current number of words stored into SVBI RAM. If Sliced RAM has more than the number of words set to FTHRESHOLD registers, FIFOTHRS interrupt is generated.

Teletext TTX Filter Control

If TTX Filter is enable, user can specify data packet to be received. TTX Filter use 4 data bit pattern included in Hamming encoded bytes. If NABTS, Teletext-C, Teletext-A, 5 header bytes (as packet prefix) are filtered by FILEMODE register=0. If WST, Teletext-B, 2 header bytes (as packet prefix) are filtered by FILMODE register=1. Only data portion {bit7, bit5, bit3, bit1} from each bytes is applied to TTX filter function with corresponding pattern bits register F1PAT1 to F2PAT5 and mask bit registers F1MASK1 to F2MASK5. TTX Filter1 equation F1Out is as follows. D1[3:0] to D5[3:0] are received 4bit data in Hamming byte. TTX Filter2 has same equation as Filter1.

D1_F1Pass = ((D1[3] xor F1PAT1[3]) nand F1MASK1[3])
and ((D1[2] xor F1PAT1[2]) nand F1MASK1[2])
and ((D1[1] xor F1PAT1[1]) nand F1MASK1[1])
and ((D1[0] xor F1PAT1[0]) nand F1MASK1[0])
D2_F1Pass = ((D2[3])xor F1PAT2[3]) nand F1MASK2[3])
and ((D2[2]) xor F1PAT2[2]) nand F1MASK2[2])
and ((D2[1]) xor F1PAT2[1]) nand F1MASK2[1])
and ((D2[0]) xor F1PAT2[0]) nand F1MASK2[0])
D3_F1Pass = ((D3[3]) xor F1PAT3[3]) nand F1MASK3[3])
and ((D3[2]) xor F1PAT3[2]) nand F1MASK3[2])
and ((D3[1]) xor F1PAT3[1]) nand F1MASK3[1])
and ((D3[0]) xor F1PAT3[0]) nand F1MASK3[0])
D4_F1Pass = ((D4[3]) xor F1PAT4[3]) nand F1MASK4[3])
and ((D4[2]) xor F1PAT4[2]) nand F1MASK4[2])
and ((D4[1]) xor F1PAT4[1]) nand F1MASK4[1])
7 and ((D4[0]) xor F1PAT4[0]) nand F1MASK4[0])
D5_F1Pass = ((D5[3]) xor F1PAT5[3]) nand F1MASK5[3])
and ((D5[2]) xor F1PAT5[2]) nand F1MASK5[2])
and ((D5[1]) xor F1PAT5[1]) nand F1MASK5[1])
and ((D5[0]) xor F1PAT5[0]) nand F1MASK5[0])
F1Pass = D1_F1Pass and D2_F1Pass and D3_F1Pass and D4_F1Pass and D5_F1Pass
F1Out = F1Pass and FIL1EN

FILLOGIC register makes the last filter selection from F1Out, F2out signal

FILLOGIC_
00 : F_Pass_n = F1Out nor F2Out
01 : F_Pass_n = F1Out nand F2Out
10 : F_Pass_n = F1Out or F2Out
01: F_Pass_n = F1Out and F2Out

When F_Pass_n is detected as negative 0, this packet is stored and output. If FILEMODE register is set to 1(2 header bytes), registers F1MASK3, F1MASK4, F1MASK5, F2MASK3, F2MASK4 and F2MASK5 should be set to 0x0 as mask bits.

Teletext Framing Code checking.

If TTXFREN register is set to 1,Teletext Framing code is compared to TTXFRPAT register value with TTXFRMASK register bits. If TTXFRMASK[m] bit is 1, this bit number m of received framing code is compared to TTXFRPAT[m] bit value. If all non-Masked bit value of received framing code are equal to the value of TTXFRPAT, this received teletext packet is stored and output. This is helpful not to receive different type of Teletext services.

V-Chip Decoder

V-Chip information is fully decoded in dedicated registers V-Chip, VCHIP_R, VCHIP_A, VCHIP_V, VCHIP_S, VCHIP_G, as EIA-608/EIA-744 bit formats. V-Chip full decoder is enable when LCTL21[3:0] register is set to Field2 CC detection mode. When V-Chip status changes, V-Chip interrupt is generated with VCHIP_CHANGED_DET status bit.

EDS Packet Decoder

EDS Packet is fully decoded in EDSDATA1 to EDSDATA10 registers with EDS Class information registers. Up to 8 Characters data after Control, Type characters are stored into EDSDATA1-10 registers. Class Information consisted of CURRENT, FUTURE, CHANNEL, MISCELLANEOUS, PUBLICSERVICE, RESERVED, UNDEFINED are detected and stored into status register. TIMEOFDAY (Time of Day) EDS packet is also detected. EDS packet decoder is enable when LCTL21[3:0] register is set to Field2 CC detection mode. When EDS packet status is detected and EDSDATA1-10 registers, EDS status register are updated, EDSSTDET interrupt is generated with EDSSTDET status bit.

Interrupt Control

Interrupt control/status registers consist 4 types of registers, INTnMASK, INTnCLEAR, INTnRAWSTATUS, and INTnSTATUS (n=1,2,3). Reg0xB6 is INT1RAWSTATUS, Reg0xB7 is INT2RAWSTATUS, and Reg0xB8 is INT3RAWSTATUS. The same bit number of these INTnMASK, INTnCLEAR, INTnRAWSTATUS, and INTnSTATUS have the relationship. The bit value of INTnRAWSTATUS shows just current hardware signal status in decoding logic. The bit value of INTnSTATUS is set to 1 by the active edge trigger of INTnRAW STATUS register bit and reset to 0 by the rising edge of the bit in INTnCLEAR register. If the bit value of INTnMASK register is set to “0”, that bit value does not cause any interrupt generation. If the value 1 is written into the bit number m(m=0-7) of INTnCLEAR register. The value of the bit number m of INTnSTATUS register is always cleared to 0. If any bit of INTnSTATUS register has the value 1, and the value of that bit number in INTnMASK register is set to 1(not MASK), Interrupt signal is generated on Pin INTREQ. In typical Interrupt application, INTnMASK, INTnCLEAR, and INTnSTATUS registers are used.

VBI data application does not need to check Sliced VBI data registers at every field or every frame period. Some VBI data service does not change the data for long period. In 525 line CGMS (WSS 525) services, if three status bits consists of NO_WSS525_CRC_ERROR, WSS_CHANGED, WSS_DET are 111b, WSS_ALLDATA registers have the valid value to be read. In 625 line WSS (Wide Screen Signaling) services, if WSS_CHANGED, WSS_DET bits are 11b, WSS_ALLDATA registers have the valid value to be read. In EIA-608 type (CC F1, CC F2) application, if NO_CCF1_NULL status bit is 1, it means CCF1DATA registers do NOT have NULL code 0x80 and CCF1DATA registers have the meaningful data to be read. If NO_CCF2_NULL status bit is 1, CCF2DATA registers also have the meaningful data like NO_CCF1_NULL case. In line16 VPS application, if VPS_CHANGE, VPS_DET status bits are 11b, VPSDATA1-13 registers are updated and having the new valid data. In VITC application, if NO_VITC_CRC_ERROR, and VITC_DEC status bits are 11b, registers VITCFRAME1 to VTICCRC are updated new data without crc error.

Audio clock generation

(Register 40 to 48)

TW9906 has built-in field locked audio clock generator for use in video capture applications. The circuitry will generate the same predefined number of audio sample clocks per field to ensure synchronous playback of video and audio after digital recording or compression. The audio clock is digitally synthesized from the crystal clock input with reference to the incoming video.

The master audio clock frequency is programmable through ACKN and ACKI register based following two equations.

ACKN = round (F audio / F field), it gives the Audio master Clock Per Field.

ACKI = round (F audio / F crystal * 2^23), it gives the Audio master Clock Nominal Increment.

Following table provides setting example of some common used audio frequency assuming crystal frequency of 27MHz.

AMCLK(Mhz)	FIELD[Hz]	ACKN [dec]	ACKN [hex]	ACKI [dec]	ACKI [hex]
256 x 48 KHz					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
256 x 44.1KHz					
11.2896	50	225792	3-72-00	3507556	35-85-65
11.2896	59.94	188348	2-DF-BC	3507556	35-85-65
256 x 32 KHz					
8.192	50	163840	2-80-00	2545166	26-D6-0E
8.192	59.94	136670	2-15-DE	2545166	26-D6-0E
256 x 8 KHz					
2.048	50	40960	A0-00	636291	9-B5-83
2.048	59.94	34168	85-78	636291	9-B5-83

Two further divided down clocks are available on pin ASCLK and pin ALRCLK. These two clocks are derived from AMXCLK input based on following two equations. The frequency of these two slower digital clocks can be controlled by registers SDIV and LRDIV as shown.

$$f_{asclk} = \frac{f_{amxclk}}{(SDIV+1) * 2}$$

$$f_{alrclk} = \frac{f_{asclk}}{LRDIV * 2}$$

Some other Audio Clock related control functions are explained here.

ACPL Audio PLL control
0 – PLL loop closed
1 – PLL loop open

SRPH ASCLK phase control
0 – Invert AMXCLK, ASCLK transition is triggered by falling edge of AMXCLK
1 – Normal AMXCLK, ASCLK transition is triggered by rising edge of AMXCLK

LRPH ALRCLK phase control
0 – Invert ASCLK, ALRCLK transition is triggered by falling edge of ASCLK
1 – Normal ASCLK, ALRCLK transition is triggered by rising edge of ASCLK

APG, APZ Audio PLL dynamic control

Test Modes

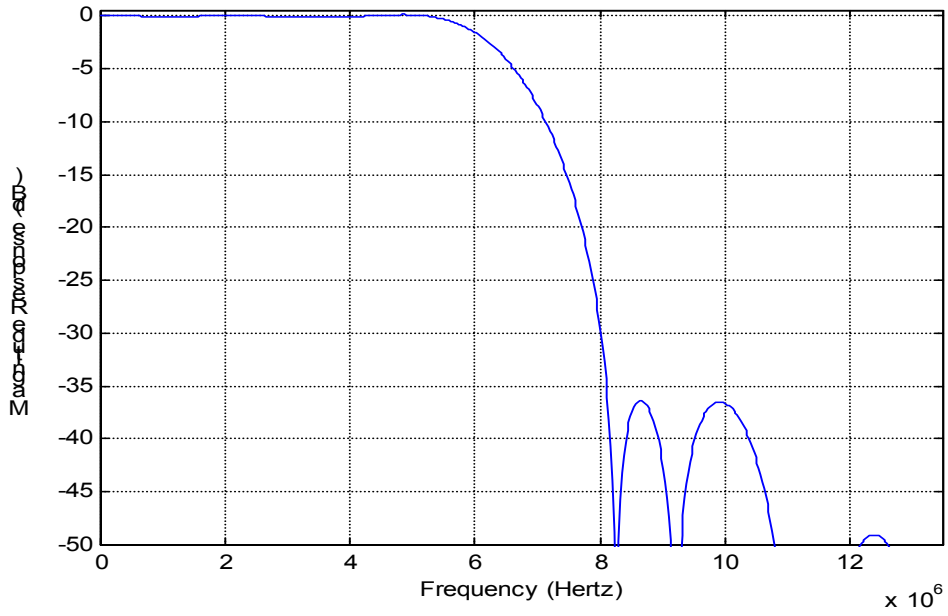
The input pin TMODE combining with RST# provide different test modes selection. If this pin is low at the rising edge of the RST# pin and remaining low afterwards, TW9906 is in the normal operating mode. Other test modes can be obtained as shown in Table 6.

Table 6. Test mode selection and description

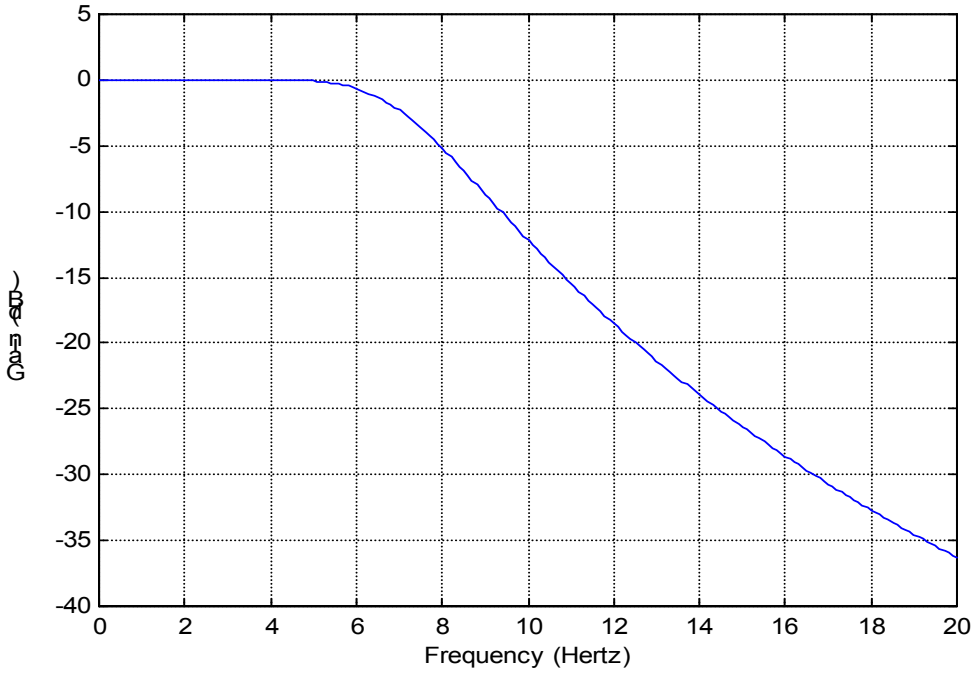
Test mode	TMODE before RST# rising edge	TMODE after RST# rising edge	Description
Normal	0	0	Normal operation mode.
Pin tri-state	0	1	In this mode, all pin output drivers are tri-stated. Pin leakage current parameters can be measured.
Outputs high	1	0	In this mode, all pin output drivers are forced to the high output state. Pin output high voltage, V_{OH} and I_{OH}, can be measured.
Outputs low	1	1	In this mode, all pin output drivers are forced to the low output state. Pin output low voltage, V_{OL} and I_{OL}, can be measured.

Filter Curves

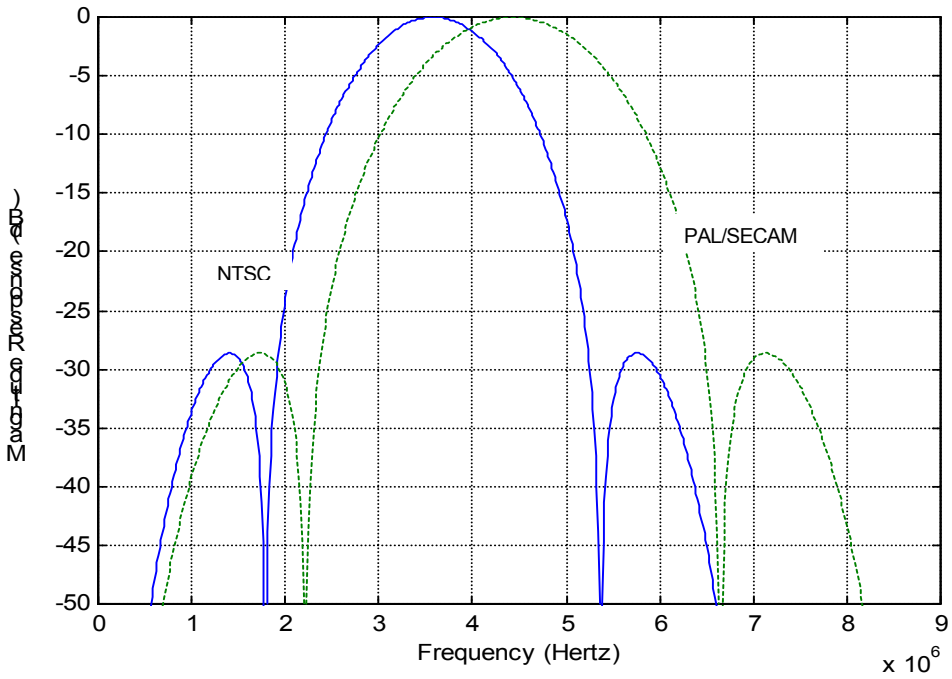
Decimation filter



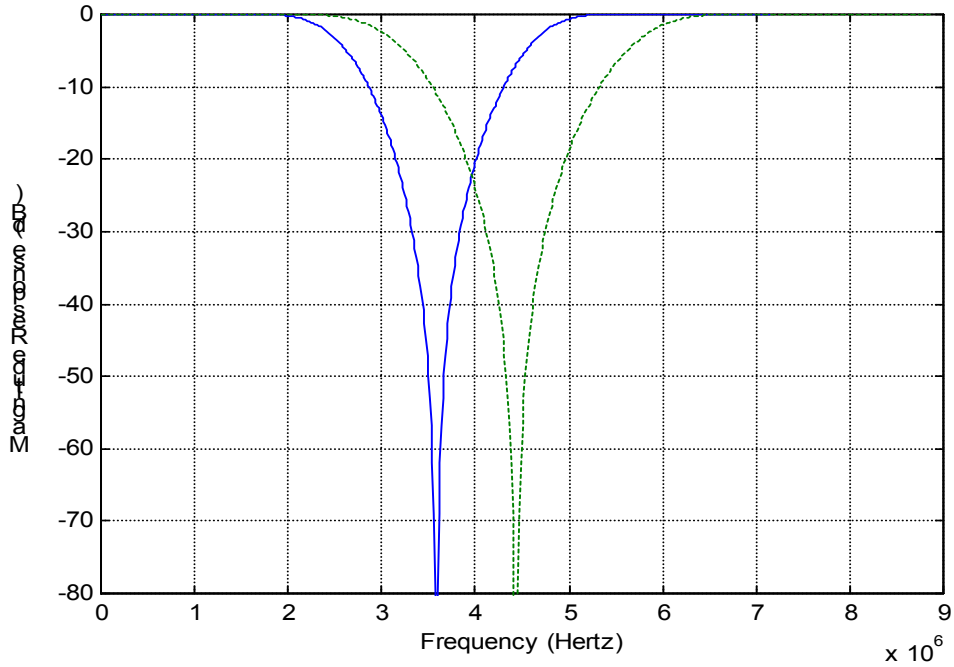
Anti-alias Filter Curve



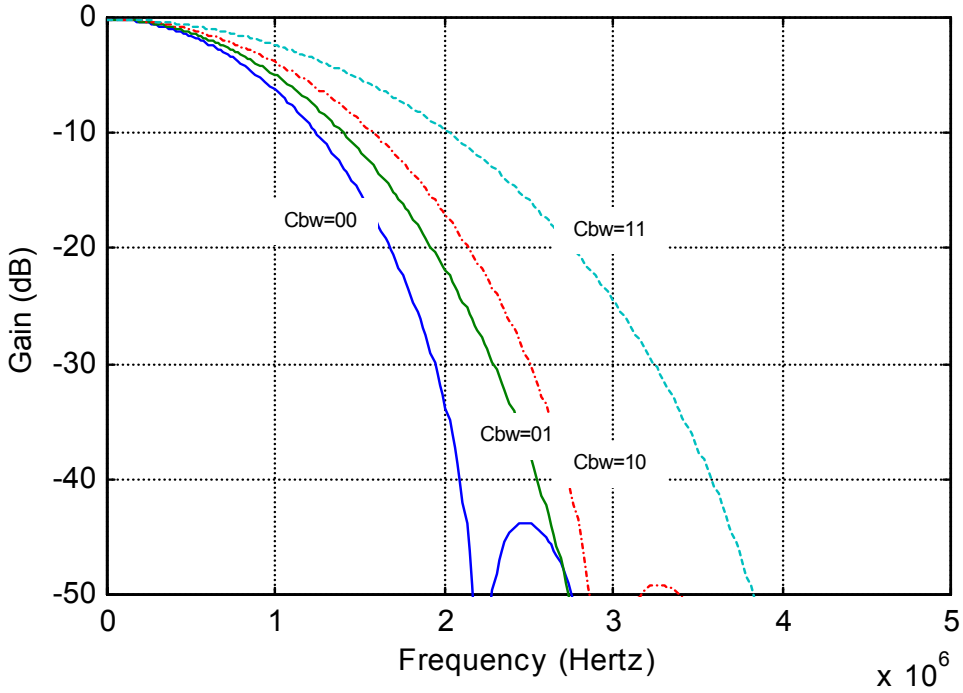
Chroma Band Pass Filter Curves



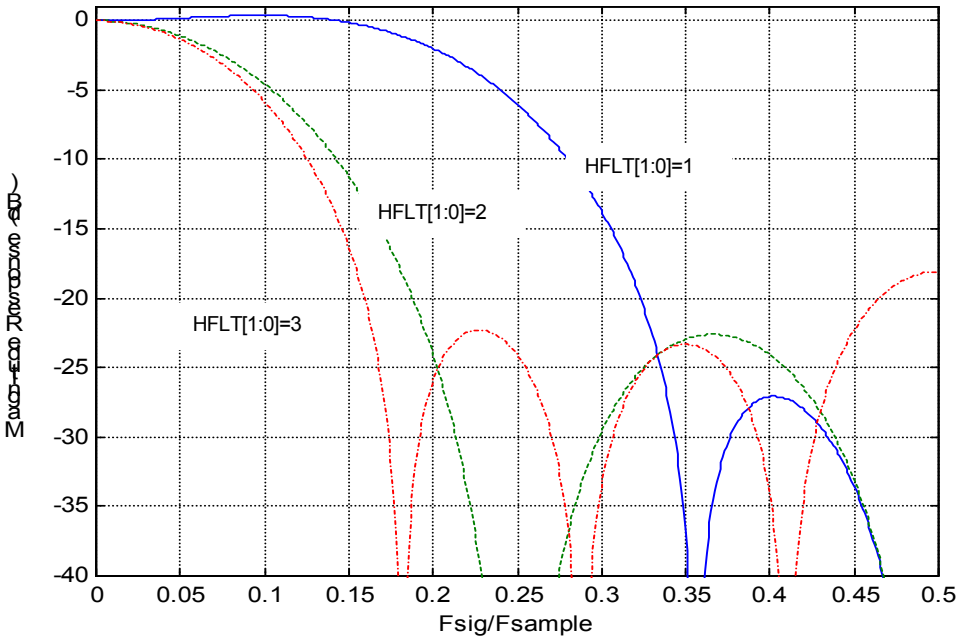
Luma Notch Filter Curve for NTSC and PAL/SECAM



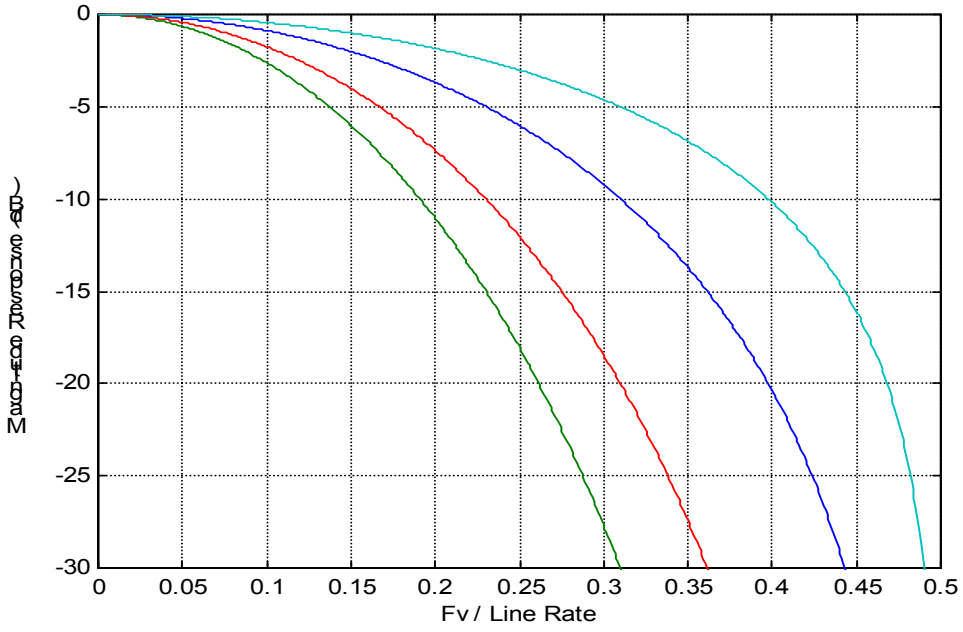
Chrominance Low-Pass Filter Curve



Horizontal Scaler Pre- Filter curves

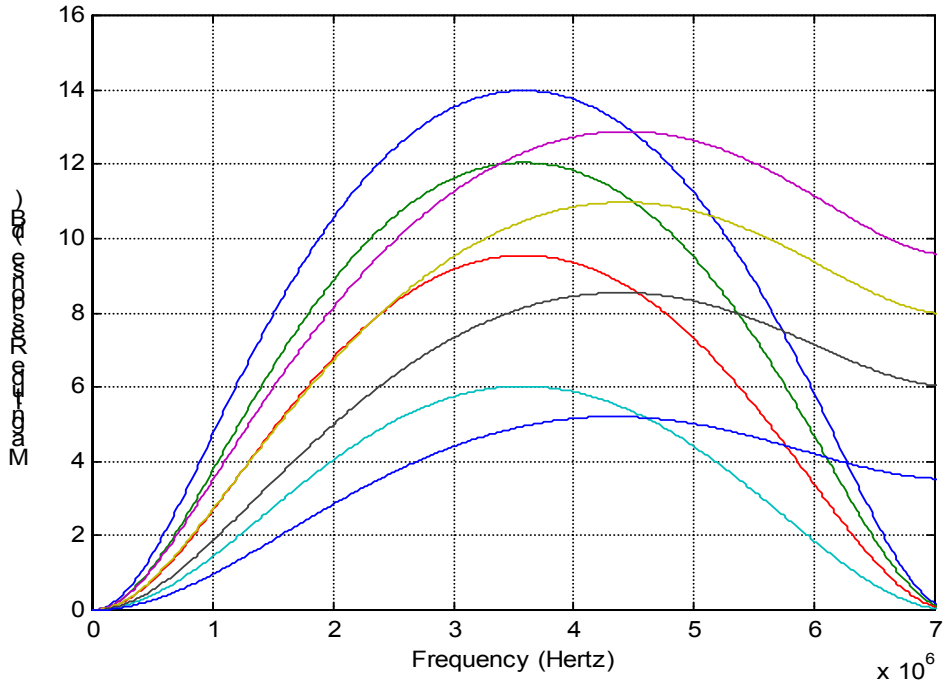


Vertical Interpolation Filter curves

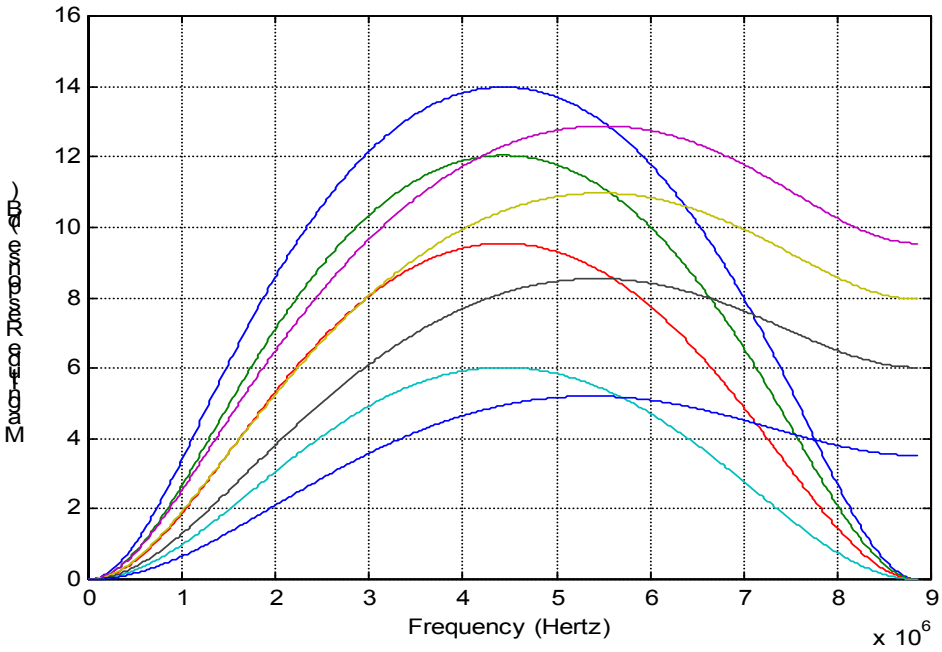


Peaking Filter Curves

NTSC



PAL



Control Register

TW9906 Register SUMMARY

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
00	ID					REV			41
01	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	00
02	YSEL2	FC27	IFSEL		YSEL		CSEL	SEL	40
03	MODE	LEN	LLCMODE	AINC	VSCTL	OEN	TRI_SEL		04
04	GMEN	CKHY		HSDLY					00
05	VSP	VSSL			HSP	HSSL			00
06	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	C_PDN	V_PDN	00
07	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
08	VDELAY_LO								12
09	VACTIVE_LO								F0
0A	HDELAY_LO								0C
0B	HACTIVE_LO								D0
0C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC
0D	VSCALE_LO								00
0E	VSCALE_HI				HSCALE_HI				11
0F	HSCALE_LO								00
10	BRIGHTNESS								00
11	CONTRAST								5C
12	SCURVE	VSF	CTI		SHARPNESS				11
13	SAT_U								80
14	SAT_V								80
15	HUE								00
16	-				-				00
17	SHCOR				-	VSHP			30
18	CTCOR		CCOR		VCOR		CIF		44
19	VBI_EN	VBI_BYT	VBI_FRAM	HA_EN	CTL656	RTSEL			58
1A	LLCTEST	PLL_PDN	MIX	VFLEN	YFLEN	YSV	CFLEN	CSV	00
1B	CK2S		CK1S		FLP	FLSL			00
1C	DTSTUS	STDNOW			ATREG	STANDARD			07
1D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	7F
1E	-	CVSTD			CVFMT				08
1F	TEST								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
20	CLPEND				CLPST				50
21	NMGAIN				WPGAIN			Agcgain[8]	22
22	AGCGAIN[7:0]								F0
23	PEAKWT								F8
24	CLMPLD	CLMPL							BC
25	SYNCTD	SYNCT							B8
26	MISSCNT				HSWIN				44
27	PCLAMP								38
28	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
29	BSHT			VSHT					00
2A	CKILMAX		CKILMIN						78
2B	HTL				VTL				44
2C	CKLM	YDLY			HFLT				30
2D	-	EVCNT	PALC	SDET	TBC_EN	BYPASS	SYOUT	HADV	10
2E	HPM		ACCT		SPM		CBW		A5
2F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0
30	SF	PF	FF	KF	CSBAD	MCVSN	CSTRIPE	CTYPE	00
31	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	00
32	HREF								X
33	FRM		YNR		CLMD		PSP		05
34	IDX		NSEN / SSEN / PSEN / WKTH						1A
35	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00
36	-								
37	-								
38	-								
39	-								
3A	-								
3B	-								
3C	-								
3D	-								
3E	-								
3F	-								
40	ACKI[7:0]								64
41	ACKI[15:8]								85
42	-		ACKI[21:16]						35
43	ACKN[7:0]								BC
44	ACKN[15:8]								DF
45							ACKN[17:16]		02
46	-		SDIV						01
47	-		LRDIV						20
48	-	APM	APG		-	ACPL	SRPH	LRPH	60

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
50	FILLDATA								A0
51	NODAEN	SYRM	SDID						22
52	ANCEN	YCBCR422	VIPCFG	DID					31
53	-								
54	-								
55	HA656	GEFOR4	HAMM84	NTSC656	VVBI				20
56	LCTL6								00
57	LCTL7								00
58	LCTL8								00
59	LCTL9								00
5A	LCTL10								00
5B	LCTL11								00
5C	LCTL12								00
5D	LCTL13								00
5E	LCTL14								00
5F	LCTL15								00
60	LCTL16								00
61	LCTL17								00
62	LCTL18								00
63	LCTL19								00
64	LCTL20								00
65	LCTL21								00
66	LCTL22								00
67	LCTL23								00
68	LCTL24								00
69	LCTL25								00
6A	LCTL26								00
6B	HSBEGIN								2C
6C	HSEND								44
6D	OVSDLY								00
6E	HSPIN	OFDLY			VSMODE	OVSEND			20
6F	PdnSVBI	CLKPLL	VBIDELAY						11

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
94	0	0	BTAT1004 FLD	F2VCNT	F2VDELAY[9:8]		F2VACTIVE[9:8]		01
95	F2VDELAY[7:0]								21
96	F2VACTIVE[7:0]								E6
97	REGSTATUS1MODE								00
98	REGSTATUS2MODE								00
99	REGSTATUS3MODE								00
9A	00		YCONT INV	VVALID MODE	INTRAW CLEAR	VCHIP TEST	VCHIP FLD	ANCDVEN	0A
9B	F1MASK1				F1PAT1				F7
9C	F1MASK2				F1PAT2				FF
9D	F1MASK3				F1PAT3				00
9E	F1MASK4				F1PAT4				00
9F	F1MASK5				F1PAT5				00
A0	F2MASK1				F2PAT1				F7
A1	F2MASK2				F2PAT2				FF
A2	F2MASK3				F2PAT3				00
A3	F2MASK4				F2PAT4				00
A4	F2MASK5				F2PAT5				00
A5	ANC MODE	SVBIRAM MODE	TTXFREN	FILLOGIC		FILE MODE	FIL2EN	FIL1EN	27
A6	TTXFRMASK								FF
A7	TTXFRPAT								27
A8	GEM2XMASK[7 :0]								FF
A9	VITCCRC OEN	GEN2XMASK[10:8]			CCNULFIL	GEN2XPAT[10:8]			7D
AA	GEM2XPAT[7:0]								B9
AB	GEM2XFIL EN	TTX ERROR	VPS ERROR	GEM2X ERROR	GEM1X ERROR	VITC ERROR	WSS ERROR	CCEDS ERROR	FF
AC	-							SVBIRAM RST	00
AD	FTHRESHOLD								90
AE	F1LIEN	F2LIEN	LINENUMBER[5:0]						1A
AF	INTTYPE	INTPOL	VBIREGLOADLINE[5:0]						1A
B0	INT1 MASK								00
B1	INT2 MASK								00
B2	INT3 MASK								00
B3	INT1 CLEAR								00
B4	INT2 CLEAR								00
B5	INT3 CLEAR								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
B6	HVLOCKSTCHANGED	MACROSTCHANGED	EDSSTDET	VCHIP_CHANGED_DET	GEM1XF2_DET	GEM1XF1_DET	GEN2XF2_DET	GEN2XF1_DET	00
B7	STANDARDCHANGED	LINE_INT	FIFOFULL	FIFOTHRS	NO_VITC_CRC_ERROR	VITC_DET	VPS_CHANGED	VPS_DET	00
B8	WST_DET	NO_WSS525_CRC_ERROR	WSS_CHANGED	WSS_DET	NO_CCF2_NULL	CCF2_DET	NO_CCF1_NULL	CCF1_DET	00
B9	INT1 STATUS								00
BA	INT2 STATUS								00
BB	INT3 STATUS								00
BC	SVBICOUNT								00
BD	CCF1DATA[7:0]								80
BE	CCF1DATA[15:8]								80
BF	CCF2DATA[7:0]								80
C0	CCF2DATA[15:8]								80
C1	VITCFRAME1[7:0]								00
C2	VITCFRAME2[7:0]								00
C3	VITCSEC1[7:0]								00
C4	VITCSEC2[7:0]								00
C5	VITCMIN1[7:0]								00
C6	VITCMIN2[7:0]								00
C7	VITCHOURS1[7:0]								00
C8	VITCHOURS2[7:0]								00
C9	VITCCRC[7:0]								00
CA	WSS_ALLDATA[7:0]/ { WSS525_CRC_ERROR, WSS_FLD, WSS_ALLDATA[5:0] }								00
CB	{WSS_DET, WSS_FLD, WSS_ALLDATA[13:8]} / WSS_ALLDATA[13:6]								00
CC	VPSDATA1/ GEM2XF1FRAME[7:0]								00
CD	VPSDATA2/ GEM2XF1FRAME[10:8]								00
CE	VPSDATA3/ GEM2XF1DATA[7:0]								00
CF	VPSDATA4/ GEM2XF1DATA[15:8]								00
D0	VPSDATA5/ GEM2XF1DATA[23:16]								00
D1	VPSDATA6/ GEM2XF1DATA[31:24]								00
D2	VPSDATA7/ GEM1XF1DATA[7:0]								00
D3	VPSDATA8/ GEM1XF1DATA[15:8]								00
D4	VPSDATA9/ GEM2XF2FRAME[7:0]								00
D5	VPSDATA10 / GEM2XF2FRAME[10:8]								00
D6	VPSDATA11/ GEM2XF2DATA[7:0]								00
D7	VPSDATA12 / GEM2XF2DATA[15:8]								00
D8	VPSDATA13/ GEM2XF2DATA[23:16]								00
D9	VPSSCODE[7:0] / GEM2XF2DATA[31:24]								00
DA	VPSSCODE[15:8] / GEM1XF2DATA[7:0]]								00
DB	TFCODE/ GEM1XF2DATA[15:8]								00
DC	0	VCHIP_R[2:0]			VCHIP_A[3:0]				0F
DD	00		VCHIP_V	VCHIP_S	0	VCHIP_G[2:0]			00
DE	TFCODE								00
DF	SVBIRDATA								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
E0	TIMEOFDAY	UNDEFINED	RESERVED	PUBLICSERVICE	MISCELLANEOUS	CHANNEL	FUTURE	CURRENT	**00**
E1	0	EDSDATA1							**00**
E2	0	EDSDATA2							**00**
E3	0	EDSDATA3							**00**
E4	0	EDSDATA4							**00**
E5	0	EDSDATA5							**00**
E6	0	EDSDATA6							**00**
E7	0	EDSDATA7							**00**
E8	-	EDSDATA8							**00**
E9	-	EDSDATA9							**00**
EA	-	EDSDATA10							**00**

0x00 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-3	ID	R	The TW9906 Product ID code is 01000.	8h
2-0	Revision	R	The revision number.	1

0x01 – Chip Status Register I (STATUS1)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by Misscnt register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2			Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0x02 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7	YSEL2	R/W	See YSEL	0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	11 = Progressive video decoding 10 = Component video decoding 01 = S-video decoding 00 = Composite video decoding	0
3-2	YSEL	R/W	YSEL2 together with these two bits control the Y input video selection. 000 = Route MUX0 input to MXOUT 001 = Route MUX1 input to MXOUT 010 = Route MUX2 input to MXOUT 011 = Route MUX3 input to MXOUT 100 = Route VIN1/MUX4 input to MXOUT 101-111 = Invalid	0
1	CSEL	R/W	This bit selects the chroma channel input. 0 = CIN0 1 = CIN1	0
0	VSEL	R/W	This bit select the V channel input 0 = VIN0 1 = VIN1	0

0x03 – Output Format Control Register (OPFORM)

Bit	Function	R/W	Description	Reset
7	MODE	R/W	0 = CCIR601 compatible YCrCb 4:2:2 format with separate syncs and flags. 1 = ITU-R-656 compatible data sequence format.	0
6	LEN	R/W	0 = 8/10-bit YCrCb 4:2:2 output format. 1 = 16/20-bit YCrCb 4:2:2 output format.	0
5	LLCMODE	R/W	1 = LLC output mode. 0 = free-run output mode	0
4	AINC	R/W	Serial interface indexing control 0 = auto-increment 1 = non-auto	0
3	VSCTL	R/W	1 = Vertical scale-downed output controlled by DVALID only. 0 = Vertical scale-downed output controlled by both HACTIVE and DVALID.	0
2	OEN	R/W	0 = Enable outputs. 1 = Tri-state outputs defined by Tri-state select bits of this register.	1
1-0	TRI_SEL	R/W	These bits select the outputs to be tri-stated when the OEN bit is asserted high. There are three major groups that can be independently tri-stated: timing group (HSYNC, VSYNC, DVALID, MPOUT, FIELD), data group (VD[19:0]), and clock group (CLKX1, CLKX2) according to following definition. 00 = Timing and data group only. 01 = Data group only. 10 = All three groups. 11 = Clock and data group only.	0

0x04 – HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	GMEN	R/W	Reserved for test.	0
6-5	CKHY	R/W	Color killer hytheresis 0 – fastest 1 – fast 2 – medium 3 - slow	0
4-0	HSDLY	RW	Reserved for test.	0

0x05 – Output Control I

Bit	Function	R/W	Description	Reset
7	VSP	R/W	0 = VSYNC pin output polarity is active low 1 = VSYNC pin output polarity is active high.	0
6-4	VSSL	R/W	VSYNC pin output control 0 = VSYNC 1 = VACT 2 = HACT 3 = VVALID 4 - 7 = Reserved	0
3	HSP	R/W	0 = HSYNC pin output polarity is active low 1 = HSYNC pin output polarity is active high.	0
2-0	HSSL	R/W	HSYNC pin output control 0 = HACT 1 = HSYNC 2 = VSYNC 3 = HLOCK 4 – 7 = Reserved	0

0x06 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	An 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference increase 30%.	0
5	VREF	R/W	0 = Internal voltage reference. 1 = Internal voltage reference shut down.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKX1 and CLKX2) are still active.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	0
0	V_PDN	R/W	0 = V channel ADC in normal operation 1 = V channel ADC in power down mode.	0

0x07 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0x08 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_ LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0x09 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_ LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0

0x0A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_ LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	0C

0x0B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE _LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0x0C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	1 = Bypass Comb filter when no burst presence 0 = No bypass	0
0	PDLY	R/W	PAL delay line. 1 = enabled. 0 = disabled.	0

0x0D – Vertical Scaling Register, Low (VSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	VSCALE_LO	R/W	These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register	00

0x0E – Scaling Register, High (SCALE_HI)

Bit	Function	R/W	Description	Reset
7-4	VSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register.	1
3-0	HSCALE_HI	R/W	These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register.	1

0x0F – Horizontal Scaling Register, Low (HSCALE_LO)

Bit	Function	R/W	Description	Reset
7-0	HSCALE_ LO	R/W	These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register.	00

0x10 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0x11 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CNTRST	R/W	These bits control the contrast. They have value of 0 to 3.98 (FFh). A value of 1 (`100_0000`) has no effect on the video data.	5C

0x12 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the sharpness filter center frequency. 0 = Normal 1 = High	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = hightest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image and '15' being the strongest.	1

0x13 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x14 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x15 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from $+36^{o}$ (7Fh) to -36^{o} (80h) with an increment of 0.28^{o}. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0^{o} (00h). This is effective only on NTSC system.	00

0x16 –

Bit	Function	R/W	Description	Reset
7-0		R/W	Reserved	0

0x17 – Vertical Sharpness (VSHARP)

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	3
3			Reserved	0
2-0	VSHP	R/W	Vertical peaking level. 0 = none. 7 = highest.	0

0x18 – Coring Control Register (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0x19 – VBI Control Register (VBICNTL)

Bit	Function	R/W	Description	Reset
7	VBI_EN	R/W	0 = VBI capture disabled. 1 = VBI capture enabled.	0
6	VBI Byte Order	R/W	If LEN(Reg0x03[6]) is “1” 0 = Pixel 1, 3, 5 … on the VD[19:10] data bus, and pixel 2, 4, 6, … on the VD[9:0] data bus. 1 = Pixel 1, 3, 5, … on the VD[9:0] data bus, and pixel 2, 4, 6, … on the VD[19:10] data bus. If LEN is “0” 0 = Pixel 2,1,4,3,6,5,…. on the VD[19:10] data bus. 1 = Pixel 1,2,3,4,5,6,…. on the VD[19:10] data bus.	1
5	VBI_FRAM	R/W	0 = Normal mode 1 = ADC data output mode	0
4	HA_EN	R/W	0 = HACTIVE output is disabled during vertical blanking period. 1 = HACTIVE output is enabled during vertical blanking period.	1

3	CNTL656	R/W	0 = 0x80 and 0x10 code will be output as invalid data during active video line. 1 = 0x00 code will be output as invalid data during active video line.	1
2-0	RTSEL	R/W	These bits control the real time signal output from the MPOUT pin. 000 = Video loss 001 = H-lock 010 = S-lock 011 = V-lock 100 = MONO 101 = Det50 110 = LVALID 111 = RTCO	0

0x1A – Analog Control II

Bit	Function	R/W	Description	Reset
7	LLCTEST	R/W	LLC test mode	0
6	PLL_PDN	R/W	0 = LLC PLL in normal operation. 1 = PLL in power down mode.	0
5	MIX	R/W	YBOUT control 1 = Y+C 0 = Y	0
4	VFLEN	R/W	V-Ch anti-alias filter control 1 = enable 0 = disable	0
3	YFLEN	R/W	Y-Ch anti-alias filter control 1 = enable 0 = disable	0
2	YSV	R/W	Reduced power mode 1 = enable 0 = disable	0
1	CFLEN	R/W	C-Ch anti-alias filter control 1 = enable 0 = disable	0
0		R/W	Reserved	0

0x1B – Output Control II

Bit	Function	R/W	Description	Reset
7-6	CK2S	R/W	CLKX2 pin output control 0 = CLKX2 1 = VCLK 2 = LLCK 3 = LLCK2	0
5-4	CK1S	R/W	CLKX1 pin output control 0 = VCLK 1 = CLKX1 2 = LLCK 3 = LLCK4	0
3	FLP	R/W	0 = FIELD pin output polarity is active high 1 = FIELD pin output polarity is active low.	0
2-0	FLSL	R/W	FIELD pin output control 0 = FIELD 1 = V-lock 2 = S-lock 3 = Vdloss 4 – 7 = Reserved	0

0x1C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0x1D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x1E – Component Video Format (CVFMT)

Bit	Function	R/W	Description	Reset
7		R	Reserved	0
6-4	CVSTD	R	Component video input format detection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p	0
3-0	CVFMT	R/W	Component video format selection. 0 = 480i, 1 = 576i, 2 = 480p, 3 = 576p, 8 = Auto	8

0x1F – Test Control Register (TEST)

Bit	Function	R/W	Description	Reset
7-0	TEST	R/W	This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 1 = Analog test mode. Y and C channel portion of the device can be tested in this mode. The Y channel ADC output can be obtained from VD[19:10] for bit9 to bit0 respectively. The C channel ADC output can be obtained from VD[9:0] for bit9 to bit0 respectively. 2 = Analog test mode. V portion of the device can be tested in this mode. The V channel ADC output can be obtained from VD[19:10] for bit9 to bit0 respectively. 3 = Reserved 4 = Digital test mode1. This is the CVBS test mode. The 8-bit input corresponds to VD[9:2] in the order of bit 9 to bit2. 5 = Digital test mode 2. This is the Y/C test mode. This test mode allows the C channel data to be inputted from VD[19:12] in addition to Y. 6 = Digital test mode 3. This is the V test mode. In addition to the digital test mode 1 and 2, the V channel data can be input from VD[19:12]. 9 = Sync output mode. The 6-bit Sync output corresponds to VD[5:0] in the order of bit 5 to 0. Y and Cb/Cr outputs correspond to VD[19-10] in 422 format B = Analog ADC CLAMP test mode, Clamp control YU, YUX, YD, YDX, CU, CUX, CD, CDX, VU, VUX, VD, and VDX are mapped to VD[3-0]. FF = SVBI 512 RAM test mode.	0

0x20 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping. It is referenced to PCLAMP position.	0

0x21 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	2
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN 8	R/W	This bit is the MSB of the 9-bit register that controls the AGC gain when AGC loop is disabled.	0

0x22 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 9-bit register that controls the AGC gain when AGC loop is disabled.	F0

0x23 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' can disable this function.	F8

0x24– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0x25– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0x26 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	MISSCNT[3] controls the speed of VDLOSS detection with '0' being fast and '1' being slow. MISSCNT[2:0] control the threshold of horizontal sync miss detection per field.	4
3-0	HSWIN	R/W	These bits determine the VCR mode Hsync detection window.	4

0x27 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	32

0x28 – Vertical Control I (VCNTL1)

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = long 0 = normal	0

0x29 – Vertical Control II (VCNTL2)

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control.	0

5-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0x2A – Color Killer Level Control (CKILL)

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	28

0x2B – Comb Filter Control (COMB)

Bit	Function	R/W	Description	Reset
7-4	HTL	R/W	Adaptive Comb filter control.	4
3-0	VTL	R/W	Adaptive Comb filter combing strength control. Higher value provides stronger comb filtering.	4

0x2C – Luma Delay and H Filter Control (LDLY)

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
3-0	HFLT	R/W	If HFLT[3] = 1, peaking with strength indicated by HFLT[2-0]. If HFLT[3] = 0, HFLT[2-0] : Pre-filter selection for horizontal scaler. 1** = Bypass 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image 010 = Recommended for QCIF size image 011 = Recommended for ICON size image	0

0x2D – Miscellaneous Control I (MISC1)

Bit	Function	R/W	Description	Reset
7	Reserved	R/W		0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	3
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	TBC_EN	R/W	1 = Internal TBC enabled.(test purpose only) 0 = TBC off.	0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	0
1	SYOUT	R/W	1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled	0
0	HADV	R/W	This bit advances the HACTIVE and DVALID pin output by one data clock when set.	0

0x2E – LOOP Control Register (LOOP)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Slow	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0x2F – Miscellaneous Control II (MISC2)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch function. 0 = Disabled.	0

0x30 – Macrovision Detection (MVSN)

Bit	Function	R/W	Description	Reset
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. Cstripe=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0x31 – Chip STATUS II (STATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	R	VCR signal indicator	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	0
1	EDSDET	R	1 = EDS data detected. 0 = Not detected.	0
0	CCDET	R	1 = CC data detected. 0 = Not detected.	0

0x32 – H monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF	R	Horizontal line frequency indicator	X

0x33 – CLAMP MODE (CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode control 0 = Auto 2 = default to 60Hz 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None 1 = smallest 2 = small 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Sync detection level control 0 = low 1 = medium 2 = high 3= highest	1

0x34 – ID Detection Control (IDCNTL)

Bit	Function	R/W	Description	Reset
7-6	IDX	R/W	These two bits indicates which of the four lower 6-bit registers is currently be controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the selected register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0x35 – Clamp Control I (CLCNTL1)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control for debugging use.	0
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5	CCLEN	R/W	1 = C channel clamp disabled 0 = Enabled.	0
4	VCLEN	R/W	1 = V channel clamp disabled 0 = Enabled.	0
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x40 – Audio Clock Increment (ACKI)

Bit	Function	R/W	Description	Reset
7-0	ACKI	R/W	Bit 7-0 of ACKI	64

0x41 – Audio Clock Increment (ACKI)

Bit	Function	R/W	Description	Reset
7-0	ACKI	R/W	Bit 15-8 of ACKI	85

0x42 – Audio Clock Increment (ACKI)

Bit	Function	R/W	Description	Reset
5-0	ACKI	R/W	Bit 21-16 of ACKI	35

0x43 – Audio Clock Number (ACKN)

Bit	Function	R/W	Description	Reset
7-0	ACKN	R/W	Bit 7-0 of Audio clock number per field	BC

0x44 – Audio Clock Number (ACKN)

Bit	Function	R/W	Description	Reset
7-0	ACKN	R/W	Bit 15-8 of ACKN	DF

0x45 – Audio Clock Number (ACKN)

Bit	Function	R/W	Description	Reset
1-0	ACKN	R/W	Bit 17-16 of ACKN	2

0x46 – Serial Clock Divider (SDIV)

Bit	Function	R/W	Description	Reset
5-0	SDIV	R/W	Serial Clock divider	01

0x47 – Left/Right Clock Divider (LRDIV)

Bit	Function	R/W	Description	Reset
5-0	LRDIV	R/W	Left/Right Clock divider	20

0x48 – Audio Clock Control (ACCNTL)

Bit	Function	R/W	Description	Reset
6	APZ	R/W	Loop control	1
5-4	APG	R/W	Loop control	2
2	ACPL	R/W	0 = Loop closed 1 = Loop open	0
1	SPH	R/W	ASCLK divider trigger phase. 0 = falling edge 1 = rising edge	0
0	LRPH	R/W	ALRCLK divider trigger phase 0 = falling edge 1 = rising edge	0

0x50 – FILLDATA

Bit	Function	R/W	Description	Reset
7-0	FILLDATA	R/W	Filled data as dummy data in ANC Dword data packet.	A0

0x51 – SDID

Bit	Function	R/W	Description	Reset
7	NODAEN	R/W	1:Bit7 in 4th byte of EAV/SAV code will be 0 when sync lost(No Video input.) 0: Bit7 in 4th byte of EAV/SAV is always VIPCFG register bit.	0
6	SYRM	R/W	1: Minimum value in raw VBI will be 0x10 for Sync Level remove. 0:none.	0
5-0	SDID	R/W	Secondary data ID in ANC data packet type 2	22

0x52 – DID

Bit	Function	R/W	Description	Reset
7	ANCEN	R/W	1:ANC data packet output enable. 0:disable.	0
6	YCBCR422	R/W	1: Averaging 4:2:2 output 0:Normal 4:2:2 output	0
5	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code.	1
4-0	DID	R/W	Data ID in ANC data packet type 2.	11

0x55 – VVBI

Bit	Function	R/W	Description	Reset
7	HA656	R/W	1:HACTIVE signal is same as DVALID signal in H-Down Scaled video output. 0:HACTIVE signal is always HACTIVE register's length.	0
6	GEFOR4	R/W	1:Special VIP output mode. 0:normal VIP(ITU-R656) output mode.	0
5	HAMM84	R/W	1:enable 84 Hamming Code checking BI Slicer. 0:disable.	0
4	NTSC656	R/W	1:Number of Even Field Video output line is (the number of Odd field Video output line – 1).This bit is required for ITU-R BT.656 output for 525 line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line.	0
3-0	VVBI	R/W	The number of raw VBI data output line counted from top video active line signal timing.	0

0x56~6A LCTL6~LCTL26

Bit	Function	R/W	Description	Reset
7-4	LCTLn	R/W	Set up VBI Data Slicer Decoding mode on Line-n in Odd field Value is set up by bellow bit3-0 meaning for line-n in Odd field.	0
3-0		R/W	Set up VBI Data Slicer Decoding mode on Line-n in Even field. 0h:disable decoding. 1h:Teletext-B 2h:Teletext-C 3h:Teletext-D 4h:Closed Captioning and Extended Data service.(EIA-608 type). 5h:CGMS(WSS525) in 525 line system or WSS625 in 625 line system. 6h:VITC 7h:Gemstar 1x 8h:Gemstar 2x 9h:VPS(Line16 VPS type) Ah:Teletext-A Bh~Fh:reserved	0

0x6B – HSGEGIN

Bit	Function	R/W	Description	Reset
7-0	HSBEGIN	R/W	HSYNC Start position.	2C

0x6C – HSEND

Bit	Function	R/W	Description	Reset
7-0	HSEND	R/W	HSYNC End position.	44

0x6D – OVSDLY

Bit	Function	R/W	Description	Reset
7-0	OVSDLY	R/W	VSYNC Start position.	00

0x6E – OVSEND

Bit	Function	R/W	Description	Reset
7	HSPIN	R/W	1:HSYNC output is HACTIVE. 0:HSYNC output is HSYNC.	0
6-4	OFDLY	R/W	FIELD output delay. 0h:0H line delay FIELD output.(601 mode only) 1h-6h: 1H-6H line delay FIELD output. 7h:Reserved.	2
3	VSMODE	R/W	1:VSYNC output is HACTIVE-VSYNC mode. 0:VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0x6F – VBIDELAY

Bit	Function	R/W	Description	Reset
7	PDNSVBI	R/W	1:Enable VBI Data Slicer,0:reset and power down VBI Data Slicer. If this bit is 0,all Sliced VBI functions are disable and in power down mode.	0
6	CLKPLL	R/W	1:External Clock input function for OUTPUT interface.(Test purpose only). 0:normal mode.	0
5-0	VBIDELAY	R/W	Raw VBI output delay	11

0x94 – F2VCNT

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		00
5	BTAT1004 FLD	R/W	1:BTA T-1004 F bit Output in EAV/SAV word on Progressive Video Data output 0:none	0
4	F2VCNT	R/W	1:Field 2 VDELAY and VACTIVE are controlled by F2VDELAY and F2VACTIVE. 0:Field 2 VDELAY and VACTIVE are controlled by VDELAY and VACTIVE	0
3-2	F2VDELAY_HI	R/W	These bits are bit9 to 8 of the 10-bit Field2 Vertical Delay register.	00
1-0	F2VACTIVE_HI	R/W	These bits are bit9 to 8 of the 10-bit Field2 Vertical Active register.	01

0x95 – F2VDELAY_LO

Bit	Function	R/W	Description	Reset
7-0	F2VDELAY_LO	R/W	These bits are bit7 to 0 of the 10-bit Field2 Vertical Delay register.	21

0x96 – F2VACTIVE_LO

Bit	Function	R/W	Description	Reset
7-0	F2VACTIVE_LO	R/W	These bits are bit7 to 0 of the 10-bit Field2 Vertical Active register.	E6

0x97 – STATUS1MODE

Bit	Function	R/W	Description	Reset
7-6	STATUS1 MODE	R/W	If this Bit-n is 0,STATUS1 Register Bit-n is INT status(set by INT raw status signal 0 to 1 rising edge,reset by write 1 in INT1 CLEAR Register Bit-n). If this Bit-n is 1,STATUS1 Register Bit-n is INT raw status.	00

0x98 – STATUS2MODE

Bit	Function	R/W	Description	Reset
7-6	STATUS2 MODE	R/W	If this Bit-n is 0,STATUS2 Register Bit-n is INT status (set by INT raw status signal 0 to 1 rising edge, reset by write 1 in INT2 CLEAR Register Bit-n). If this Bit-n is 1,STATUS2 Register Bit-n is INT raw status.	00

0x99 – STATUS3MODE

Bit	Function	R/W	Description	Reset
7-6	STATUS3 MODE	R/W	If this Bit-n is 0,STATUS3 Register Bit-n is INT status (set by INT raw status signal 0 to 1 rising edge, reset by write 1 in INT3 CLEAR Register Bit-n). If this Bit-n is 1,STATUS3 Register Bit-n is INT raw status.	00

0x9A – INTRAWCLEAR

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		00
5	YCOUTINV	R/W	0:VD[19:10],VD[9:0] pin output normal. 1:VD[19:10],VD[9:0] pin output inverse.(Test purpose only)	0
4	VVALIDMODE	R/W	0:VVALID(LVLAID) is generated independently.(normal mode) 1:VVALID(LVALIUD) is same as VACTIVE.(Test purpose only)	0
3	INTRAWCLEAR	R/W	0:INT raw status signal is not cleared by start of VSYNC per each field. 1:INT raw status signal is cleared by start of VSYNC per each field. This bit “1” is required if INT STATUS register bit is needed to set to “1” after detection per each field with cleared to “0” by start of VSYNC.	1
2	VCHIPTEST	R/W	0:normal mode. 1:VCHIP Test purpose only.	0
1	VCHIPFLD	R/W	0:VCHIP detection is executed on field 1.(Test purpose only) 1:VCHIP detection is executed on field2.(normal mode)	1
0	ANCDVEN	R/W	0:Not output ANC packet DVALID signals. 1:ANC packet DVALID signal output enable. DVALID signal is valid during ANC packet output timing, 0x00(start code) to BC(end code)	0

0x9B – TTXF1MASKPAT1

Bit	Function	R/W	Description	Reset
7-4	F1MASK1	R/W	1st 4Bit Nibble data masking pattern on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1.	F
3-0	F1PAT1	R/W	1 ST 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1	7

0x9C – TTXF1MASKPAT2

Bit	Function	R/W	Description	Reset
7-4	F1MASK2	R/W	2nd 4Bit Nibble data masking pattern on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1.	F
3-0	F1PAT2	R/W	2nd 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1	F

0x9D – TTXF1MASKPAT3

Bit	Function	R/W	Description	Reset
7-4	F1MASK3	R/W	3rd 4Bit Nibble data masking pattern on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1.	0
3-0	F1PAT3	R/W	3rd 4Bit Nibble data on 84Hamming data bytes in Teletext packet required to be filtered in TTX Filter1	0

0x9E – TTXF1MASKPAT4

Bit	Function	R/W	Description	Reset
7-4	F1MASK4	R/W	4th 4Bit Nibble data masking pattern on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1.	0
3-0	F1PAT4	R/W	4th 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1	0

0x9F – TTXF1MASKPAT5

Bit	Function	R/W	Description	Reset
7-4	F1MASK5	R/W	5th 4Bit Nibble data masking pattern on 84Hamming data bytes in Teletext packet that requires be filtered in TTX Filter1.	0
3-0	F1PAT5	R/W	5th 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter1	0

0xA0 – TTXF2MASKPAT1

Bit	Function	R/W	Description	Reset
7-4	F2MASK1	R/W	1st 4Bit Nibble data masking pattern on 84Hamming data bytes In Teletext packet that requires to be filtered in TTX Filter2.	F
3-0	F2PAT1	R/W	1st 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2	7

0xA1 – TTXF2MASKPAT2

Bit	Function	R/W	Description	Reset
7-4	F2MASK2	R/W	2nd 4Bit Nibble data mask pattern on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2.	F
3-0	F2PAT2	R/W	2nd 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2	F

0xA2 – TTXF2MASKPAT3

Bit	Function	R/W	Description	Reset
7-4	F2MASK3	R/W	3rd 4Bit Nibble data mask pattern on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2.	0
3-0	F2PAT3	R/W	3rd 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2	0

0xA3 – TTXF2MASKPAT4

Bit	Function	R/W	Description	Reset
7-4	F2MASK4	R/W	4th 4Bit Nibble data mask pattern on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2.	0
3-0	F2PAT4	R/W	4th 4Bit Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2	0

0xA4 – TTXF2MASKPAT5

Bit	Function	R/W	Description	Reset
7-4	F2MASK5	R/W	5th 4Bit Nibble data mask pattern on 84Hamming data bytes in Teletext packet requires to be filtered in TTX Filter2.	0
3-0	F2PAT5	R/W	5th Nibble data on 84Hamming data bytes in Teletext packet that requires to be filtered in TTX Filter2	0

0xA5 – TTXFILCTL

Bit	Function	R/W	Description	Reset
7	ANCMODE	R/W	0:ANC Packet header type0. 1:ANC Packet Hearer type1. Type1 is same as TW9905C ANC Packet header.	0
6	SVBIRAMMODE	R/W	0:only Teletext ANC packets are stored in sliced VBI RAM. 1:All ANC packets are stored in sliced VBI RAM.	0
5	TTXFREN	R/W	1:Teletext Framing code is filtered. 0: not filtered.	1
4-3	FILLOGIC	R/W	Teletext Filter1 and Filter 2 pass mode selection 00:NOR, 01:NAND, 10:OR, 11:AND	00
2	FILMODE	R/W	Teletext nibble data filter mode. 0:5 header nibble data are filtered. 1:2 header nibble data are filtered.	1
1	FIL2EN	R/W	1:enable Teletext header nibble data filter2, 0:disable	1
0	FIL1EN	R/W	1:enable Teletext header nibble data filter1, 0:disable	1

0xA6 – TTXFRMASK

Bit	Function	R/W	Description	Reset
7-0	TTXFRMASK	R/W	Set up 1byte Teletext Framing Code mask pattern. If bit-n is 0,bit-n in Framing code is masked in framing code filter.	FF

0xA7 – TTXFRPAT

Bit	Function	R/W	Description	Reset
7-0	TTXFRPAT	R/W	Set up 1byte Teletext Framing Code pattern to be filtered. Default 0x27 is 625 WST-B Teletext Framing code pattern.	27

0xA8 – GEM2XMASK_LO

Bit	Function	R/W	Description	Reset
7-0	GEM2XMASK_LO	R/W	Set up bit7 to 0 of Gemstar2x Frame code mask pattern to be filtered.	FF

0xA9 – GEM2X_HI

Bit	Function	R/W	Description	Reset
7	VITCCRCOEN	R/W	0:VITCCRC register has only 0x00(no VITC error) and 0x01(VITC error). 1:VITCCRC register has 8bits VITC CRC data.	0
6-4	GEM2XMASK_HI	R/W	Set up bit10 to 8 of Gemstar2x Frame code mask pattern to be filtered.	7
3	CCNULFIL	R/W	0:disable CC NUL filter 1:Enable CC NULL filter. If this bit is “1”, Field1 CC and Filed2 CC don’t have NULL data pattern {0x80,0x80} on those registers and ANC packets.	1
2-0	GEM2XPAT_HI	R/W	Set up bit10 to 8 of Gemstar2x Frame code pattern to be filtered.	5

0xAA – GEM2XPAT_LO

Bit	Function	R/W	Description	Reset
7-0	GEM2XPAT_LO	R/W	Set up bit7 to 0 of Gemstar2x Frame code pattern to be filtered.	B9

0xAB – SVBIERRORMODE

Bit	Function	R/W	Description	Reset
7	GEM2XFILEN	R/W	0:disable GEMSTAR2X Frame code filter. 1:enable GEMSTAR2X Frame code filter.	1
6	TTXERROR	R/W	0:always output Teletext ANC Packets. 1:don't output Teletext ANC Packets if detection error.	1
5	VPSERROR	R/W	0:always output VPS ANC Packets. 1:don't output VPS ANC Packets if detection error.	1
4	GEM2XERROR	R/W	0:always output GEMSTAR2X ANC Packets. 1:don't output GEMSTAR2X ANC Packets if detection error.	1
3	GEM1XERROR	R/W	0:always output GEMSTAR1X ANC Packets. 1:don't output GEMSTAR1X ANC Packets if detection error.	1
2	VITCERROR	R/W	0:always output VITC ANC Packets. 1:don't output VITC ANC Packets if detection error.	1
1	WSSERROR	R/W	0: always output WSS ANC packets. 1:don't output WSS ANC packets if detection error.	1
0	CCEDSERROR	R/W	0:always output field 1 and field2 CC ANC packets.. 1:don't output field 1 and field 2 CC ANC packets if detection error.	1

0xAD – FTHRESHOLD

Bit	Function	R/W	Description	Reset
7-0	FTHRESHOLD	R/W	FIFOTHRES raw status register is "1" while the number of words in sliced VBI RAM is more than this register value.	70

0xAE – LINENUMBERINT

Bit	Function	R/W	Description	Reset
7	F1LIEN	R/W	0:disble LINE_INT during filed 1. 1:enable LINE_INT during field 1.	0
6	F2LIEN	R/W	0:disble LINE_INT during filed 2. 1:enable LINE_INT during field 2.	0
5-0	LINENUMBER	R/W	LINE_INT raw status register is “1” while video line number is more than this value. Line number is referred from standard video line number.	1A

0xAF – VBIREGLOAD

Bit	Function	R/W	Description	Reset
7	INTTYPE	R/W	0:INTREQ pin is level interrupt signal. 1:INTREQ pin is edge interrupt signal.	0
6	INTPOL	R/W	0:INTREQ pin is negative active. 1:INTREQ pin is positive active.	0
5-0	VBIREGLOADLINE	R/W	All Host accessed Sliced VBI registers are released and updated at the start of this video line number. Line number is referred from standard video line number.	1A

0xB0 – INT1MASK

Bit	Function	R/W	Description	Reset
7-0	INT1MASK	R/W	Bit-n masks interrupt signal generated by INT1STATUS register Bit-n	00

0xB1 – INT2MASK

Bit	Function	R/W	Description	Reset
7-0	INT2MASK	R/W	Bit-n masks interrupt signal generated by INT2STATUS register Bit-n	00

0xB2 – INT3MASK

Bit	Function	R/W	Description	Reset
7-0	INT3MASK	R/W	Bit-n masks interrupt signal generated by INT3STATUS register Bit-n	00

0xB3 – INT1CLEAR

Bit	Function	R/W	Description	Reset
7-0	INT1CLEAR	R/W	If value “1” is written into this register Bit-n,INT1STATUS register Bit-n is reset to “0”.This register bit value will be “0” after value “1” is written automatically.	00

0xB4 – INT2CLEAR

Bit	Function	R/W	Description	Reset
7-0	INT2CLEAR	R/W	If value “1” is written into this register Bit-n,INT2STATUS register Bit-n is reset to “0”.This register bit value will be “0” after value “1” is written automatically.	00

0xB5 – INT3CLEAR

Bit	Function	R/W	Description	Reset
7-0	INT3CLEAR	R/W	If value “1” is written into this register Bit-n,INT3STATUS register Bit-n is reset to “0”.This register bit value will be “0” after value “1” is written automatically.	00

0xB6 – INT1RAWSTATUS

Bit	Function	R/W	Description	Reset
7	HVLOCKSTCHANGED	R	1:H/V lock status changed. 0:H/V lock status not changed.	0
6	MACROSTCHANGED	R	1:Macrovision status changed. 0:Macrovision status not changed.	0
5	EDSSTDET	R	1:EDS packet detected and available for new value. 0:not available.	0
4	VCHIP_CHANGED_DET	R	1:VCHIP register changed and available for new value. 0:VCHIP register not changed and not available for new value.	0
3	GEM1XF2_DET	R	1:GEMSTAR1X data on field 2 available 0:not available	0
2	GEM1XF1_DET	R	1:GEMSTAR1X data on field 1 available 0:not available	0
1	GEM2XF2_DET	R	1:GEMSTAR2X data on field 2 available. 0:not available	0
0	GEM2XF1_DET	R	1:GEMSTAR2X data on field 1 available. 0:not available	0

0xB7 – INT2RAWSTATUS

Bit	Function	R/W	Description	Reset
7	STANDARDCHANGED	R	1:Video standard changed. 0:Video standard not changed.	0
6	LINE_INT	R	1:Current Video line number is more than the number of LINENUMBER register. 0: Current Video line number is smaller than the number of LINENUMBER register.	0
5	FIFOFULL	R	1:Sliced VBI RAM has overflow and full. 0:not overflow	0
4	FIFOTHRS	R	1:Sliced VBI RAM has the words more than the number of FTHRESHOLD register. 0:not	0
3	NO_VITC_CRC_ERROR	R	1:VITC data do not have CRC error. 0:VITC data has CRC error.	0
2	VITC_DET	R	1:VITC data available 0:VITC data not available	0
1	VPS_CHANGED	R	1:Line16 VPS data changed 0:Line16 VPS data not changed.	0
0	VPS_DET	R	1:Line16 VPS data available 0:Line16 VPS data not available	0

0xB8 – INT3RAWSTATUS

Bit	Function	R/W	Description	Reset
7	WST_DET	R	1:Teletext data available 0:Teletext data not available	0
6	NO_WSS 525_CRC _ERROR	R	1:WSS data do not have 525CRC error.. 0:WSS data have 525CRC error.	0
5	WSS_CH ANGED	R	1:WSS data changed. 0:WSS data not changed.	0
4	WSS_DET	R	1:WSS data available. 0:WSS data not available.	0
3	NO_CCF2 _NULL	R	1:Field 2 CC data do not have NULL bytes {0x80,0x80}. 0:Field 2 CC data have NULL bytes{0x80,0x80}.	0
2	CCF2_DE T	R	1:Field 2 CC data available. 0:Field 2 CC data not available.	0
1	NO_CCF1 _NULL	R	1: Field1 CC data do not have NULL bytes {0x80,0x80}. 0:Field1 CC data have NULL bytes{0x80,0x80}	0
0	CCF1_DE T	R	1:Field 1 CC data available. 0:Field 1 CC data not available.	0

0xB9 – INT1STATUS

Bit	Function	R/W	Description	Reset
7-0	INT1STAT US	R	If STATUS1MODE register Bit-n is “0”, This Bit-n is set to “1” when INT1RAWSTATUS register Bit-n changes “1” from “0” and reset to “0” when value “1” is written into IN1CLEAR register Bit-n. If STATUS1MODE register Bit-n is “1”, This Bit-n is equal to INT1RAWSTATUS register Bit-n.	00

0xBA – INT2STATUS

Bit	Function	R/W	Description	Reset
7-0	INT2STATUS	R	If STATUS2MODE register Bit-n is “0”, This Bit-n is set to “1” when INT2RAWSTATUS register Bit-n changes “1” from “0” and reset to “0” when value “1” is written into IN2CLEAR register Bit-n. If STATUS2MODE register Bit-n is “1”, This Bit-n is equal to INT2RAWSTATUS register Bit-n.	00

0xBB – INT3STATUS

Bit	Function	R/W	Description	Reset
7-0	INT3STATUS	R	If STATUS3MODE register Bit-n is “0”, This Bit-n is set to “1” when INT3RAWSTATUS register Bit-n changes “1” from “0” and reset to “0” when value “1” is written into IN3CLEAR register Bit-n. If STATUS3MODE register Bit-n is “1”, This Bit-n is equal to INT3RAWSTATUS register Bit-n.	00

0xBC – SVBIWCOUNT

Bit	Function	R/W	Description	Reset
7-0	SVBIWCOUNT	R	This value shows the number of words stored into sliced VBI RAM. 1 word is 2 bytes sliced VBI data in ANC packet	00

0xBD – CCF1DATA1

Bit	Function	R/W	Description	Reset
7-0	CCF1DATA1	R	Field 1 CC data 1st byte	80

0xBE – CCF1DATA2

Bit	Function	R/W	Description	Reset
7-0	CCF1DATA2	R	Field 1 CC data 2nd byte	80

0xBF – CCF2DATA1

Bit	Function	R/W	Description	Reset
7-0	CCF2DATA1	R	Field 2 CC data 1st byte	80

0xC0 – CCF2DATA2

Bit	Function	R/W	Description	Reset
7-0	CCF2DATA2	R	Field 2 CC data 2nd byte	80

0xC1 – VITCFRAME1

Bit	Function	R/W	Description	Reset
7-0	VITCFRAME1	R	VITC Bit9-2,1st Frame data	00

0xC2 – VITCFRAME2

Bit	Function	R/W	Description	Reset
7-0	VITCFRAME2	R	VITC Bit19-12,2nd Frame data	00

0xC3 – VITCSEC1

Bit	Function	R/W	Description	Reset
7-0	VITCSEC 1	R	VITC Bit29-22,1st Second data	00

0xC4 – VITCSEC2

Bit	Function	R/W	Description	Reset
7-0	VITCSEC 2	R	VITC Bit39-32,2nd Second data	00

0xC5 – VITCMIN1

Bit	Function	R/W	Description	Reset
7-0	VITCMIN1	R	VITC Bit49-42,1st Minute data	00

0xC6 – VITCMIN2

Bit	Function	R/W	Description	Reset
7-0	VITCMIN2	R	VITC Bit59-52,2nd Minute data	00

0xC7 – VITCHOUR1

Bit	Function	R/W	Description	Reset
7-0	VITCHOU R1	R	VITC Bit69-62,1st Hour data	00

0xC8 – VITCHOUR2

Bit	Function	R/W	Description	Reset
7-0	VITCHOU R2	R	VITC Bit79-72,2nd Hour data	00

0xC9 – VITCCRC

Bit	Function	R/W	Description	Reset
7-0	VITCCRC	R	If VITCCRCOEN register is “0”,this register has only two data type. 0x00 means “no CRC error” and 0x01 means “CRC error”. If VITCCRCOEN register is “1”,this register has 8bit VITC CRC data.	00

Following 0xCA-0xDB registers are under 625-line system detection.

0xCA – WSS_LO

Bit	Function	R/W	Description	Reset
7-5	WSS_LO2	R	These are bit7 to bit5 of WSS625 data. It should read “000”	000
4	WSS_LO1	R	These are bit4 of WSS625 data. 0:camera mode, 1:film mode.	0
3-0	WSS_LO0	R	These are bit3 to bit0 of WSS625 data.bit3 is odd parity bit. 1000:full format 4:3 0001: box 14:9 centre 0010:box 14:9 top 1011:box 16:9 centre 0100:box 16:9 top 1101:box > 16:9 centre 1111:full format 14:9 centre shoot and protect 14:9 0111:full format 16:9 anamorphic	00

0xCB – WSS_HI

Bit	Function	R/W	Description	Reset
7	WSS_DET	R	1:WSS625 is detected and available. 0:WSS625 is not available.	0
6	WSS_FLD	R	0:WSS625 data on field1, 1:WSS625 data on field 2.	0
5-3	WSS_HI2	R	These are bit13 to bit11 of WSS625 data. It should read “000”	000
2-1	WSS_HI1	R	These are bit10 to bit9 of WSS625 data. 00:no open subtitles 01:subtitles in active image area 10:subtitles out of active image area. 11:reserved.	00
0	WSS_HI0	R	These are bit8 of WSS625 data. 0:no subtitles within teletext 1:subtitles within teletext.	0

0xCC – VPSDATA1

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 1	R	These are bit7 to bit0 of 1st VPS data except Clock run-in and start code.	00

0xCD – VPSDATA2

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 2	R	These are bit7 to bit0 of 2nd VPS data except Clock run-in and start code.	00

0xCE – VPSDATA3

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 3	R	These are bit7 to bit0 of 3rd VPS data except Clock run-in and start code.	00

0xCF – VPSDATA4

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 4	R	These are bit7 to bit0 of 4th VPS data except Clock run-in and start code.	00

0xD0 – VPSDATA5

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 5	R	These are bit7 to bit0 of 5th VPS data except Clock run-in and start code.	00

0xD1 – VPSDATA6

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 6	R	These are bit7 to bit0 of 6th VPS data except Clock run-in and start code.	00

0xD2 – VPSDATA7

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 7	R	These are bit7 to bit0 of 7th VPS data except Clock run-in and start code.	00

0xD3 – VPSDATA8

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 8	R	These are bit7 to bit0 of 8th VPS data except Clock run-in and start code.	00

0xD4 – VPSDATA9

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 9	R	These are bit7 to bit0 of 9th VPS data except Clock run-in and start code.	00

0xD5 – VPSDATA10

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 10	R	These are bit7 to bit0 of 10th VPS data except Clock run-in and start code.	00

0xD6 – VPSDATA11

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 11	R	These are bit7 to bit0 of 11th VPS data except Clock run-in and start code.	00

0xD7 – VPSDATA12

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 12	R	These are bit7 to bit0 of 12th VPS data except Clock run-in and start code.	00

0xD8 – VPSDATA13

Bit	Function	R/W	Description	Reset
7-0	VPSDATA 13	R	These are bit7 to bit0 of 13th VPS data except Clock run-in and start code.	00

0xD9 – VPSSCODE1

Bit	Function	R/W	Description	Reset
7-0	VPSSCODE1	R	These are 1st byte of VPS Start code. Value is 0x51 normally.	00

0xDA – VPSSCODE2

Bit	Function	R/W	Description	Reset
7-0	VPSSCODE2	R	These are 2nd byte of VPS Start code. Value is 0x99 normally.	00

0xDB – TFCODE

Bit	Function	R/W	Description	Reset
7-0	TFCODE	R	These are Teletext framing code, 0x27:Teletext-B, 0xA7:Teletext-D, 0xE7:Teletext-A and Teletext-C	00

Following 0xCA-0xDB Registers are under 525 line system detection.

0xCA – WSS_LO

Bit	Function	R/W	Description	Reset
7	WSS525_CRC_ERROR	R	1: WSS525(CGMS) data has CRC error. 0: WSS525(CGMS) data do not have CRC error.	0
6	WSS_FLD	R	0: WSS525(CGMS) data on field1,1:WSS525(CGMS) data on field 2.	0
5-2	WSS_LO1	R	These are bit5 to bit2 of WSS525(CGMS) data 0000:copy control information 1111:default	0
1-0	WSS_LO0	R	These are bit1 to bit0 of WSS525(CGMS) data 00:4:3 aspect ratio normal 01:16:9 aspect ratio anamorphic 10:4:3 aspect ratio letterbox 11:reserved	00

0xCB – WSS_HI

Bit	Function	R/W	Description	Reset
7-5	WSS_HI3	R	These are bit13 to bit11 of WSS525(CGMS) data. It should read "000"	000
4	WSS_HI2	R	This is bit10 of WSS525(CGMS) data. 0:not analog pre-recorded medium. 1:analog pre-recorded medium	0
3-2	WSS_HI1	R	These are bit9 to bit8 of WSS525(CGMS) data. 00:PSP off 01:PSPon,2-line split burst on 10:PSPon,split burst off 11:PSP on,4-line split burst on	00
1-0	WSS_HI0	R	These are bit7 to bit6 of WSS525(CGMS) data. 00:copying permitted. 01:one copy permitted. 10:reserved. 11:no copying permitted.	00

0xCC – GEM2XF1FRAME_LO

Bit	Function	R/W	Description	Reset
7-0	GEM2XF1FRAME_LO	R	These are bit7 to bit0 of GEMSTAR2X data on field1.	00

0xCD – GEM2XF1FRAME_HI

Bit	Function	R/W	Description	Reset
7-3	Reserved	R		00
2-0	GEM2XF1FRAME_HI	R	These are bit10 to bit8 of GEMSTAR2X data on field1.	0

0xCE – GEM2XF1DATA1

Bit	Function	R/W	Description	Reset
7-0	GEM2XF1 DATA1	R	These are 1st byte of GEMSTAR2X data on field1.	00

0xCF – GEM2XF1DATA2

Bit	Function	R/W	Description	Reset
7-0	GEM2XF1 DATA2	R	These are 2nd byte of GEMSTAR2X data on field1.	00

0xD0 – GEM2XF1DATA3

Bit	Function	R/W	Description	Reset
7-0	GEM2XF1 DATA3	R	These are 3rd byte of GEMSTAR2X data on field1.	00

0xD1 – GEM2XF1DATA4

Bit	Function	R/W	Description	Reset
7-0	GEM2XF1 DATA4	R	These are 4th byte of GEMSTAR2X data on field1.	00

0xD2 – GEM1XF1DATA1

Bit	Function	R/W	Description	Reset
7-0	GEM1XF1 DATA1	R	These are 1st byte of GEMSTAR1X data on field1.	00

0xD3 – GEM1XF1DATA2

Bit	Function	R/W	Description	Reset
7-0	GEM1XF1 DATA2	R	These are 2nd byte of GEMSTAR1X data on field1.	00

0xD4 – GEM2XF2FRAME_LO

Bit	Function	R/W	Description	Reset
7-0	GEM2XF2 FRAME_L O	R	These are bit7 to bit0 of GEMSTAR2X data on field2.	00

0xD5 – GEM2XF2FRAME_HI

Bit	Function	R/W	Description	Reset
7-3	Reserved	R		00
2-0	GEM2XF2 FRAME_H I	R	These are bit10 to bit8 of GEMSTAR2X data on field2.	0

0xD6 – GEM2XF2DATA1

Bit	Function	R/W	Description	Reset
7-0	GEM2XF2 DATA1	R	These are 1st byte of GEMSTAR2X data on field 2.	00

0xD7 – GEM2XF2DATA2

Bit	Function	R/W	Description	Reset
7-0	GEM2XF2 DATA2	R	These are 2nd byte of GEMSTAR2X data on field 2	00

0xD8 – GEM2XF2DATA3

Bit	Function	R/W	Description	Reset
7-0	GEM2XF2 DATA3	R	These are 3rd byte of GEMSTAR2X data on field2.	00

0xD9 – GEM2XF2DATA4

Bit	Function	R/W	Description	Reset
7-0	GEM2XF2 DATA4	R	These are 4th byte of GEMSTAR2X data on field2.	00

0xDA – GEM1XF2DATA1

Bit	Function	R/W	Description	Reset
7-0	GEM1XF2 DATA1	R	These are 1st byte of GEMSTAR1X data on field 2.	00

0xDB – GEM1XF2DATA2

Bit	Function	R/W	Description	Reset
7-0	GEM1XF2 DATA2	R	These are 2nd byte of GEMSTAR1X data on field2.	00

0xDC – VCHIPRA

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-4	VCHIP_R	R	These are V-chip r2-r0 bits. 000=NA, 001=G,010=PG, 011=PG-13, 100=R, 101=NC-17, 110=X, 111=not rated.	000
3-0	VCHIP_A	R	These are V-chip a3-a0 bits. L=V-chip a3, D=V-chip a2. xxx0: MPAA movie rating. LD01: USA TV rating. 0011: Canadian English TV rating. 0111: Canadian French TV rating. 1011,1111:reserved.	F

0xDD – VCHIPG

Bit	Function	R/W	Description	Reset
7-6	Reserved	R		00
5	VCHIP_V	R	This bit is V-chip V. 1:violence is present, 0:not	0
4	VCHIP_S	R	This bit is V-chip S. 1:sexual situations are present. 0:not	0
3	Reserved	R		0
2-0	VCHIP_G	R	These are V-chip g2-g0 000=not rated. 001=TV-Y, 010=TV-Y7, 011=TV-G, 100=TV-PG, 101=TV-14, 110=TV-MA, 111=not rated.	000

0xDE – TFCODE

Bit	Function	R/W	Description	Reset
7-0	TFCODE	R	These are Teletext framing code, 0x27:Teletext-B, 0xA7:Teletext-D, 0xE7:Teletext-A and Teletext-C. These are useful under 525-line system detection. These are equal to 0xDB TFCODE register under 625-line system detection.	00

0xDF – SVBIRDATA

Bit	Function	R/W	Description	Reset
7-0	SVBIRDATA	R	These are current sliced VBI RAM data byte	00

0xE0 – EDSSTATUS

Bit	Function	R/W	Description	Reset
7	TIMEOFDAY	R	1:EDS packet "Time of Day" available in edsdata1-10 registers 0:not available	0
6	UNDEFINED	R	1:EDS packet Class "undefined" available in edsdata1-10 registers. 0:not available	0
5	RESERVED	R	1:EDS packet Class "reserved" available in edsdata1-10 registers. 0:not available	0
4	PUBLICSERVICE	R	1:EDS packet Class "public service: available in edsdata1-10 registers. 0:not available	0
3	MISCELLANEOUS	R	1:EDS packet Class "miscellaneous" available in edsdata1-10 registers. 0:not available When TIMEOFDAY bit is "1", this bit is "0".	0
2	CHANNEL	R	1:EDS packet Class "channel" available in edsdata1-10 registers. 0:not available	0
1	FUTURE	R	1:EDS packet Class "future" available in edsdata1-10 registers. 0:not available	0
0	CURRENT	R	1:EDS packet Class "current" available in edsdata1-10 registers. 0:not available	0

0xE1 – EDSDATA1

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA1	R	These are control code characters in EDS data packets when EDS data packet is detected.	00

0xE2 – EDSDATA2

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 2	R	These are type characters in EDS data packets when EDS data packet is detected.	00

0xE3 – EDSDATA3

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 3	R	These are 1st byte data after type character when EDS data packet is detected.	00

0xE4 – EDSDATA4

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 4	R	These are 2nd byte data after type character when EDS data packet is detected.	00

0xE5 – EDSDATA5

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 5	R	These are 3rd byte data after type character when EDS data packet is detected.	00

0xE6 – EDSDATA6

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 6	R	These are 4th byte data after type character when EDS data packet is detected.	00

0xE7 – EDSDATA7

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 7	R	These are 5th byte data after type character when EDS data packet is detected.	00

0xE8 – EDSDATA8

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 8	R	These are 6th byte data after type character when EDS data packet is detected.	00

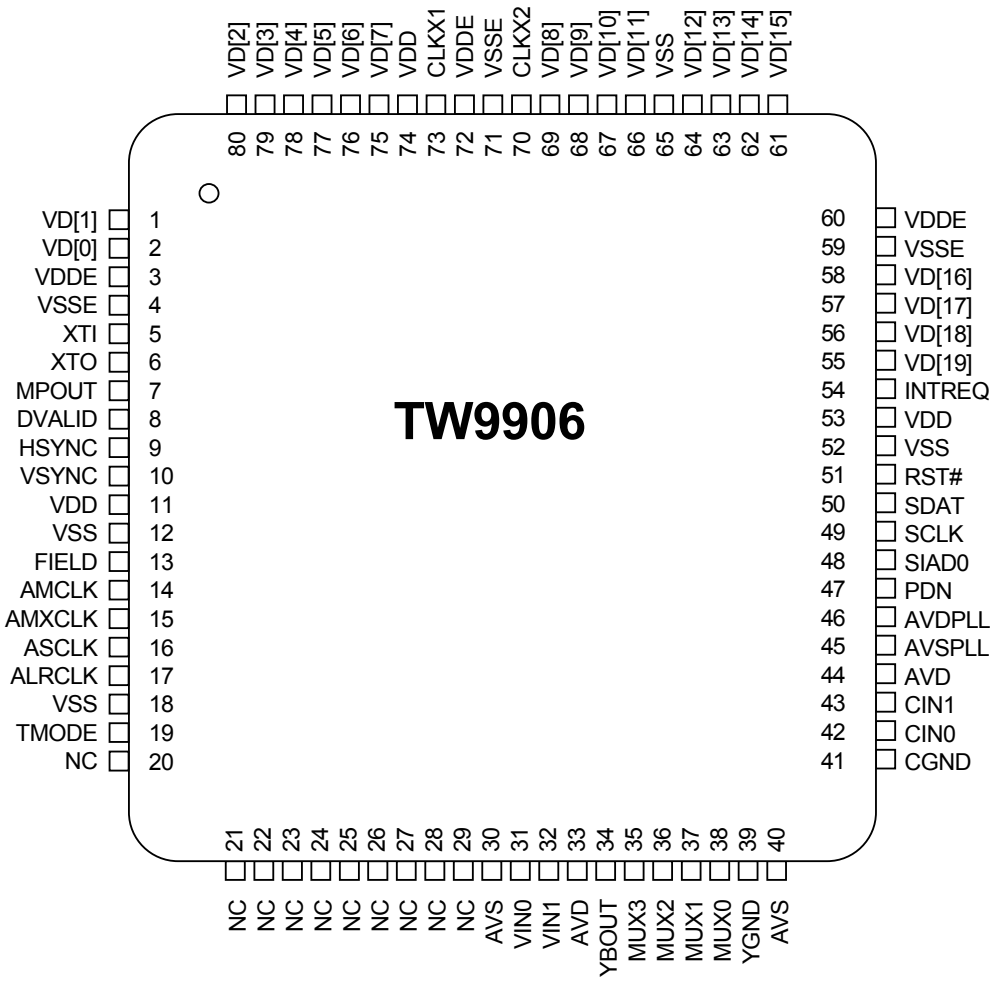
0xE9 – EDSDATA9

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 9	R	These are 7th byte data after type character when EDS data packet is detected.	00

0xEA – EDSDATA10

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-0	EDSDATA 10	R	These are 8th byte data after type character when EDS data packet is detected.	00

Pin Diagram


TW9906
1 VD[1]
2 VD[0]
3 VDDE
4 VSSE
5 XTI
6 XTO
7 MPOUT
8 DVALID
9 HSYNC
10 VSYNC
11 VDD
12 VSS
13 FIELD
14 AMCLK
15 AMXCLK
16 ASCLK
17 ALRCLK
18 VSS
19 TMODE
20 NC
21 NC
22 NC
23 NC
24 NC
25 NC
26 NC
27 NC
28 NC
29 NC
30 AVS
31 VIN0
32 VIN1
33 AVD
34 YBOUT
35 MUX3
36 MUX2
37 MUX1
38 MUX0
39 YGND
40 AVS
41 CGND
42 CIN0
43 CIN1
44 AVD
45 AVSPLL
46 AVDPLL
47 PDN
48 SIAD0
49 SCLK
50 SDAT
51 RST#
52 VSS
53 VDD
54 INTREQ
55 VD[19]
56 VD[18]
57 VD[17]
58 VD[16]
59 VSSE
60 VDDE
61 VD[15]
62 VD[14]
63 VD[13]
64 VD[12]
65 VSS
66 VD[11]
67 VD[10]
68 VD[9]
69 VD[8]
70 CLKX2
71 VSSE
72 VDDE
73 CLKX1
74 VDD
75 VD[7]
76 VD[6]
77 VD[5]
78 VD[4]
79 VD[3]
80 VD[2]

Pin Description

This section provides a detailed description of each pin for the TW9906. The pins are arranged in functional groups according to their associated interface.

The active state of the signal is determined by the trailing symbol at the end of the signal name. A "#" symbol indicates that the signal is active or asserted at a low voltage level. When "#" is not present after the signal name, the signal is active at the high voltage level.

Analog Interface Pins

Pin#	I/O	Pin Name	Description
35, 36, 37,38	I	MUX3, MUX2, MUX1, MUX0	Analog CVBS or Y input.
39		YGND	Signal ground for Y-ADC.
42	I	CIN0	Analog chroma input. Connect unused input to AGND through 0.1uF capacitor.
43	I	CIN1	Analog chroma input. Connect unused input to AGND through 0.1uF capacitor.
41		CGND	Signal ground for C-ADC.
31	I	VIN0	The analog V input to the V-ADC in component video input mode.
32	I	VIN1/MUX4	This is software selectable input pin for either analog V input to the V-ADC in component video input mode or analog composite video input MUX4 to Y-ADC.
34	O	YBOUT	Buffered analog output. Leave it open when no used.

Two Wire Interface Pins

Pin#	I/O	Pin Name	Description
49	I	SCLK	The MPU Serial interface Clock Line.
50	I/O	SDAT	The MPU Serial interface Data Line.
48	I	SIAD0	The MPU interface address select pin 0. This pin is used to select one of the two addresses that chip will respond. It is internally pulled down to ground.
51	I	RST#	Master Reset Input. A logical zero for a minimum of four consecutive clock cycles is required to reset the device to its default state.

Video Timing Unit Pins

Pin#	I/O	Pin Name	Description
9	O	HSYNC	Horizontal Sync or multi-purpose Output pin. See Register 0x05 for control information.
10	O	VSYNC	Vertical Sync or multi-purpose Output pin. See Register 0x05 for control information.

Pin#	I/O	Pin Name	Description
13	O	FIELD	Odd/Even Field or multi-purpose Output pin. See Register 0x1B for control information.
55,56,57, 58,61,62, 63,64,66, 67	I/O	VD[19:10]	Digitized Video Data Outputs. VD[0] is the least significant bit of the bus in 20-bit mode. VD[10] is the least significant bit of the bus in 10-bit mode. In 8-bit mode, VD[19] is the MSB and VD[12] is the LSB.
68,69,75, 76,77,78, 79,80,1,2	I/O	VD[9:0]	
8	**O**	DVALID	Data Valid flag Output. This pin indicates when a valid pixel is being output onto the data bus.
47	**I**	PDN	Power down control pin. It is high active.
7	**O**	MPOUT	Multi-purpose output pin. The output function can be selected by RTSEL of register 0x19. See Register 0x19 for control information.
19	**I**	TMODE	This pin is used to enable the in-circuit test mode. It should be connected to VSS through a 10K ohm pull-down resistor for in-circuit test or tied to VSS directly for others.
54	**O**	INTREQ	Interrupt request output.
Audio Clock Signals			
15	**I**	AMXCLK	Audio clock input. It should be connected to AMCLK in normal operation.
14	**O**	AMCLK	Field locked audio clock output.
16	**O**	ASCLK	Audio bit serial clock.
17	**O**	ALRCLK	Audio frame clock.

Clock Interface Pins

Pin#	I/O	Pin Name	Description
5	**I**	XTI	Clock Zero pins. A 27MHz fundamental (or third harmonic) crystal can be connected directly to these pins, or a single-ended oscillator can be connected to XTI.
6	**O**	XTO	For Crystal 27MHz connection.
73	**O**	CLKX1	Multi-function clock output pin. The output function can be selected by CK1S of register 0x1B.
70	**O**	CLKX2	Multi-function clock output pin. The output function can be selected by CK2S of register 0x1B.

Power and Ground Pins

Pin#	I/O	Pin Name	Description
11,53,74	P	VDD	+2.5 V Power supply for digital circuitry. A 0.1 μF ceramic capacitor should be connected between each group of VDD pins and the ground plane as close to the device as possible.
12,18,52 ,65	G	VSS	Core power return.
3,60,72	P	VDDE	+3.3 V Power supply for IO Pad. A 0.1 μF ceramic capacitor should be connected between each group of VDD pins and the ground plane as close to the device as possible.
4,59,71	G	VSSE	I/O power return.
33,44	P	AVD	+2.5 V Power supply for analog circuitry. A 0.1 μF ceramic capacitor should be connected between each group of AVDD pins and the ground plane as close to the device as possible.
30,40	G	AVS	Analog 2.5V Power return.
46	P	AVDPLL	Analog +3.3V Power supply.
45	G	AVSPLL	Analog 3.3V Power return.

Parametric Information

AC/DC Electrical Parameters

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVDD (measured to AVSS)	V_{DDAM}	-	-	3.0	V
V_{DD} (measured to DVSS)	V_{DDM}		-	4.0	V
Voltage on any signal pin (See the note below)	-	DVSS – 0.5	-	V_{DDM} + 0.5	V
Analog Input Voltage	-	AVSS – 0.5	-	V_{DDAM} + 0.5	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Vapor Phase Soldering(15 Seconds)	T_{VSOL}	-	-	+220	°C

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latchup.

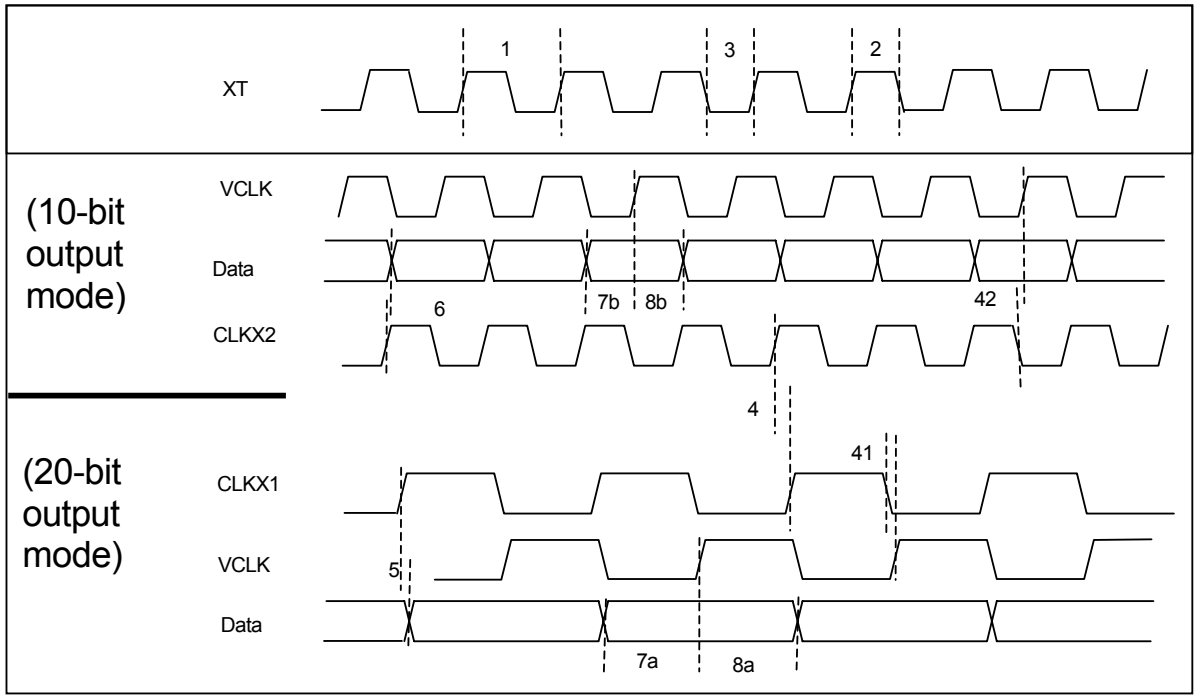
Table 8. characteristics

	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO PAD	V_{DDE}	3.15	3.3	3.6	V
Power Supply — Analog PLL	V_{DDP}	3.15	3.3	3.45	V
Power Supply — Analog ADC	V_{DDA}	2.4	2.5	2.8	V
Power Supply — Digital Core	V_{DD}	2.3	2.5	2.6	V
Maximum $\|V_{DD} - AVDD\|$		-	-	0.3	V
MUX0, MUX1, MUX2, MUX3 and MUX4 Input Range (AC coupling required)		0.5	1.00	2.00	V
CIN Amplitude Range (AC coupling required)		0.5	1.00	2.00	V
VIN Amplitude Range (AC coupling required)		0.5	1.00	2.00	V
Ambient Operating Temperature	T_A	0		+70	°C
Analog Supply current	Iaa	-	20	50	mA
Digital IO Supply current	Idd	-	20	-	mA
Digital Core Supply current		-	55	-	mA
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	V_{DDM} + 0.5	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DDM} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	VSS -0.5	-	1.0	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	μA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	μA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF

Parameter	Symbol	Min	Typ	Max	Units
Digital Outputs					
Output High Voltage (I_{OH} = –4 mA)	V_{OH}	2.4	-	V_{DDE}	V
Output Low Voltage (I_{OL} = 4 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	10	-	bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	24	27	30	MHz
Video bandwidth (-3db)	BW	-	10	-	MHz
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
deviation		-	-	±50	ppm
Temperature range	Ta	0	-	70	°C
load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
Oscillator Input					
nominal frequency		-	27	-	MHz
deviation		-	-	±25	ppm
duty cycle		-	-	55	%

Parameter	Symbol	Min	Typ	Max	Units
XT input					
Cycle Time	1	-	18	-	ns
High Time	2	-	9	-	ns
Low Time	3	-	9	-	ns
Output CLK					
CLKX1		12	13.5	15	MHz
CLKX2		24	27	30	MHz
CLKX1 Duty Cycle		-	-	55	%
CLKX2 Duty Cycle		-	-	55	%
CLKX2 to CLKX1 Delay	4	-	-	2	ns
CLKX1 to Data Delay	5	-	-	2	ns
CLKX2 to Data Delay	6	-	-	2	ns
CLKX1 (Falling Edge) to VCLK (Rising Edge)	41	-	0	-	ns
CLKX2 (Falling Edge) to VCLK (Rising Edge)	42	-	0	-	ns
Output Video Data					
10-bit Mode (1)					
Data to VCLK (Rising Edge) Delay	7b	-	18	-	ns
VCLK (Rising Edge) to Data Delay	8b	-	18	-	ns
20-bit Mode (1)					
Data to VCLK (Rising Edge) Delay	7a	-	37	-	ns
VCLK (Rising Edge) to Data Delay	8a	-	37	-	ns

Clock Timing Diagram



Application Information

Video Input Interface

The TW9906 has a built-in 5:1 input MUX for software controllable input selections. This MUX can be used to select three composite video sources and one S-Video source or two composite video sources, one S-video and one component video source. The chroma of the S-Video input should be connected to CIN0 or CIN1 of the C-Channel A/D converter. In the case of component video, the Y input should be connected to one of the Y channel input. The Pb input should be connected to one of the C channel input. The Pr input should be connected to one of the V channel input. For a typical application, a video input should be first terminated with a 75 ohm resistor before it is AC coupled by a 0.1uF capacitor to the input of the MUX.

A/D Converter

The TW9906 has three internal A/D converters to cover all possible analog video signal sources. The reference supply generator for the A/D converter is also on-chip.

Clamping/AGC

The TW9906 has built-in automatic clamping control circuitry. No extra external component is needed for this operation. The clamping loop gain can be controlled through register setting. The TW9906 also has built-in automatic AGC control circuitry. The AGC loop gain can also be controlled by register. The AGC loop response time is also register programmable.

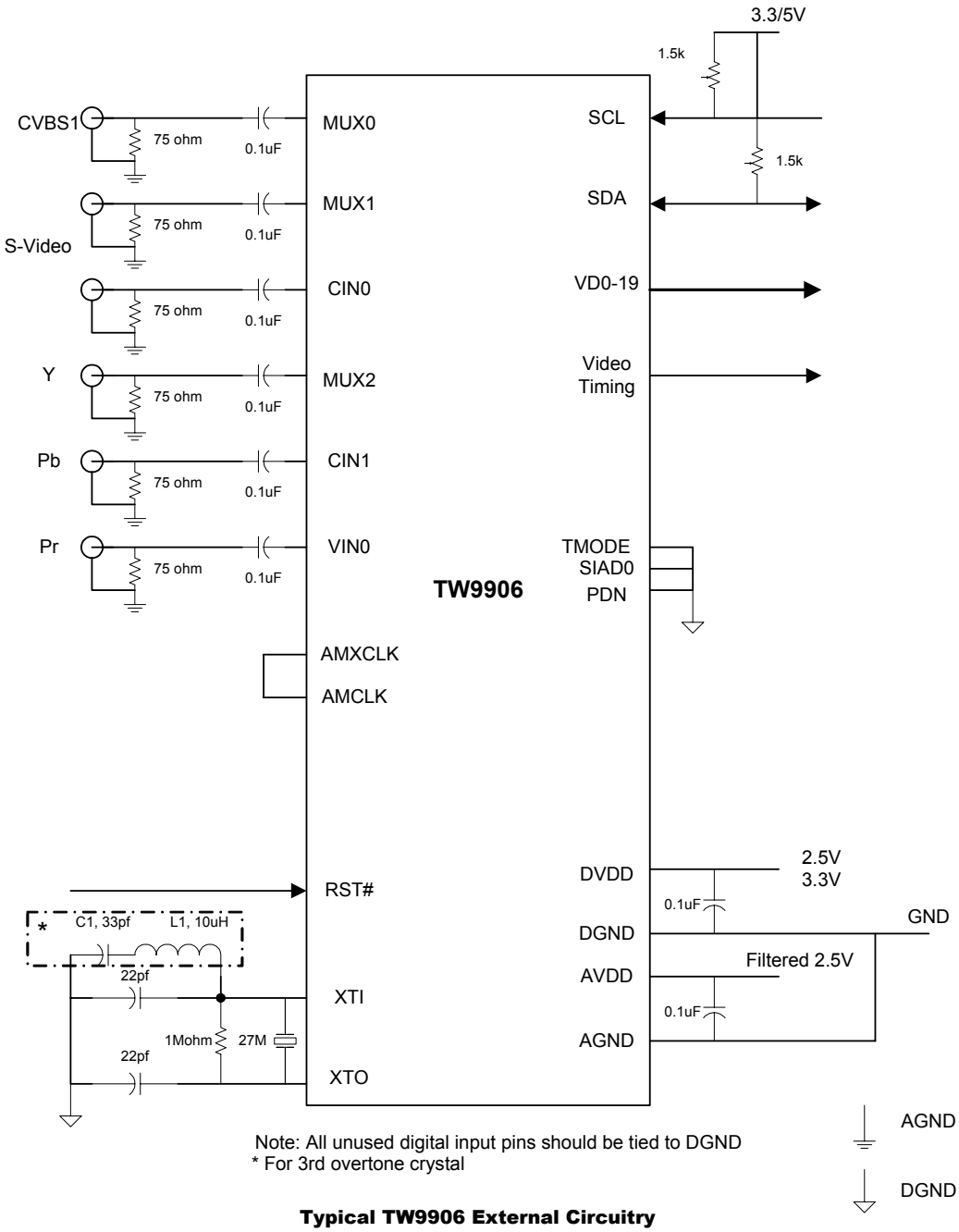
Clock Generation

The TW9906 requires one 27MHz crystal connected to XTI and XTO for all format decoding. The default crystal type should be 27MHz, fundamental mode, 20pF load capacitance or less, +-50ppm, and with series resistance of 80 ohm or less. An external clock source of 27MHz can also be connected to the XTI input in place of the crystal. For True Square Pixel mode applications, a 24.54MHz crystal for 60Hz field rate source and a 29.5MHz crystal for 50Hz field rate source should be used. In this case, the bit FC27 of registers 0x02 should be set to '0' for proper operation. A typical 27MHz third overtone crystal circuit is shown in the following figure. In the case of using 27MHz fundamental mode crystal, the C1 and L1 can be omitted.

Power-Up

After power-up, the TW9906 registers have unknown values. The RST# pin must be asserted and released to bring all registers to its default values. After reset, the TW9906 data outputs are tri-stated. The OPFORM register should be written after reset to enable outputs desired.

Application Schematics



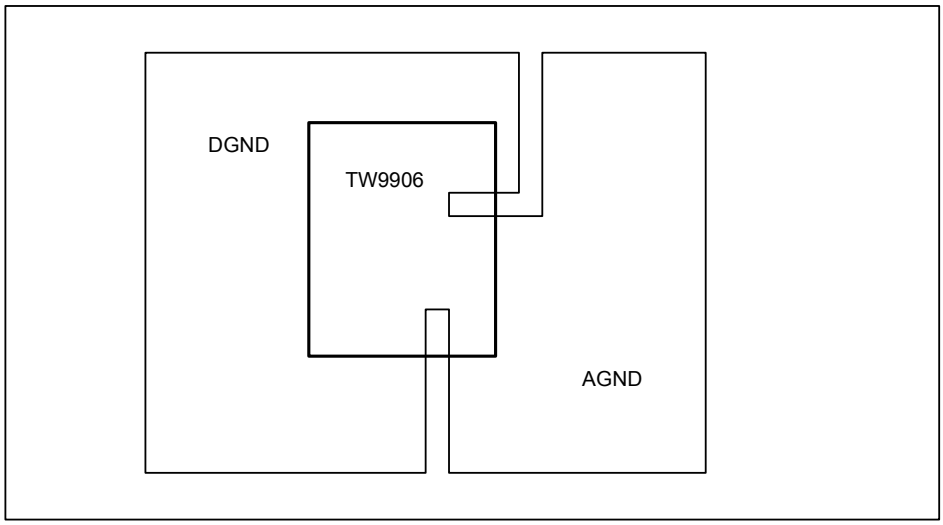
Note: All unused digital input pins should be tied to DGND
* For 3rd overtone crystal

Typical TW9906 External Circuitry

PCB Layout Considerations

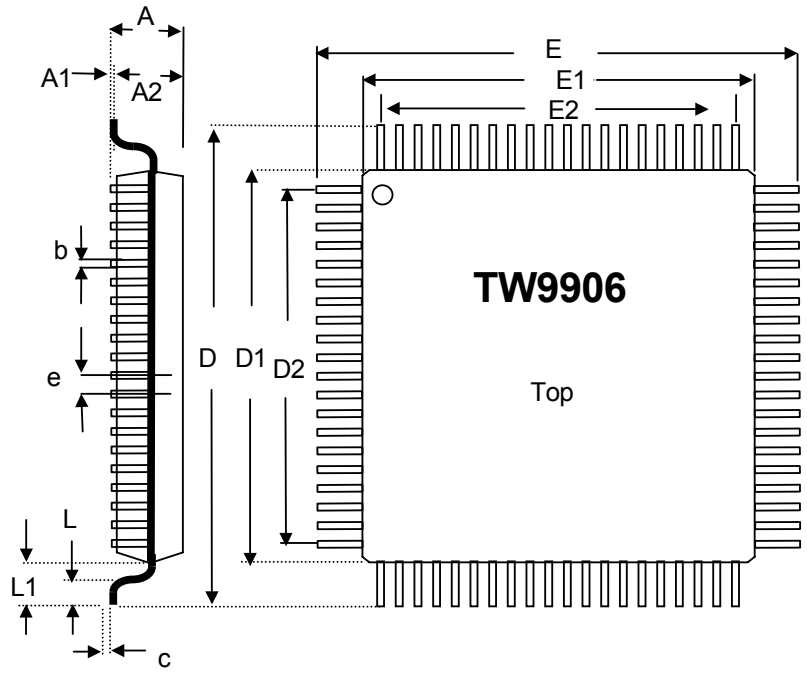
The PCB layout should be done to minimize the power and ground noise on the TW9906. This is done by good power de-coupling with minimum lead length on the de-coupling capacitors; well-filtered and regulated analog power input shielding and ground plane isolation.

The ground plane should cover most of the PCB area with separated digital and analog ground planes surrounding the chip. These two planes should be at the same electrical potential and connected together under TW9906. The following figure shows a ground plane layout example.



To minimize crosstalk, the digital signals of TW9906 should be separated from the analog circuitry. Moreover, the digital signals should not cross over the analog power and ground plane. Parallel running of digital lines for long distance should also be avoided.

80-pin TQFP Package Mechanical Drawing



	Millimeter			Inch		
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	---	---	1.60	---	---	0.063
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.27	0.005	0.006	0.009
c	0.09	---	0.20	0.004	---	0.008
e	0.5 Basic			0.020 Basic		
D	14.0 Basic			0.551 Basic		
D1	12.00 Basic			0.472 Basic		
D2	9.50			0.374		
E	14.0 Basic			0.551Basic		
E1	12.00 Basic			0.472 Basic		
E2	9.50			0.374		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 Ref			0.039Ref		

Note: 1. Dimension of D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed. The maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the lead root. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm Pitch Packages.

Copyright Notice

Disclaimer

This document provides technical information for the user. Techwell, Inc. reserves the right to modify the information in this document as necessary. The customer should make sure that they have the most recent data sheet version. Techwell, Inc. holds no responsibility for any errors that may appear in this document. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Techwell, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Life Support Policy

Techwell, Inc. products are not authorized for use as critical components in life support devices or systems.

Datasheet revision history

Date	
12/06/2004	First draft.
2/16/2005	A few bugs are fixed. Supply currents are added.
3/21/2005	XT input parameters are added. CLKx1,2 to data delay fixed.
8/01/2005	Chip revision B
10/7/2005	Pg22. fig9,10 data output fixed to 10bit(VD[19:10], VD[9:0]). Pg110. AVDD symbol : V_{DDAM}, VDD symbol : V_{DDM} Pg111. Output High Voltage max : V_{DDE}
11/01/2005	Pg51. Vsync/Hsync output polarity fixed. ‘0’ active low. ‘1’active high.