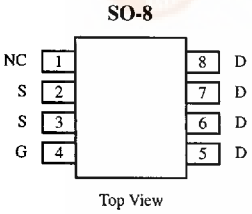
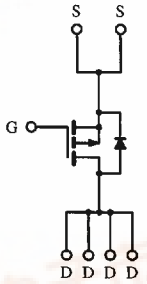
P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–20	0.10 @ V_{GS} = –10 V	±4.3
	0.16 @ V_{GS} = –4.5 V	±3.4

Recommended upgrade: Si9430DY
Lower profile/smaller size—see LITE FOOT® equivalent: Si6447DQ





P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–20	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±4.3	A
	T_A = 70°C		±3.3	
Pulsed Drain Current		I_{DM}	±20	
Continuous Source Current (Diode Conduction)[a]		I_S	–2.2	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1202. A SPICE Model data sheet is available for this product (FaxBack document #5102).

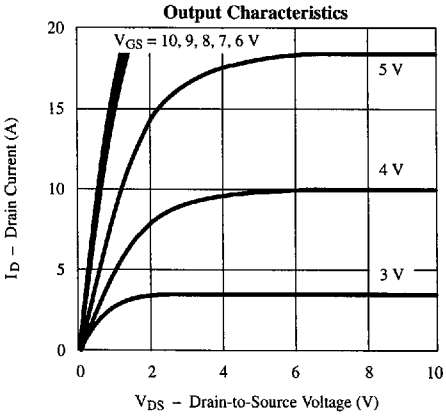
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 µA	–0.5			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –16 V, V_{GS} = 0 V			–2	µA
		V_{DS} = –16 V, V_{GS} = 0 V, T_J = 55°C			–25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≤ –5 V, V_{GS} = –10 V	–20			A
		V_{DS} ≤ –5 V, V_{GS} = –4.5 V	–5			
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = 2.0 A		0.07	0.10	Ω
		V_{GS} = –4.5 V, I_D = 2.0 A		0.11	0.16	
Forward Transconductance[b]	g_{fs}	V_{DS} = –15 V, I_D = –4.3 A		6		S
Diode Forward Voltage[b]	V_{SD}	I_S = –1.25 A, V_{GS} = 0 V		–0.8	–1.6	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = –10 V, V_{GS} = –10 V, I_D = –2.0 A		29	40	nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			14		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –10 V, R_L = 10 Ω I_D ≅ –1 A, V_{GEN} = –10 V, R_G = 6 Ω		15	30	ns
Rise Time	t_r			30	80	
Turn-Off Delay Time	$t_{d(off)}$			142	200	
Fall Time	t_f			130	200	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, di/dt = 100 A/µs		70		

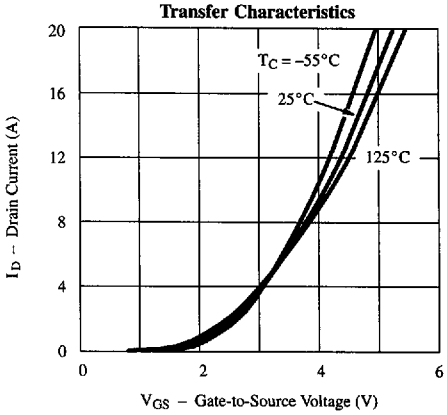
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted)

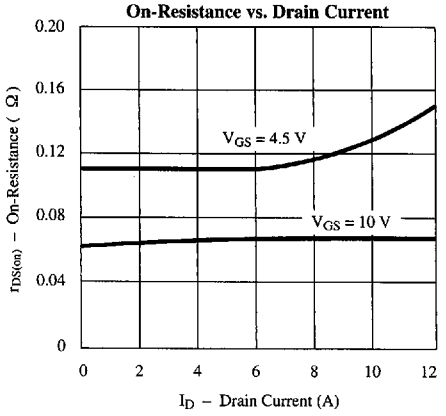
Output Characteristics



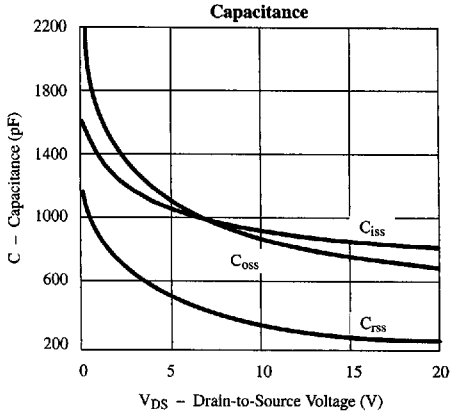
Transfer Characteristics



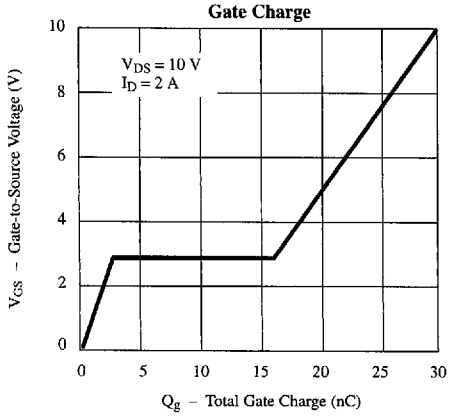
On-Resistance vs. Drain Current



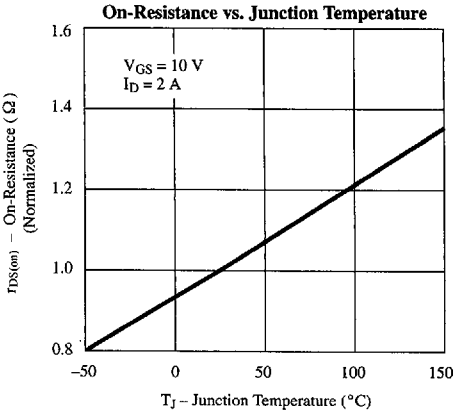
Capacitance



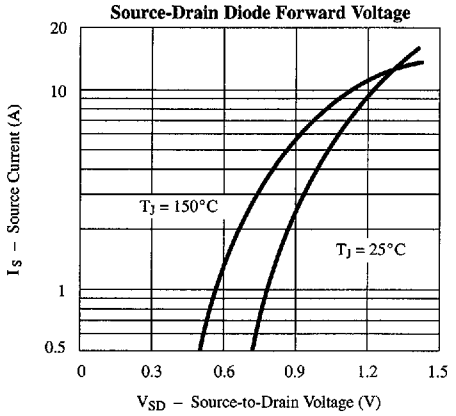
Gate Charge

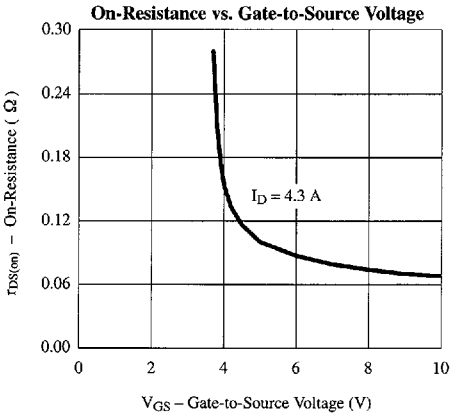


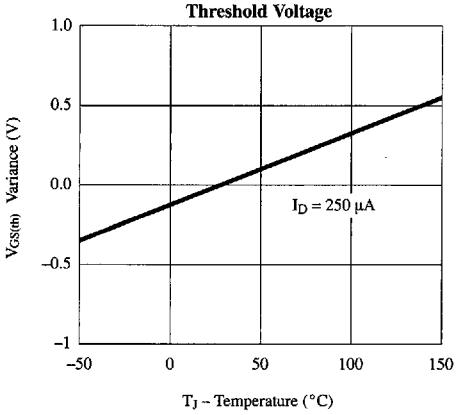
On-Resistance vs. Junction Temperature

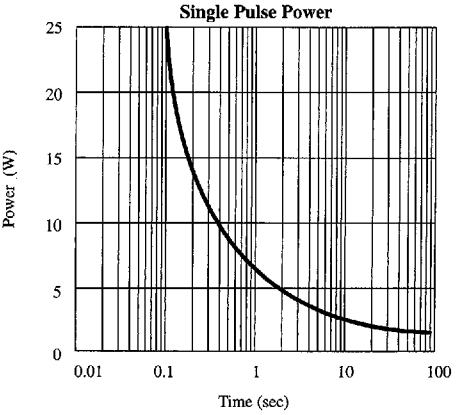


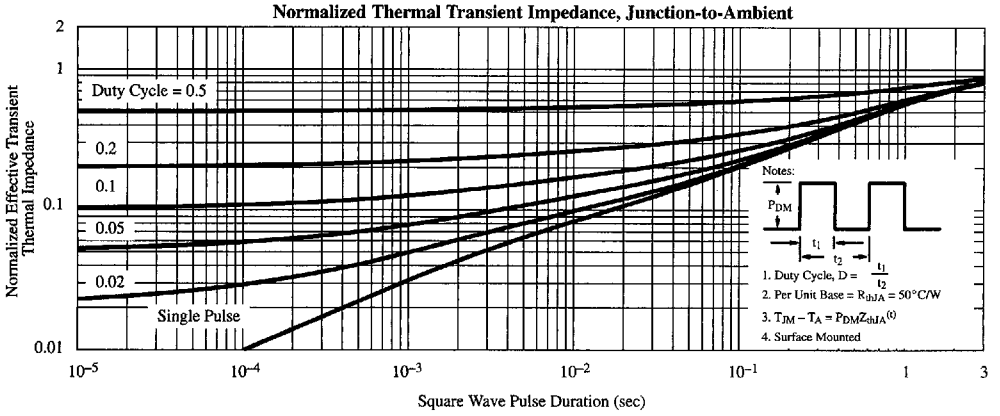
Typical Characteristics (25°C Unless Otherwise Noted)



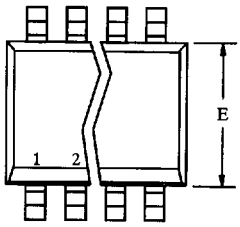


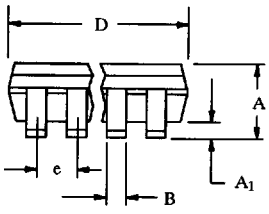


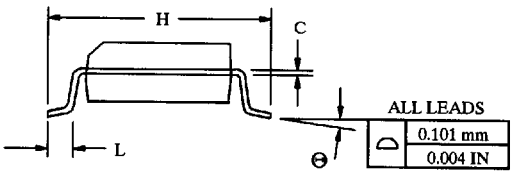




SO Package (Y Suffix), 8–16 Leads







Dim	Millimeters		Inch
	Min	Max	Min
A	1.35	1.75	0.053
A_1	0.10	0.20	0.004
B	0.35	0.45	0.014
C	0.18	0.23	0.007
D-8	4.60	5.20	0.181
D-14	8.35	8.95	0.329
D-16	9.60	10.20	0.378
E	3.55	4.05	0.140
e	1.27 BSC		0.050 B
H	5.70	6.30	0.224
L	0.60	0.80	0.024
Θ	0°	8°	0°