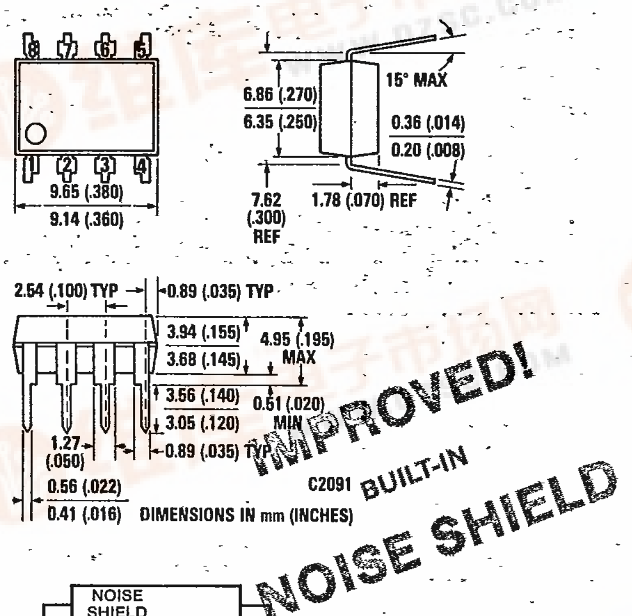
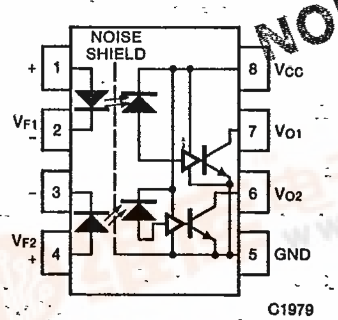
GENERAL INSTRUMENT

DUAL VERY HIGH-SPEED LOGIC GATE OPTOCOUPLERS

DUAL 10 MBit/s LOGIC GATE MCL2630 (HCPL-2630) MCL2631 (HCPL-2631)

PACKAGE DIMENSIONS





A 0.1μF bypass capacitor must be connected between pins 8 and 5. (See note 1)

Equivalent Circuit

DESCRIPTION

The MCL/HCPL-2630 and MCL/HCPL-2631 dual channel optocouplers have two channels, each consisting of a 700 nm GaAsP LED, optically coupled to a very high speed integrated photodetector logic gate. The outputs feature open collectors, thereby permitting wired-OR outputs. The coupled parameters are guaranteed over the temperature range of 0-70°C. A maximum input signal of 5 mA will provide a minumum output sink current of 13 mA (fan-out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/μs. The MCL/HCPL 2631 has a minimum CMR of 1 kV/μs.

An improved double-molded package allows superior insulation, permitting a 480 V working voltage compared to industry standard 220 V.

FEATURES

- Very high speed — 10 MBit/s
- Superior CMR — 10 kV/μs
- Superior insulation — 2500 V RMS 1 min.
- Double working voltage — 480 V
- Fan-out of 8 over 0-70°C
- Logic gate output
- Wired-OR — open collector
- U.L. recognized (File #E50151)

APPLICATIONS

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

ABSOLUTE MAXIMUM RATINGS

Storage temperature .... -55°C to +125°C
Operating temperature .... 0°C to +70°C
Lead solder temperature.......... 260°C for 10 s
DC/Average forward input current (each channel).......................... 15 mA
Peak forward input current (each channel)...... 30 mA (≤ 1 msec duration)

Reverse input voltage (each channel)........ 5.0 V
Reverse supply voltage (-Vcc) .... -500 mV
Supply voltage, (Vcc) ... 7.0 V/1 minute maximum
Output current, (Io) (each channel) .... 16 mA
Output voltage, (Vo) (each channel).......... 7.0 V
Collector output power dissipation .... 60 mW

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN.	MAX.	UNITS
Input current, low level	I_{FL}	0	250	μA
Input current, high level	I_{FH}	6.3*	15	mA
Supply voltage, output	V_{CC}	4.5	5.5	V
Operating temperature	T_A	0	70	°C
Fan out (TTL Load)	N		8	

6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C Unless Otherwise Specified)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
High level output current	I_{OH}		2	250	μA	V_{CC} = 5.5 V, V_O = 5.5 V I_F = 250 μA, Note 6
Low level output voltage	V_{OL}		0.34	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA Note 6, I_{OL} = 13 mA
High level supply current	I_{CCH}		14	30	mA	V_{CC} = 5.5 V, I_F = 0 mA (Both channels)
Low level supply current	I_{CCL}		26	36	mA	V_{CC} = 5.5 V, I_F = 10 mA (Both channels)
Input forward voltage	V_F		1.55	1.75	V	I_F = 10 mA, T_A = 25°C
Input reverse breakdown voltage	B_{VR}	5.0			V	I_R = 10 μA, T_A = 25°C
Input capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz
Input diode temperature coefficient	$\Delta V_F/\Delta T_A$		-1.4		mV/°C	I_F = 10 mA
Input-input insulation leakage current	I_{I-I}		0.005		μA	Relative humidity = 45% t = 5 s, V_{I-I} = 500 V, Note 7
Resistance (input-input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V, Note 7
Capacitance (input-input)	C_{I-I}		0.25		pF	f = 1 MHz, Note 7
Input-output insulation leakage current	I_{I-O}			1.0	μA	Relative humidity = 45% T_A = 25°C, t = 5 s V_{I-O} = 3000 V dc Note 10
Resistance (input to output) Capacitance (input to output)	R_{I-O} C_{I-O}		10^{12} 0.6		Ω pF	V_{I-O} = 500 V, Note 10 f = 1 MHz, Note 10
Withstand insulation test voltage	V_{ISO}	2500			V_{RMS}	RH < 50% T_A = 25°C t = 1 min

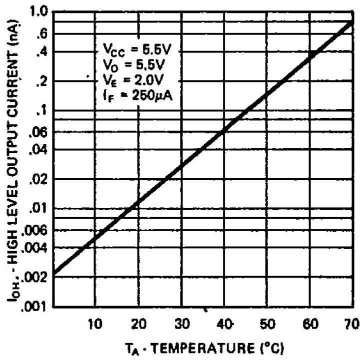
All typical values are at V_{CC} = 5 V, T_A 25°C (each channel).

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V Unless Otherwise Specified)

PARAMETER	SYMBOL	DEVICE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Propagation delay time (For output high level)	t_{PLH}			48	75	ns	
Propagation delay time (For output low level	t_{PHL}			48	75	ns	R_L = 350 Ω C_L = 15 pF
Output rise time (10-90%)	t_r			30		ns	I_F = 7.5 mA
Output fall time (90-10%)	t_f			14		ns	Notes, 2, 3, 4 & 5, Fig. 8
Common mode transient immunity (At output high level)	CM_H	2631 2630	1000	10,000 10,000		V/μs	V_{CM} = 50 V (peak) I_F = 0 mA, V_{OL} (min) = 2.0 V R_L = 350 Ω, Note 9, Fig. 12
Common mode transient immunity (At output low level)	CM_L	2631 2630	-1000	-10,000 -10,000		V/μs	V_{CM} = 50 V (peak) I_F = 7.5 mA, V_{OL} (max) = 0.8 V R_L = 350 Ω, Note 8, Fig. 12

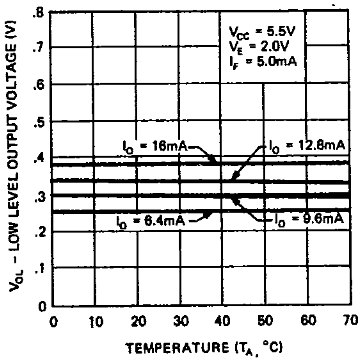
MCL2630 (HCPL-2630) MCL2631 (HCPL-2631)

TYPICAL CHARACTERISTIC CURVES (T_A = 25° C Unless Otherwise Specified)



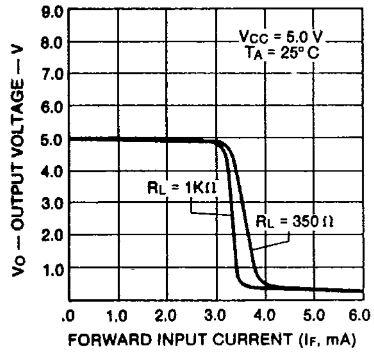
C1613

Fig. 2. High Level Output Current vs. Temperature



C1598

Fig. 3. Low Level Output Voltage vs. Temperature



C1602

Fig. 4. Output Voltage vs. Forward Input Current

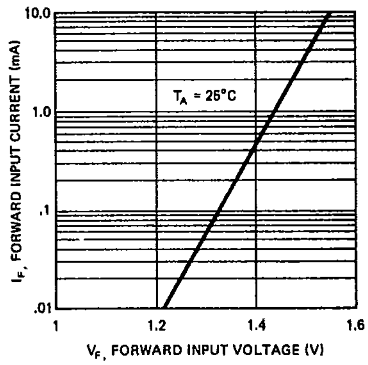


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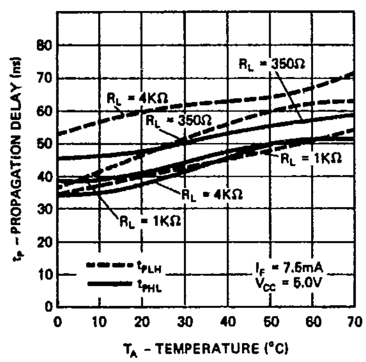
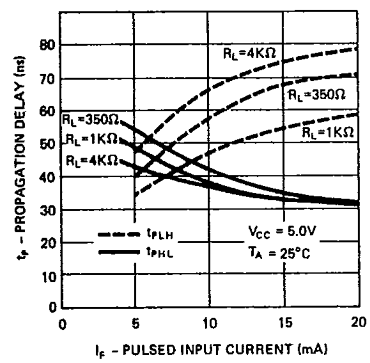
Fig. 5. Forward Input Current vs. Forward Input Voltage



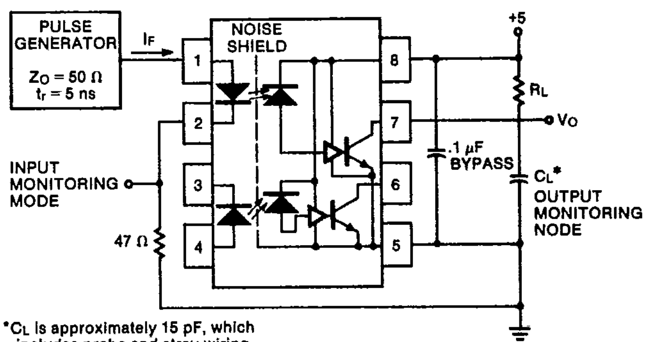
C1604

Fig. 6. Propagation Delay vs. Temperature



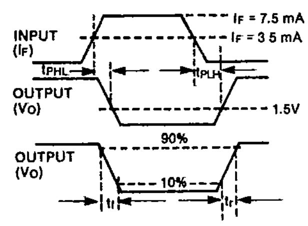
C1603

Fig. 7. Propagation Delay vs. Pulse Input Current



*CL is approximately 15 pF, which includes probe and stray wiring capacitance

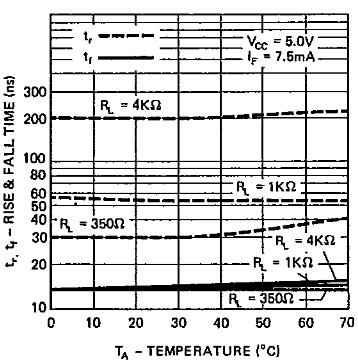
C1980



C1790

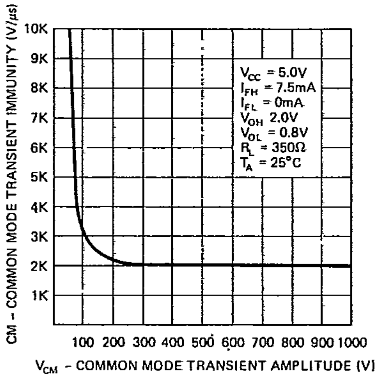
Fig. 8. Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f

TYPICAL CHARACTERISTIC CURVES (T_A = 25°C Unless Otherwise Specified)



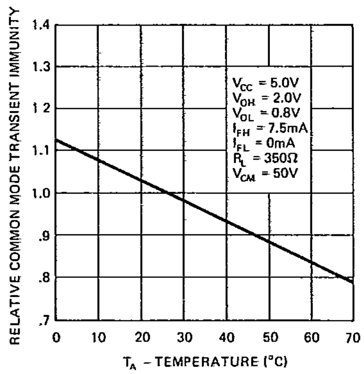
C1601

Fig. 9. Rise and Fall Time vs. Temperature



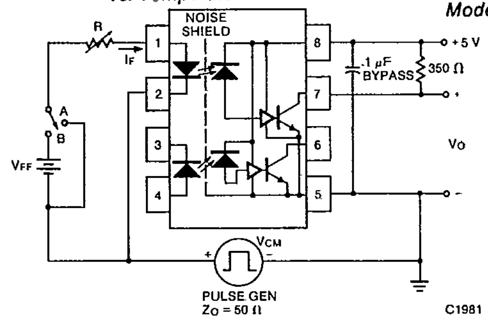
C1590

Fig. 10. Relative Common Mode Transient Immunity vs. Common Mode Transient Complitude

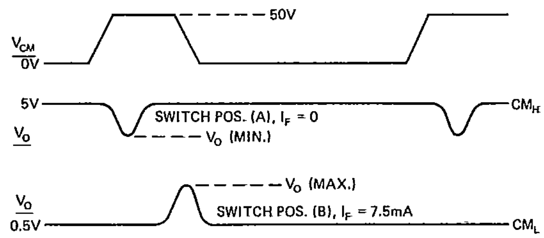


C1595

Fig. 11. Relative Common Mode Transient Immunity vs. Temperature



C1981



C1594

Fig. 12. Test Circuit for Transient Immunity and Typical Waveforms

NOTES:

1. *The V_{CC} supply voltage to each MCL2630 isolator must be bypassed by a 0.1 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.*
2. *t_{PHL} – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.*
3. *t_{PLH} – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the Low to High transition of the output voltage pulse.*
4. *t_f – Fall time is measured from the 10% to the 90% levels of the HIGH to LOW transition on the output pulse.*
5. *t_r – Rise time is measured from the 90% to the 10% levels of the LOW to HIGH transition on the output pulse.*
6. *Each channel.*
7. *Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.*
8. *CM_L – The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_{OUT} > 0.8 V). Measured in volts per microsecond (V/%s).*
9. *CM_H – The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., V_{OUT}> 2.0 V). Measured in volts per microsecond (V/μs).*

   Volts/microsecond can be translated to sinusoidial voltages:

   $$V/\mu s = \frac{(dV_{CM})}{dt} \text{ Max.} = \pi f_{CM} V_{CM} (p.p.)$$

   Example: $V_{CM} = 318\ V_{pp}$ when f_{CM} = 1 MHz using CM_L and CM_H = 1000 V/μs.

10. *–Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.*