

THC63LVDM83R/THC63LVDM63R

REDUCED SWING LVDS 24Bit/18Bit COLOR HOST-LCD PANEL INTERFACE

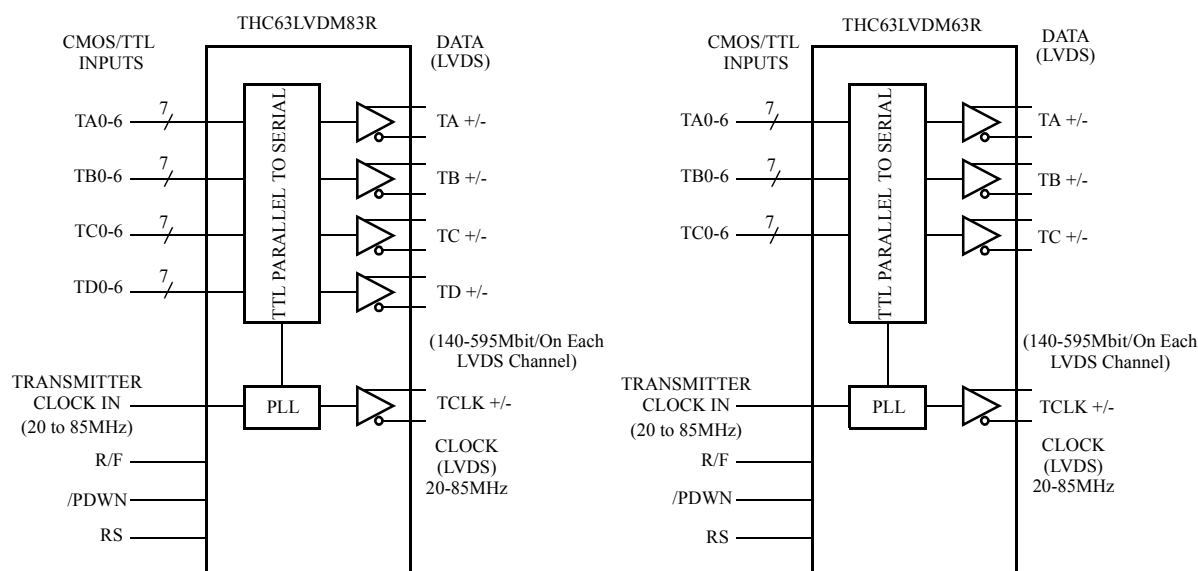
General Description

The THC63LVDM83R transmitter converts 28bits of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. At a transmit clock frequency of 85MHz, 28bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at a rate of 595Mbps per LVDS channel. Also available is THC63LVDM63R that converts 21bits of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. Both transmitters can be programmed reduced swing LVDS through a dedicated pin for low power consumption and EMI.

Features

- 28:4 Data channel compression at up to 298 Megabytes per sec throughput
- Wide dot clock range: 20-85MHz suited for VGA, SVGA, XGA and SXGA
- Narrow bus (10 lines or 8 lines) reduces cable size
- Support Reduced swing LVDS for Low EMI
- 200mV swing LVDS/350mV swing LVDS selectable
- Support Spread Spectrum Clock Generator
- On chip Input Jitter Filtering
- PLL requires No external components
- Single 3.3V supply with 125mW(TYP)
- Power-Down Mode
- Low profile 56 or 48 Lead TSSOP Package
- Clock Edge Programmable
- Improved Replacement for the National DS90C383 or DS90C363

Block Diagram



Pin Out

THC63LVDM83R		THC63LVDM63R	
RS	1	TA4	1
TD1	2	RS	2
TA5	3	TA5	3
TA6	4	TA6	4
GND	5	GND	5
TB0	6	TB0	6
TB1	7	TB1	7
TD2	8	VCC	8
VCC	9	TB2	9
TD3	10	TB3	10
TB2	11	GND	11
TB3	12	TB4	12
GND	13	TB5	13
TB4	14	R/F	14
TB5	15	TB6	15
TD4	16	TC0	16
R/F	17	GND	17
TD5	18	TC1	18
TB6	19	TC2	19
TC0	20	TC3	20
GND	21	VCC	21
TC1	22	TC4	22
TC2	23	TC5	23
TC3	24	GND	24
TD6	25		
VCC	26		
TC4	27		
TC5	28		
		56	TA4
		55	TA3
		54	TA2
		53	GND
		52	TA1
		51	TA0
		50	TD0
		49	LVDS GND
		48	TA-
		47	TA+
		46	TB-
		45	TB+
		44	LVDS VCC
		43	LVDS GND
		42	TC-
		41	TC+
		40	TCLK-
		39	TCLK+
		38	TD-
		37	TD+
		36	LVDS GND
		35	PLL GND
		34	PLL VCC
		33	PLL GND
		32	/PDWN
		31	CLK IN
		30	TC6
		29	GND
		48	TA3
		47	TA2
		46	GND
		45	TA1
		44	TA0
		43	N/C
		42	LVDS GND
		41	TA-
		40	TA+
		39	TB-
		38	TB+
		37	LVDS VCC
		36	LVDS GND
		35	TC-
		34	TC+
		33	TCLK-
		32	TCLK+
		31	LVDS GND
		30	PLL GND
		29	PLL VCC
		28	PLL GND
		27	/PDWN
		26	CLK IN
		25	TC6

THC63LVDM83R Pin Description

Pin Name	Pin #	Type	Description								
TA+, TA-	47, 48	LVDS OUT	LVDS Data Out.								
TB+, TB-	45, 46	LVDS OUT									
TC+, TC-	41, 42	LVDS OUT									
TD+, TD-	37, 38	LVDS OUT									
TCLK+, TCLK-	39, 40	LVDS OUT	LVDS Clock Out.								
TA0 ~ TA6	51, 52, 54, 55, 56, 3, 4	IN	Pixel Data Inputs.								
TB0 ~ TB6	6, 7, 11, 12, 14, 15, 19	IN									
TC0 ~ TC6	20, 22, 23, 24, 27, 28, 30	IN									
TD0 ~ TD6	50, 2, 8, 10, 16, 18, 25	IN									
/PDWN	32	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)								
RS	1	IN	LVDS swing control. <table border="1" data-bbox="965 779 1380 896"> <thead> <tr> <th>RS</th> <th>LVDS swing</th> </tr> </thead> <tbody> <tr> <td>VCC</td> <td>350mV</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>GND</td> <td>200mV</td> </tr> </tbody> </table>	RS	LVDS swing	VCC	350mV	:	:	GND	200mV
RS	LVDS swing										
VCC	350mV										
:	:										
GND	200mV										
R/F	17	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge								
VCC	9, 26	Power	Power Supply Pins for TTL inputs and digital circuitry.								
CLKIN	31	IN	Clock in.								
GND	5, 13, 21, 29, 53	Ground	Ground Pins for TTL inputs and digital circuitry.								
LVDS VCC	44	Power	Power Supply Pins for LVDS Outputs.								
LVDS GND	36, 43, 49	Ground	Ground Pins for LVDS Outputs.								
PLL VCC	34	Power	Power Supply Pin for PLL circuitry.								
PLL GND	33, 35	Ground	Ground Pins for PLL circuitry.								

THC63LVDM63R Pin Description

Pin Name	Pin #	Type	Description								
TA+, TA-	40, 41	LVDS OUT	LVDS Data Out.								
TB+, TB-	38, 39	LVDS OUT									
TC+, TC-	34, 35	LVDS OUT									
TCLK+, TCLK-	32, 33	LVDS OUT	LVDS Clock Out.								
TA0 ~ TA6	44, 45, 47, 48, 1, 3, 4	IN	Pixel Data Inputs.								
TB0 ~ TB6	6, 7, 9, 10, 12, 13, 15	IN									
TC0 ~ TC6	16, 18, 19, 20, 22, 23, 25	IN									
/PDWN	27	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)								
RS	2	IN	LVDS swing control. <table border="1" data-bbox="965 1870 1380 1986"> <thead> <tr> <th>RS</th> <th>LVDS swing</th> </tr> </thead> <tbody> <tr> <td>VCC</td> <td>350mV</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>GND</td> <td>200mV</td> </tr> </tbody> </table>	RS	LVDS swing	VCC	350mV	:	:	GND	200mV
RS	LVDS swing										
VCC	350mV										
:	:										
GND	200mV										

Pin Name	Pin #	Type	Description
R/F	14	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge
VCC	8, 21	Power	Power Supply Pins for TTL inputs and digital circuitry.
CLKIN	26	IN	Clock in.
GND	5, 11, 17, 24, 46	Ground	Ground Pins for TTL inputs and digital circuitry.
LVDS VCC	37	Power	Power Supply Pins for LVDS Outputs.
LVDS GND	36, 42	Ground	Ground Pins for LVDS Outputs.
PLL VCC	29	Power	Power Supply Pin for PLL circuitry.
PLL GND	28, 30	Ground	Ground Pins for PLL circuitry.

Absolute Maximum Ratings ¹

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ ($V_{CC} + 0.3V$)
CMOS/TTL Output Voltage	-0.3V ~ ($V_{CC} + 0.3V$)
LVDS Driver Output Voltage	-0.3V ~ ($V_{CC} + 0.3V$)
Output Current	continuous
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +150°C
Resistance to soldering heat	+260°C / 10sec
Maximum Power Dissipation @+25°C	0.5W

Electrical Characteristics

CMOS/TTL DC Specifications

 $V_{CC} = 3.0V \sim 3.6V, T_a = -10^\circ C \sim +70^\circ C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{CC}$			± 10	μA
I_{PD}	Pull Down Current	R/F pin, $V_{IH} = V_{CC}$			100	μA
I_{RS}	RS Pull Down Current	RS pin, $V_{IH} = V_{CC}$			100	μA

1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

LVDS Transmitter DC Specifications

 $V_{CC} = 3.0V \sim 3.6V, T_a = -10^{\circ}C \sim +70^{\circ}C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS=V _{CC}	250	350	450	mV
			Reduced swing RS=GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω			35	mV	
VOC	Common Mode Voltage		1.125	1.25	1.375	V	
ΔVOC	Change in VOC between complementary output states				35	mV	
I _{OS}	Output Short Circuit Current	V _{OUT} =0V, RL=100Ω			-24	mA	
I _{OZ}	Output TRI-STATE Current	/PDWN=0V, V _{OUT} =0V to V _{CC}			±10	μA	

THC63LVDM83R Supply Current

 $V_{CC} = 3.0V \sim 3.6V, T_a = -10^{\circ}C \sim +70^{\circ}C$

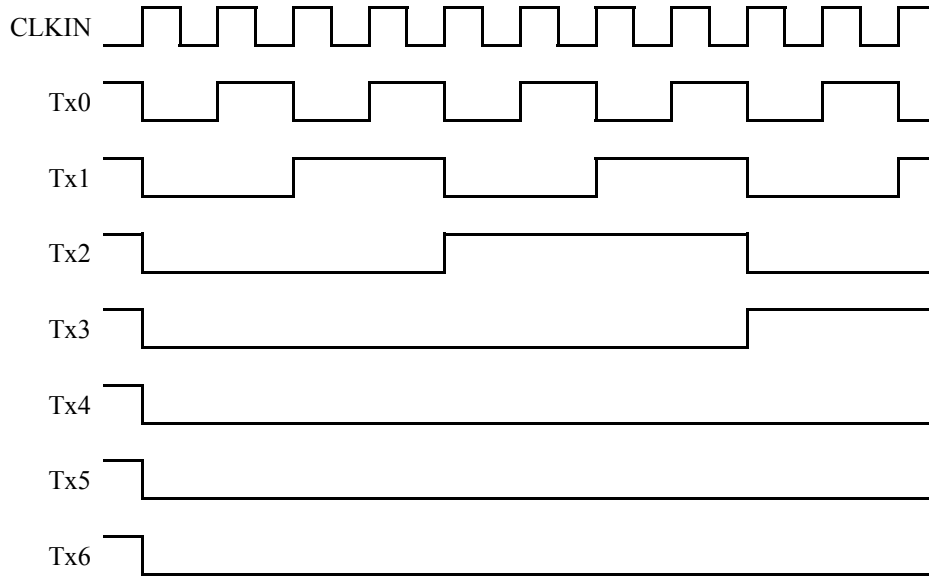
Symbol	Parameter	Condition(*)	Typ.	Max.	Units	
I _{TCCG}	Transmitter Supply Current	RL=100Ω, CL=5pF V _{CC} =3.3V, RS=V _{CC} 16 Gray Scale Pattern	f=65MHz	36	46	mA
			f=85MHz	39	49	mA
		RL=100Ω, CL=5pF V _{CC} =3.3V, RS=GND 16 Gray Scale Pattern	f=65MHz	31	41	mA
			f=85MHz	34	44	mA
I _{TCCW}	Transmitter Supply Current	RL=100Ω, CL=5pF V _{CC} =3.3V, RS=V _{CC} Worst Case Pattern	f=65MHz	38	48	mA
			f=85MHz	41	51	mA
		RL=100Ω, CL=5pF V _{CC} =3.3V, RS=GND Worst Case Pattern	f=65MHz	33	43	mA
			f=85MHz	36	46	mA
I _{TCCS}	Transmitter Power Down Supply Current	/PDWN = L		10	μA	

THC63LVDM63R Supply Current

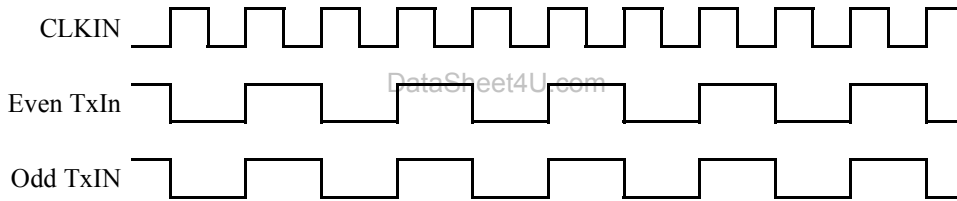
 $V_{CC} = 3.0V \sim 3.6V, T_a = -10^{\circ}C \sim +70^{\circ}C$

Symbol	Parameter	Condition(*)	Typ.	Max.	Units	
I_{TCCG}	Transmitter Supply Current	RL=100Ω, CL=5pF V _{CC} =3.3V, RS=V _{CC} 16 Gray Scale Pattern	f=65MHz	33	41	mA
			f=85MHz	37	45	mA
		RL=100Ω, CL=5pF V _{CC} =3.3V, RS=GND 16 Gray Scale Pattern	f=65MHz	29	36	mA
			f=85MHz	33	39	mA
I_{TCCW}	Transmitter Supply Current	RL=100Ω, CL=5pF V _{CC} =3.3V, RS=V _{CC} Worst Case Pattern	f=65MHz	35	43	mA
			f=85MHz	39	47	mA
		RL=100Ω, CL=5pF V _{CC} =3.3V, RS=GND Worst Case Pattern	f=65MHz	31	38	mA
			f=85MHz	35	42	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L		10	μA	

16 Gray Scale Pattern



Worst Case Pattern



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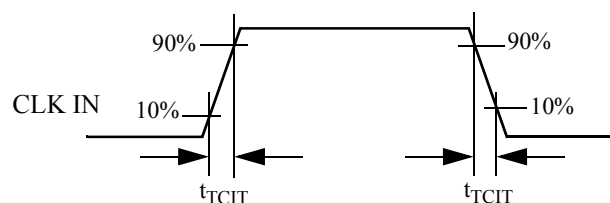
Switching Characteristics

 $V_{CC} = 3.0V \sim 3.6V, T_a = -10^{\circ}C \sim +70^{\circ}C$

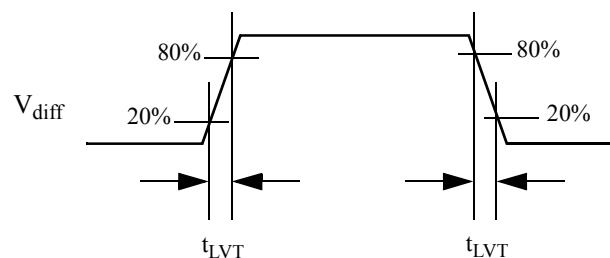
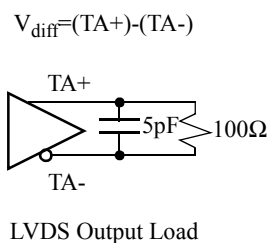
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{TCIT}	CLK IN Transition time			5.0	ns
t_{TCP}	CLK IN Period	11.76	T	50.0	ns
t_{TCH}	CLK IN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLK IN Low Time	0.35T	0.5T	0.65T	ns
t_{TCD}	CLK IN to TCLK+/- Delay		2T/7		ns
t_{TS}	TTL Data Setup to CLK IN	2.5			ns
t_{TH}	TTL Data Hold from CKL IN	2.5			ns
t_{LVT}	LVDS Transition Time		0.6	1.5	ns
t_{TOP1}	Output Data Position0 (T=11.76ns)	-0.2	0.0	+0.2	ns
t_{TOP0}	Output Data Position1 (T=11.76ns)	$\frac{T}{7} - 0.2$	$\frac{T}{7}$	$\frac{T}{7} + 0.2$	ns
t_{TOP6}	Output Data Position2 (T=11.76ns)	$2\frac{T}{7} - 0.2$	$2\frac{T}{7}$	$2\frac{T}{7} + 0.2$	ns
t_{TOP5}	Output Data Position3 (T=11.76ns)	$3\frac{T}{7} - 0.2$	$3\frac{T}{7}$	$3\frac{T}{7} + 0.2$	ns
t_{TOP4}	Output Data Position4 (T=11.76ns)	$4\frac{T}{7} - 0.2$	$4\frac{T}{7}$	$4\frac{T}{7} + 0.2$	ns
t_{TOP3}	Output Data Position5 (T=11.76ns)	$5\frac{T}{7} - 0.2$	$5\frac{T}{7}$	$5\frac{T}{7} + 0.2$	ns
t_{TOP2}	Output Data Position6 (T=11.76ns)	$6\frac{T}{7} - 0.2$	$6\frac{T}{7}$	$6\frac{T}{7} + 0.2$	ns
t_{TPLL}	Phase Lock Loop Set			10.0	ms

AC Timing Diagrams

TTL Input

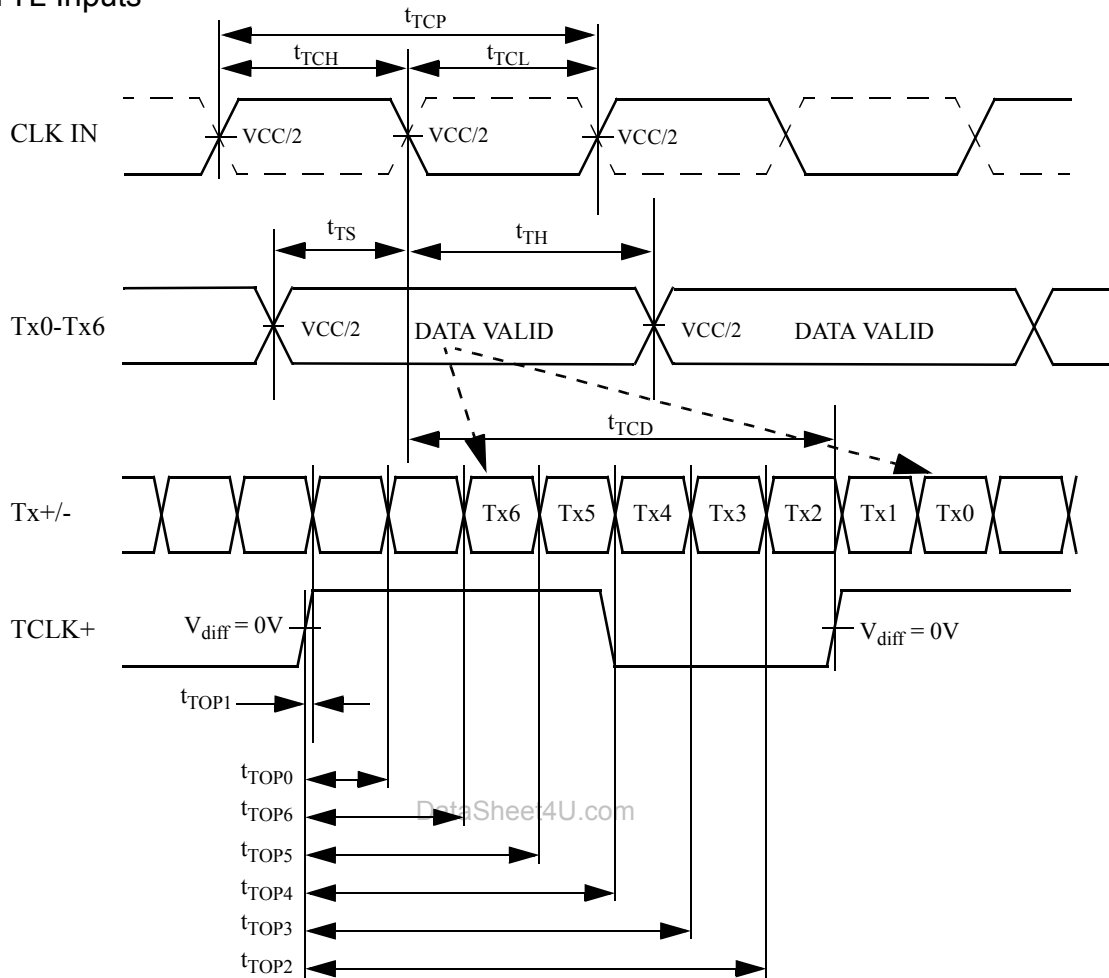


LVDS Output



AC Timing Diagrams

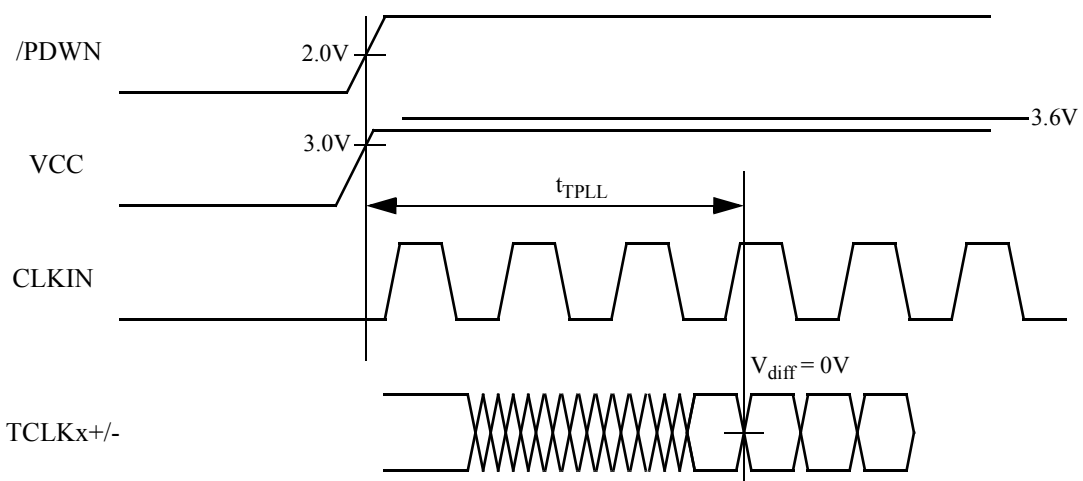
TTL Inputs



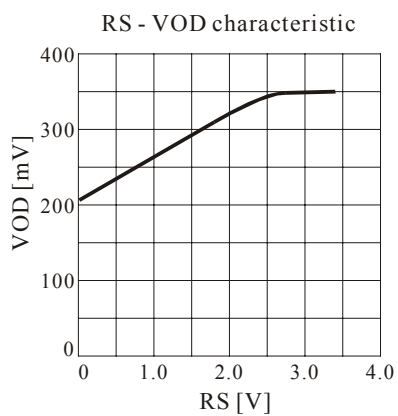
Note:

- 1) CLK IN: for THC63LVDM83R/THC63LVDM63R(R/F=GND), denote as solid line,
for THC63LVDM83R/THC63LVDM63R(R/F=VCC), denote as dashed line
- 2) $V_{diff} = (T_{yx+}) - (T_{yx-})$, ---- (TCLKx+) - (TCLKx-)

Phase Lock Loop Set Time



Reduced Swing Characteristic ($T_A=25^{\circ}\text{C}$, $V_{CC}=3.3\text{V}$, $R_L=100\Omega$)



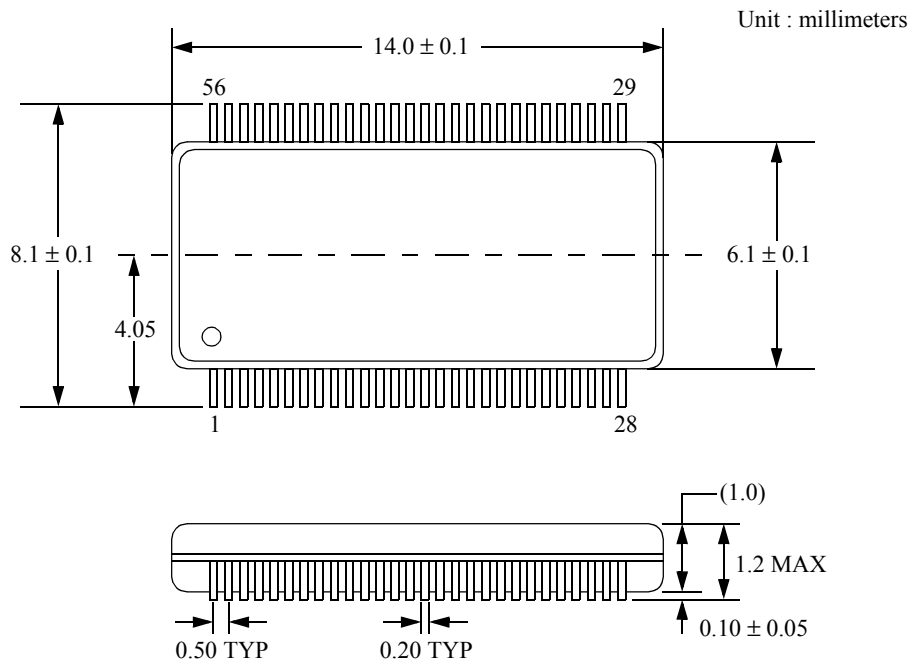
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Package

56 Lead Molded Thin Shrink Small Outline Package, JEDEC

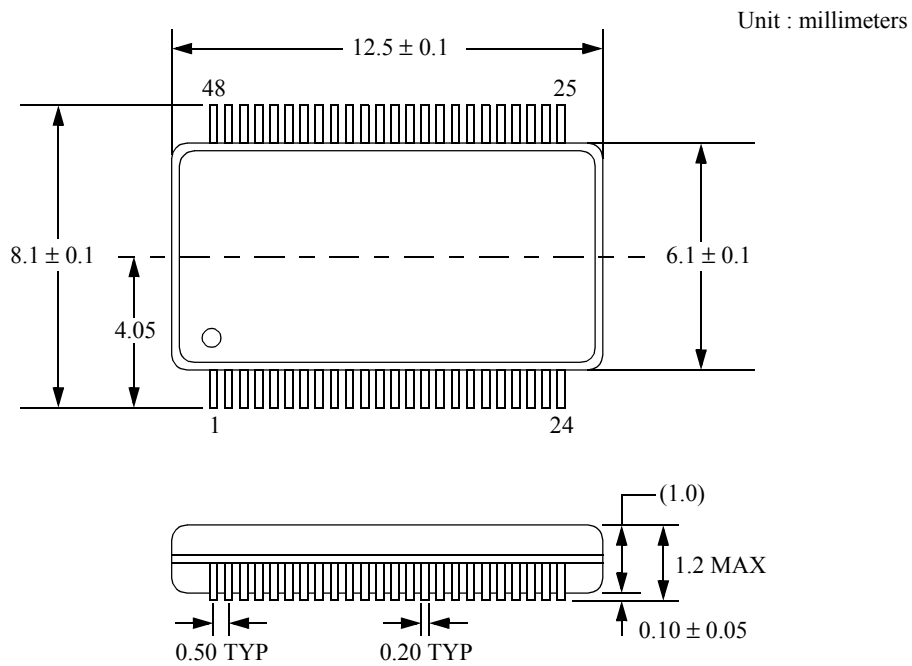


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48 Lead Molded Thin Shrink Small Outline Package, JEDEC



Notes to Users:

1. The contents of this data sheet are subject to change without prior notice.
2. Circuit diagrams shown in this data sheet are examples of application. Therefore, please pay sufficient attention when designing circuits. Even if there are incorrect descriptions, we are not responsible for any problem due to them. Please note that incorrect descriptions sometimes cannot be corrected immediately if found.
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5. We are making the utmost effort to improve the quality and reliability of our products. However, there is a very slight possibility of failure in semiconductor devices. To avoid damage to social or official organizations, much care should be taken to provide sufficient redundancy and fail-safe design.
6. No radiation-hardened design is incorporated in THC63LVDM83R/THC63LVDM63R.
7. Judgment on whether THC63LVDM83R/THC63LVDM63R comes under strategic products prescribed by the Foreign Exchange and Foreign Trade Control Law is the user's responsibility.
8. This technical document was provisionally created during development of THC63LVDM83R/THC63LVDM63R, so there is a possibility of differences between it and the product's final specifications. When designing circuits using THC63LVDM83R/THC63LVDM63R, be sure to refer to the final technical documents.

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