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Confidential

(Preliminary)

SPECIFICATIONS

PART No.: MN673276

The products and specifications are subject to change without any notice. Please ask for the latest Specifications to guarantee the satisfaction of your product requirements.

SYSTEM LSI DIVISION

SEMICONDUCTOR COMPANY

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

ESTABLISHED BY	APPLIED BY	CHECKED BY	PREPARED BY

DATE PREPARED	DATE ESTABLISHED				
June 28, 2002					

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☆ This document is based on an equivalent Japanese document that was prepared on Apr. 25, 2002.

1. Table of Contents

2. Product Type

LSI with A/D and D/A converters for digital signal processing (Y, C, ALC, AWB, and AGC) of cameras.

3. Function Overview

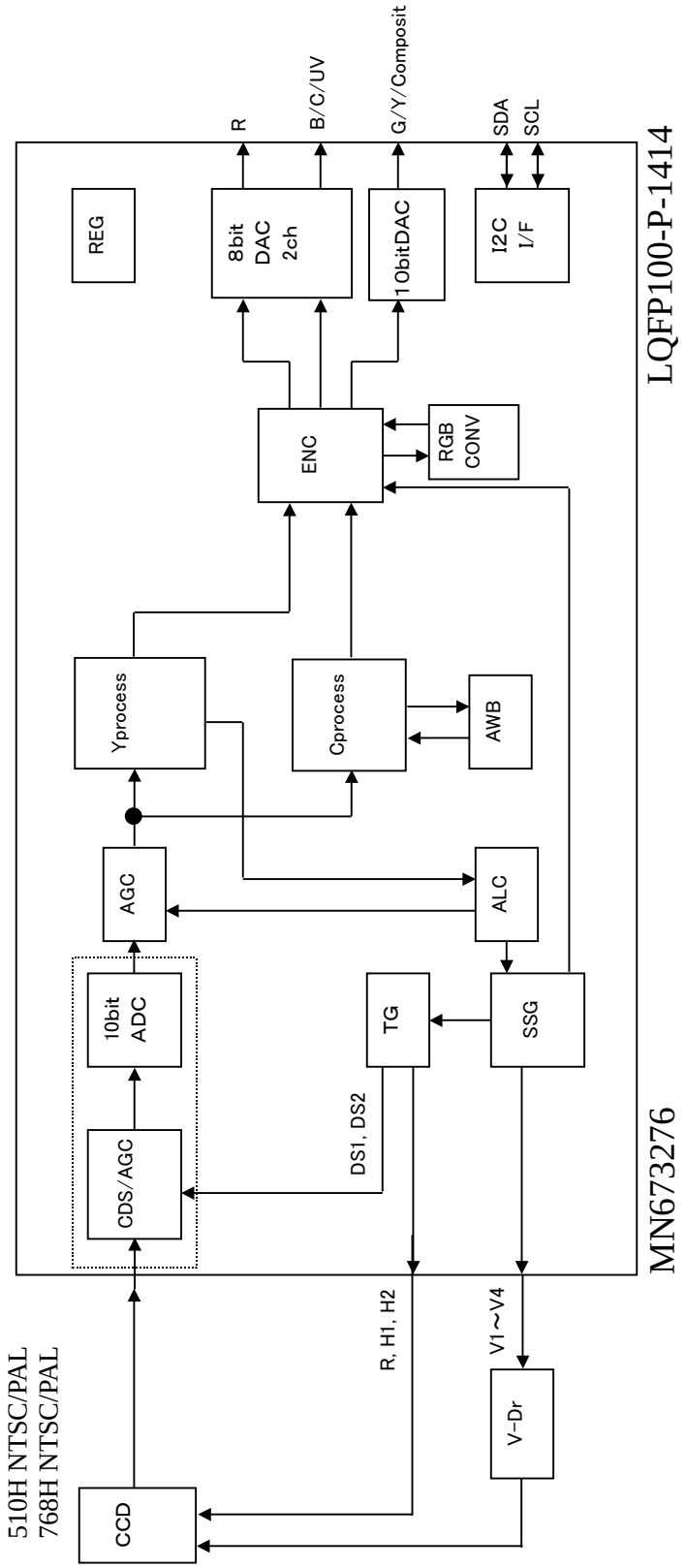
This is an LSI for monitoring cameras and PC inputs. In addition to its standard function, i.e. luminance and chroma signal processing, this LSI features ALC, AWB, and AGC, which have conventionally been left to a microprocessor, and an analog CDS/AGC circuit, which has conventionally been added externally. These features are integrated with SSG, CG, and I2C into a single chip.

4. Features

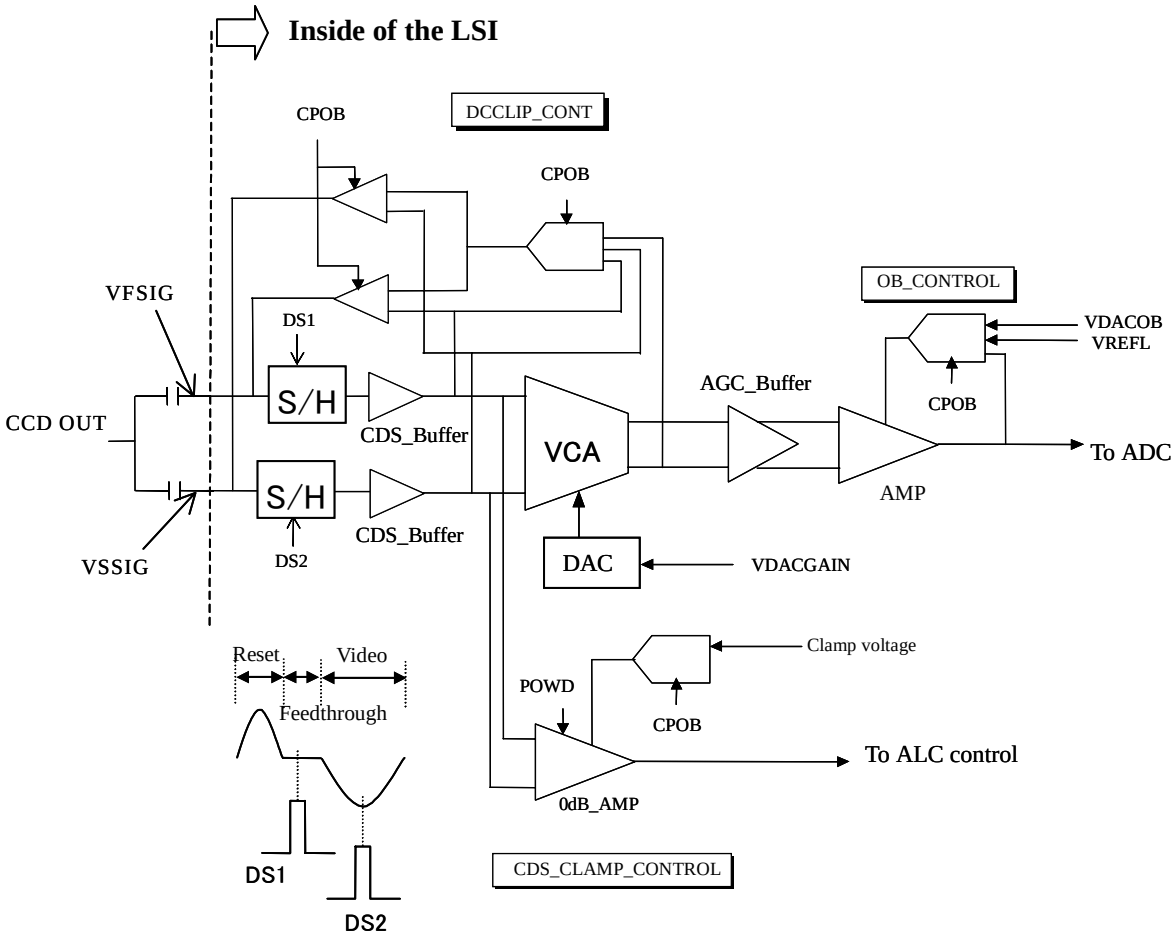
(1) Input: Analog signal (A/D input)
(2) Output: Analog output
Y signal
C signal
Composite output
RGB output
(3) Operating supply voltage:
3.3 V ± 0.3 V (IO, DAC, analog CDS/AGC)
2.0 V ± 0.2 V (internal logic, ADC)
(4) Operating frequency range: 9.5 MHz to 28.7 MHz
(5) Form to supply: LQFP100-P-1414
(6) Major functions

- Built-in 10-bit A/D converter
- Built-in 10-bit D/A converter (1 ch)
- Built-in 8-bit D/A converter (2 ch)
- Built-in analog CDS/AGC
- Built-in CG and SSG
- 510 H and 768 H (NTSC/PAL system)
- Monochrome CCD signal processing is available.
- CCD defect compensation circuit (including a color defect corrective function)
- Max. digital AGC gain: 18 dB
- Left/Right reversal function (controlled by external pins)
- Adjustable gamma (0.3 to 1)
- Supports external synchronization in HD/VD, VD2, SYNC, and LL modes.
- Built-in I2C bus
- ELC/AGC
- 2-mode white balance (Manual/ATW) with an ATW locking function
- OB auto corrective function (analog/digital)

5. Block Diagram



CDS/AGC/16-bit ADC Block Diagram



(1) The CCD output signals are input to VFSIG and VSSIG of the DSP, and sampled by DS1 and DS2. Then the signal components are output via the differential amplifier.
(Properly set the phases of DS1 and DS2 in the registers WEC2 and C3.)

(2) After amplification in the AGC amplifier, the OB level is added to the signals, and the signals are input to ADC.

6. Function Descriptions

(Functions of each block)

- CDS/AGC
  Conducts correlation double sampling on signals output from the CCD to sample signal components. This block also has an analog AGC circuit to perform AGC in an analog fashion.

- ADC
  Converts CCD signals subjected to CDS into 10-bit digital signals.

- PATGEN
  Generates pattern signals with three-color bars. Both horizontal and vertical patterns are available. This block emulates outputs from the four-complementary-color filters of the CCD. This is useful for isolating problems in the analog sections from CCD to ADC from those in the LSI.
  It can also be used as a blue background by temporarily stopping the video output from the CCD.

- AGC (AGC, Pixel MIX, Mirror image, and OB clamp)
  This is a digital AGC. It performs AGC in a digital fashion interlocked with ALC (Max. +18 dB). In the mirror mode of the 510 H/768 H-pixel CCD, video signals can be reversed by controlling the RAM. This block also corrects OB. The digital mode is for processing in the LSI, and the analog mode is to control the clamp voltage of the IC for CDS/AGC.

- ALC
  Performs full-screen center-weighted averaging metering according to luminance signal inputs, compares the result to a target optimum exposure value, and controls the electronic shutter of the CCD to electronically control the amount of light.
  During ELC, the AGC circuit is also used for smooth control because the accumulation time of the electronic shutter is discrete. This block also performs a 3-field averaging flicker control.

- Y system
  After generating a luminance signal using outputs from the complementary color filter CCD in LPF, this block generates horizontal and vertical aperture signals, and performs coring, low luminance suppression, gamma correction, and blanking. Two outline corrective levels are selectable in the external pin APGAIN.
  This block has a CCD defect compensation circuit. Gamma can be continuously adjusted from 0.3 to 1. Ready for monochrome CCD, bypassing the LPF for luminance signals is available.

- C system
  This block performs white balance processing, carrier balance, color temperature correction, and low/high luminance chroma suppression.

- AWB
  Generates auto white balance control signals. With low-illuminance scenes, the white balance operation holds just before an optimum illuminance status.

- ENC
  Modulates in accordance with the selection of NTSC/PAL. Integrates the clock systems into one system by adopting a digital VCO system, which generates 4fSC from FCK. To create composite video signals, Y signals are also mixed in a digital fashion by clock rate conversion. Digital mixing is available for SYNC.

- RGBconv
  This is a matrix circuit to convert YUV signals comprising Y and C signals into RGB signals. Note that the UV signal bands of all 3 channels are not the same as those of Y signals, unlike 3-CCD cameras, because the band of signals is reduced to approx. 800 kHz in the relatively early stages of the C signals.

- DAC
  Converts digital outputs into analog ones. There are three channels, one for composite, Y, and G signals. It also has a 10-bit accuracy for digital mixing of SYNC. The other two channels are 8-bit DAC for chroma, R, and B signals.

- PWM
  Has a 4-ch PWM output that can independently control analog circuits around the LSI.
  For example, this block can be used for adjusting VREF of DAC.

- CG
  Generates high-speed pulses for CCD (H1, H2, R, DS1, and DS2).
  The power supply for this logic block is separated from that of other logic blocks in the LSI to protect it from noise.

- SSG
  Generates low-speed pulses for CCD and other pulses for signal processing. Also supports external synchronization. (VBS Gen locking is not available.)

- I2C
  When the power is turned on, this block reads an external EEPROM and sets the registers in the LSI. Because this does not support multi-master, an external device should not be a master when the power is turned on.
  Read/write in the registers of the LSI from external devices are available (partly restricted).

7. Register Descriptions

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Adjustable Range	R/W
**H	I2C/SCL frequency switching @i2c (57h: 400 kHz Others: 100 kHz) Read mode switching as a master @i2c (0: Random read 1: Sequential read)	－＊＊＊＊＊＊＊ ＊－－－－－－－	80H		W W
00H	OB reference data @obclp (Reference data for digital clamping)	＊＊＊＊＊＊＊＊	40H		W
01H	H aperture coring @hvap	＊＊＊＊＊＊＊＊	0CH		W
02H	Color/Monochrome switching @ylpf (0: Monochrome 1: Color) (Not assigned)	－－－－－－－＊ ＊＊＊＊＊＊＊－	01H		W
03H	AGC threshold @hvap (When aperture gain decreases due to increase of AGC gain)	＊＊＊＊＊＊＊＊	FFH		W
04H	OB sample select @obclp (Horizontal phase setting: 0 is prohibited) 1T DSEL@obclp (0: 4T width 1: 8T wide-ready) OB clamp ON/OFF switching @obclp (0: ON 1: OFF (digital clamping ON/OFF))	－－＊＊＊＊＊＊ －＊－－－－－－ ＊－－－－－－－	84H		W W W
05H	HAP coring when AGC gain increases @hvap	＊＊＊＊＊＊＊＊	0CH		W
06H	NRST phase switching @RRAMCNT	＊＊＊＊＊＊＊＊	46H		W
07H	ON/OFF of AP gain decreasing when AGC gain increases @hvap (0: OFF 1: ON) AP gain when AGC gain increases @hvap (0: 1/2 1: 1/4) ON/OFF of AP coring up when AGC gain increases @ hvap (0: OFF 1: ON) AP gain decrease threshold hysteresis @hvap (Valid only when AGC gain increases)	－－－－－－－＊ －－－－－－＊－ －－－－－＊－－ ＊＊＊＊＊－－－	05H		W W W W
08H	(Not assigned) @i2c GATEWE @i2c (0: Normal 1: Gated clock mode) READ @i2c (0: Normal 1: Forcefully shifts to the master mode) (Not assigned)	－－－－－－－＊ －－－－－－＊－ －－－－－＊－－ ＊＊＊＊＊－－－	02H		 W W
09H	Edge coloring suppression: Suppression width switching @apcsup (00: 2 01: 3 10: 4 11: 5) Edge coloring suppression: Change amount switching @apcsup (00: 16 10: 8 11: 4) Edge coloring suppression: Max. suppression amount switching @apcsup (00: -25 dB 01: -3 dB 10: -6 dB 11: -12 dB) High illuminance color suppression: Suppression width switching @apg (00: 3 01: 4 10: 5 11: 1)	－－－－－－＊＊ －－－－＊＊－－ －－＊＊－－－－ ＊＊－－－－－－	E1H		W W W W
0AH	Luminance signal DC setting @yadj	＊＊＊＊＊＊＊＊	10H		W
0BH	Chroma coring @cgain	＊＊＊＊＊＊＊＊	06H		W

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Adjustable Range	R/W
0CH	BPF characteristic switching @prelp (0: (1+Z-2) 3 (1+Z-4) 1: (1+Z-2) 3 FCK 05 phase switching 1 @wbmpy FCK 05 phase switching 2 @wbmpy FCK 05 phase switching 3 @cgmlp FCK 05 phase switching 4 @rbmtx AWB gain fixing SW @wbmpy (0: Normal 1: Fixed WB gain) (Not assigned)	―――――――＊ ――――――＊― ――――――＊―― ―――――＊――― ――――＊―――― ―――＊――――― ――＊―――――― ＊＊――――――	00H		W W W W W W W
0DH	Base clip (B-Y) @cgain Base clip (R-Y) @cgain	―――＊＊＊＊ ＊＊＊＊―――	00H		W W
0EH	C gamma setup @cgset	＊＊＊＊＊＊＊＊	00H		W
0FH	B carrier balance @cgain (to be adjusted according to the video) R carrier balance @cgain (to be adjusted according to the video)	―――＊＊＊＊ ＊＊＊＊―――	00H		W W
10H	R-Y matrix gain @rbmtx (Not assigned)	―＊＊＊＊＊＊＊ ＊―――――――	02H		W
11H	CCD defect correction: White detection level LSB @mdf (OFF at FFH, Address 35H for MSB)	＊＊＊＊＊＊＊＊	FFH		W
12H	B-Y matrix gain @rbmtx (Not assigned)	―＊＊＊＊＊＊＊ ＊―――――――	22H		W
13H	CCD defect correction: Black detection level LSB @mdf (OFF at FFH, Address 35H for MSB)	＊＊＊＊＊＊＊＊	FFH		W
14H	R-Y gain @cgain	＊＊＊＊＊＊＊＊	9DH		W
15H	Flicker correction ON/OFF switching @fgain (00: ON 01: Y OFF 10: C OFF 11: YC OFF) (Not assigned)	―――――＊＊ ＊＊＊＊＊＊――	00H		W
16H	B-Y gain @cgain	＊＊＊＊＊＊＊＊	86H		W
17H	YC phase adjustment @ycdsel UV output control: FH2 phase adjustment @ycdsel UV output control: FC05 phase adjustment @ycdsel UV output control: UV phase adjustment @ycdsel UV output control: C/UV output switching @ycdsel (0: C 1: UV)	―――＊＊＊＊ ―――＊――― ――＊――― ―＊――― ＊―――――	O5H		W W W W W
18H	Y gain @yadj (1x at 80H)	＊＊＊＊＊＊＊＊	80H		W
19H	AGC-interlocked aperture suppression factor @aagc (00: 1 01: 1/2 10: 1/4 11: 3/8) AGC-interlocked color suppression factor @aagc (00: 1 01: 1/2 10: 1/4 11: 3/8)	――――――＊＊ ――――＊＊――	00H		W W

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Adjustable Range	R/W
1AH	Negative/Positive switching @yadj (0: Normal 1: Negative) Normal input/ramp waveform input switching @yadj (0: Normal input 1: Ramp waveform input) (Not assigned)	―――――――＊ ――――――＊― ＊＊＊＊＊＊＊――	00H		W W
1BH	Color defect correction setting @ckizu (00: Correction OFF 10: 2-pixel continuous 11: 1-pixel forced) (Not assigned)	――――――＊＊ ＊＊＊＊＊＊――	00H		W
1CH	Color gain decrease aperture offset @apcsup (Off at 7FH) Edge color suppression: VAP suppression ON/OFF switching @apcsup (0: OFF 1: ON)	―＊＊＊＊＊＊＊ ＊――――――	7FH		W W
1DH	AWB saturation level @sat (OFF at FFH)	＊＊＊＊＊＊＊＊	FFH		W
1EH	AGC-interlocked aperture suppression offset @aagc (OFF at FFH)	＊＊＊＊＊＊＊＊	FFH		W
1FH	AGC-interlocked color suppression offset @aagc (OFF at FFH)	＊＊＊＊＊＊＊＊	FFH		W
20H	RGBCNV U gain @rgb1 (1x at 80H)	＊＊＊＊＊＊＊＊	80H		W
21H	RGBCNV V gain @rgb1 (1x at 80H)	＊＊＊＊＊＊＊＊	80H		W
22H	FC05 phase switching @rgb1 UV phase adjustment	―――――――＊ ――――――＊―	00H		W W
23H	R factor @rgb1 (Factor 0.5 at 80H)	＊＊＊＊＊＊＊＊	4CH		W
24H	B factor @rgb1 (Factor 0.5 at 80H)	＊＊＊＊＊＊＊＊	1DH		W
25H	R gain @rgb2 (1x at 80H)	＊＊＊＊＊＊＊＊	80H		W
26H	B gain @rgb2 (1x at 80H)	＊＊＊＊＊＊＊＊	80H		W
27H	G gain @rgb2 (1x at 40H)	＊＊＊＊＊＊＊＊	6DH		W
28H	R offset @rgb2	＊＊＊＊＊＊＊＊	00H		W
29H	B offset @rgb2	＊＊＊＊＊＊＊＊	00H		W
2AH	G offset @rgb2	＊＊＊＊＊＊＊＊	00H		W
2BH	Insufficient blackening correction start level @yadj (The pedestal sinks at this AGC gain value or less)	＊＊＊＊＊＊＊＊	00H		W
2CH	Insufficient blackening correction low clip value (Clip value: Register value - 64)	―＊＊＊＊＊＊＊	00H		W
2DH	Insufficient blackening correction gain setting (000: 1/16 001: 1/8 010: 1/4 011: 1/2 100: 1 101: 2) Insufficient blackening correction ON/OFF (0: OFF 1: ON) (Not assigned)	―――――＊＊＊ ―――＊――― ＊＊＊＊――――	00H		W W
2EH	PWM0	＊＊＊＊＊＊＊＊	00H		W
2FH	PWM1	＊＊＊＊＊＊＊＊	00H		W

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Adjustable Range	R/W
30H	Digital OB control coring setting Digital OB control hysteresis setting	―――――＊＊＊ ＊＊＊＊＊―――	19H		W W
31H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
32H	Internal AD/External AD switching @obclp (0: Normal 1: External AD) Test/Normal switching @ (0: Normal 1: Color bar) (Not assigned) AD power down ON/OFF (0: OFF 1: ON (HCLR = Power down for “H” period) (Not assigned) D clamp/A clamp switching (0: D clamp 1: A clamp)	―――――――＊ ――――――＊― ―――＊＊―― ――＊―――― ―＊＊―――― ＊―――――――	10H		W W W W
33H	OB auto correction reference value @obclp (OB reference value)	＊＊＊＊＊＊＊＊	40H		W
34H	(Not assigned) Number of OB sampling times switching @obclp (00: 256 01: 128A 10: 128B 11: 256 (Same as "00")) Reversing video left to right @RRAMCNT (0: Normal 1: Reversed left to right)	―――――＊＊ ―――＊＊―― ――＊――――	00H		 W W
35H	CCD defect correction: White detection level MSB @mdf (Address 11H for LSB) CCD defect correction: Black detection level MSB @mdf (Address 13H for LSB) (Not assigned)	―――――＊＊ ―――＊＊―― ＊＊＊＊―――	0FH		W W
36H	Offset decrement @ladd (Offset: 64 (40H) for 10-bit data)	＊＊＊＊＊＊＊＊	80H		W
37H	Aperture low illuminance suppression offset @apg 00H: OFF	＊＊＊＊＊＊＊＊	00H		W
38H	High illuminance color suppression off set @apg FFH: OFF	＊＊＊＊＊＊＊＊	90H		W
39H	Low illuminance color suppression offset @apg 00H: OFF	＊＊＊＊＊＊＊＊	00H		W
3AH	Aperture low illuminance suppression factor @apg (00: 1 01: 1/2 10: 1/4 11: 3/8) High illuminance color suppression factor @apg (00: 1 01: 1/2 10: 1/4 11: 3/8 100: 0) Low illuminance color suppression factor @apg (00: 1 01: 1/2 10: 1/4 11: 3/8) (Not assigned)	―――――＊＊ ―――＊＊＊―― ―＊＊―――― ＊―――――――	03H		W W W W
3BH	VAP coring @hvap	＊＊＊＊＊＊＊＊	0CH		W
3CH	VAP coring when AGC gain increases @ hvap	＊＊＊＊＊＊＊＊	0CH		W
3DH	HAP gain @hvap (Adjustable from 0x to 4x)	＊＊＊＊＊＊＊＊	40H		W
3EH	VAP gain @hvap (Adjustable from 0x to 4x)	＊＊＊＊＊＊＊＊	40H		W
3FH	Test switching when mounted @yadj (0: Normal 1: Test) Aperture decrease amount switching @hvap (0: Decreasing by 100% 1: Decreasing by 50%)	―――――――＊ ――――――＊―	00H		W W

ADR	Data Descriptions	Data Configuration	Standard Setting		Adjustable Range	R/W
		76543210	NTSC 510/768	PAL 510/768		
40H	ALC full-screen averaging in H direction start @alclp	********	13H/14H	13H/14H		W
41H	ALC full-screen averaging in H direction end @alclp	********	89H/C8H	89H/C8H		W
42H	ALC full-screen averaging in V direction start @alclp	********	0CH	13H		W
43H	ALC full-screen averaging in V direction end Lower 8B @alclp	********	FCH	2FH		W
44H	ALC full-screen averaging in V direction end MSB @alclp ALC full-time 3 V control ON/OFF selecting (0: Normal 1: Full-time 3 V control)	-------* ------*-	00H	01H		W W
45	Setting a particular period after powering on @alclp ON/OFF setting in a particular period after powering on @alclp (0: ON 1: OFF)	-******* *-------	40H	40H		W W
46H	Center weighting in H direction start @alcar	********	27H/3CH	27H/3CH		W
47H	Center weighting in H direction end @alcar	********	4EH/78H	4EH/78H		W
48H	Center weighting in V direction start @alcar	********	53H	61H		W
49H	Center weighting in V direction end Lower 8 bits @alcar (Address 4DH for MSB)	********	A3H	C0H		W
4AH	Number of sub output lines in the low-speed shutter mode @hactr Number of sub output lines in the mid-speed shutter mode @hactr Switching sub output system (0: Fixed change rate 1: Adjustable)	----**** -***---- *-------	28H	28H		W W W
4BH	Shutter high/mid speed threshold (HSSO/2 setting) @hactr	********	CAH	65H		W
4CH	Shutter mid/high speed threshold (HSSO/2 setting) @hactr	********	4BH	25H		W
4DH	ELC (normal) response speed switching (in fixed change rate mode) @hactr (0: 1/4 1: 1/8 2: 1/16 3: 1/32) HSSMAX MSB for sub calculation when outputting H rate (Address 4EH for lower 8 bits) HSSMAXH MSB for sub calculation when outputting 1/16H (Address 4FH for lower 8 bits) Center weighting in V direction end MSB @alcar (Address 49H for lower 8 bits)	------** -----*-- ----*--- ---*----	05H	01H		W W W W
4EH	HSSMAX for 1H control sub output calculation @hactr (For PAL, HSSO/2 setting)	********	06H	9CH		W
4FH	HSSMAXH for 1/16H control sub calculation @hactr (For PAL, HSSO/2 setting)	********	DDH	96H		W

ADR	Data Descriptions	Data Configuration	Standard Setting		Adjustable Range	R/W
		76543210	NTSC 510/768	PAL 510/768		
50H	AGC change amount in HSM @hactr Number of sub output lines in the initial area of 1/16H rate	---***** ***-----	62H	62H		W W
51H	ELC (HSM) response speed switching @hactr (0: 1/2 1: 1/4 2: 1/8 3: 1/16 4: 1/32) ELC speed switching in the high-speed mode after powering on ON/OFF in high-speed mode after powering on (0: ON 1: OFF) (Not assigned)	-----*** --***--- -*------ *-------	0AH	01H		W W W W
52H	Setting of max. number of sub output lines MSB @hssun (Address 55H for lower 8 bits) Register setting YAVE ON/OFF @alcct (0: Normal 1: YAVE of the register value)	------** -----*--	01H	02H		W W
53H	Register setting YAVE @alcct	********	00H	00H		W
54H	(Not assigned)					
55H	Setting of max. number of sub output lines Lower 8B@hssun	********	D4H	50H		W
56H	Gain setting when AGC is off @agcun	********	00H	00H		W
57H	AGC response speed switching ON/OFF (ALCNEAR control) @agcun (0: Speed switching 1: Speed fixed) AGC response speed setting (0: 1x 1: 2x) AGC ON/OFF selecting (0: ON 1: OFF) AGC mode switching (0: Digital AGC 1:Analog AGC)	-------* ------*- -----*-- ----*---	09H	09H		W W W W
58H	AGC max. setting @agcun	********	80H	80H		W
59H	Analog AGC offset @agcun	********	40H	40H		W
5AH	Digital AGC offset @agcun	********	20H	20H		W
5BH	(Not assigned)					
5CH	Flicker gain selecting @fgain Gain setting when flicker correction in low illuminance scene is off	-------* *******-	FFH	FFH		W W
5DH	Flicker OFF threshold in low illuminance scene @fgain	********	0AH	0AH		W
5EH	ALC HSM threshold: Higher than the target value @alcct	********	76H	76H		W
5FH	ALC HSM threshold: Lower than the target value @alcct	********	14H	14H		W
60H	ALC target value (in BLCON state) @alcct	********	4CH	4CH		W
61H	ALC target value (in BLCOFF state) @alcct	********	26H	26H		W
62H	Convergence coring offset setting @alcct Coring setting when AGC is ON	----**** ****----	63H	63H		W W

ADR	Data Descriptions	Data Configuration	Standard Setting		Adjustable Range	R/W
		76543210	NTSC 510/768	PAL 510/768		
63H	Threshold of 1 V/3 V control switching in the normal state @alcct Coring ON/OFF when AGC is ON (0: OFF 1: ON (1 V only)) Convergence coring setting (0: 1/64 1: 1/128 2: 1/256 3: 1/256)	---***** --*----- **------	6AH	2AH		W W W
64H	Threshold of sub output rate switching (ALCNEAR) @alcct Coring when BLC is ON IRIS 1 V/3 V control switching (0: ON 1: OFF)	---***** -**----- *-------	CCH	CCH		W W W
65H	ULI Threshold higher than the target value @alcct	********	98H	98H		W
66H	ULI Threshold lower than the target value @alcct	********	20H	20H		W
67H	Area A weighting coefficient in the BLCOFF state @alcav (08H: x 1)	********	08H	08H		W
68H	Area A weighting coefficient in the BLCON state @alcav	********	08H	08H		W
69H	IRIS change amount switching threshold (IRISNEAR) @alcct HSM 3 V/1 V control switching (0: Switching (1/3 V) 1: Fixed (1 V only)) ON/OFF switching of high-speed mode after powering on (0: ON 1: OFF) HSM ON/OFF switching	---***** --*----- -*------ *-------	0BH	0BH		W W W W
6AH	Area B weighting coefficient in the BLCOFF state @alcav (20H: x 4)	--******	20H	20H		W
6BH	Area B weighting coefficient in the BLCON state @alcav (20H: x 4)	--******	20H	20H		W
6CH	Area C weighting coefficient in the BLCOFF state @alcav (10H: x 2)	--******	10H	10H		W
6DH	Area C weighting coefficient in the BLCON state @alcav (10H: x 2)	--******	10H	10H		W
6EH	IRIS coring value setting @alcct	---*****	00H	00H		W
6FH	SUB output when ALCELC = H @hssun	********	40H	40H		W
70H	IRIS offset in BLCOFF state (ALCDC) @hssun	********	00H	00H		W
71H	IRIS offset in BLCON state (ALCDC) @hssun	********	10H	10H		W
72H	LSB of sub 1/16H rate output start position @hssun	********	F7H	24H		W
73H	LSB of sub output setting when ALCELC = L @	********	00H	00H		W

ADR	Data Descriptions	Data Configuration 76543210	Standard Setting NTSC 510/768	Standard Setting PAL 510/768	Adjustable Range	R/W
74H	ALC ON/OFF switching @hssun (0: ON 1: OFF) MSB of sub 1/16H rate output start position MSB of sub output setting when ALCELC = L (Not assigned) ELC_ONLY mode (0: ON 1: OFF (Set LSB to 1 first.))	-------* -----**- ---**--- --*----- -*------	00H	02H		W W W W
75H	IRIS upper limit setting @hssun	********	01H	01H		W
76H	Screen-averaged value (Calculated value read)	********				R
77H	H-rate shutter value HSSO LSB (Calculated value read)	********				R
78H	1/16 shutter value HSSOS (Calculated value read) H-rate shutter value HSSO MSB	----**** --**----				R R
79H	Digital AGC gain (Calculated value read)	********				R
7AH	Analog AGC gain (Calculated value read)	********				R
7BH	AGC gain (before adding offset) (Calculated value read)	********				R
7CH	OB tracking speed switching threshold @obclp OB tracking speed switching @obclp (0: 8x speed 1: 16x speed)	---***** --*-----	34H	34H		W W
7DH	Analog OB control offset @obclp	********	00H	00H		W
7EH	LSI CODE @agcreg (LSI development code (register read only))	********		03H		R
7FH	LSI Version @agcreg (LSI development version (register read only))	********		01H		R

ADR	Data descriptions	Data configuration 7 6 5 4 3 2 1 0	Standard setting	Reset setting	R/W
80H	Full-screen averaging in H direction start position @awblp	＊＊＊＊＊＊＊＊	1CH		W
81H	Full-screen averaging in H direction end position LSB @awblp	＊＊＊＊＊＊＊＊	1AH		W
82H	Full-screen averaging in H direction end MSB @awblp	――――――＊＊	43H		W
	Full-screen averaging in V direction end MSB @awblp	―――――＊――			W
	Full-screen averaging 1 V/3 V selecting (V3OFF) @awblp (0: 3 V 1: 1 V)	――――＊―――			W
	HCLR/TESTHD, VD/TESTVD selecting @awblp (0: HD, VD 1: TESTHD, TESTVD)	―――＊―――			W
	Horizontal addition divisor switching @awblp (0: 1/128 1: 1/256)	――＊―――			W
	ATWLOCK register switching @wbgai (00: Pin control 01: Normal 11: ATWLOCK)	＊＊―――――			W
83H	Full-screen averaging in V direction start position @awblp	＊＊＊＊＊＊＊＊	0DH		W
84H	Full-screen averaging in V direction end position LSB @awblp	＊＊＊＊＊＊＊＊	FDH		W
85H	AWB response speed switching (for power-on mode) @awblp (0: 1/16 V 1: 1/8 V 2: 1/4 V 3: 1/2 V 4: 1/1 V)	―――＊＊＊	24H		W
	AWB response speed switching (for normal mode) @awblp (0: 1/16 V 1: 1/8 V 2: 1/4 V 3: 1/2 V 4: 1/1 V)	――＊＊＊―――			W
	Default when power-on mode is off @awblp	―＊―――――			W
	Power-on mode ON/OFF switching @awblp (0: POWR used 1: Default used)	＊―――――――			W
86H	Drive pulse setting for AWB gain calculation (F4A, F2A) @awblp	―――＊＊＊＊＊	10H		W
	AWB delay adjustment @wbave (0: 0T (without delay) 1: 1T added)	――＊―――――			W
	POWR selecting (V3 control) @wbave (0: V3 control (V3 invalid when POWR is "H") 1: V3 through)	―＊―――――			W
	Long-time storage mode setting @wbave (0: Long-time storage mode ON 1: OFF)	＊―――――――			W
87H	AWB gain clip CG lower limit MSB @wbgai	―――――――＊	3AH		W
	AWB gain clip CG upper limit MSB @wbgai	――――――＊―			W
	AWB gain clip CMg lower limit MSB @wbgai	―――――＊――			W
	AWB gain clip CMg upper limit MSB @wbgai	――――＊―――			W
	AWB OFF gain setting R-Y MSB @wbgai	―――＊―――――			W
	AWB OFF gain setting B-Y MSB @wbgai	――＊―――――			W
	AWB ON/OFF switching @wbgai (0: ON 1: OFF)	―＊―――――			W
	(Not assigned)	＊―――――――			
88H	AWB gain clip CG lower limit LSB @wbgai (0F6H)	＊＊＊＊＊＊＊＊	80H		W
89H	AWB gain clip CG upper limit LSB @wbgai (10BH)	＊＊＊＊＊＊＊＊	40H		W
8AH	AWB gain clip CMg lower limit LSB @wbgai (0F3H)	＊＊＊＊＊＊＊＊	40H		W
8BH	AWB gain clip CMg upper limit LSB @wbgai (10FH)	＊＊＊＊＊＊＊＊	80H		W
8CH	AWB OFF gain setting R-Y LSB @wbgai5 (0D9H)	＊＊＊＊＊＊＊＊	D9H		W

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Reset Setting	R/W
8DH	AWB OFF gain setting B-Y LSB @wbgai (12CH)	＊＊＊＊＊＊＊＊	2CH		W
8EH	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
8FH	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
90H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
91H	AWB response speed switching ON/OFF SW @wbgai (0: OFF 1: ON) Switching AWB convergence speed in normal mode @wblpf (0: 1 or 4 convergence 1: 1 or 8 convergence) (Not assigned)	－－－－－－－＊ －－－－－－＊－ ＊＊＊＊＊＊－－	01H		W W W
92H	AWB gain coring hysteresis setting @wblpf ATWLOCK register switching @wblpf (00: Pin control 01: Normal 11: ATWLOCK) (Not assigned)	－－－＊＊＊＊＊ －＊＊－－－－－ ＊－－－－－－－	22H		W W W
93H	AWB gain coring hysteresis setting @wblpf (Hysteresis valid at this value or less) Power-on mode ON/OFF SW @wblpf (0: ON 1: OFF) Default when power-on mode is off @wblpf (Not assigned)	－－－＊＊＊＊＊ －－＊－－－－－ －＊－－－－－－ ＊－－－－－－－	02H		W W W
94H	AWB gain initial value 1 (CG) @wblpf (40H x 8 = 200H)	＊＊＊＊＊＊＊＊	40H		W
95H	AWB gain initial value 2 (YM) @wblpf (40H x 8 = 200H)	＊＊＊＊＊＊＊＊	40H		W
96H	AWB gain initial value 3 (CM) @wblpf (40H x 8 = 200H)	＊＊＊＊＊＊＊＊	40H		W
97H	AWB gain initial value 4 (YG) @wblpf (40H x 8 = 200H)	＊＊＊＊＊＊＊＊	40H		W
98H	AWB response speed switching threshold 1 @wblpf (± 2 for power-on)	＊＊＊＊＊＊＊＊	10H		W
99H	AWB response speed switching threshold 2 @wblpf (± 4 for power-on)	＊＊＊＊＊＊＊＊	20H		W
9AH	AWB response speed switching threshold 3 @wblpf (± 8 for power-on)	＊＊＊＊＊＊＊＊	40H		W
9BH	AWB response speed switching threshold A @wblpf (± 1 or ± 4 or ± 8 for normal mode)	＊＊＊＊＊＊＊＊	1FH		W
9CH	AWB YM average LSB @wbave (READ data)	＊＊＊＊＊＊＊＊			R
9DH	AWB CG average LSB @wbave (READ data)	＊＊＊＊＊＊＊＊			R
9EH	AWB YG average LSB @wbave (READ data)	＊＊＊＊＊＊＊＊			R
9FH	AWB CM average LSB @wbave (READ data)	＊＊＊＊＊＊＊＊			R

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Reset Setting	R/W
A0H	AWB YM average MSB @wblpf (READ data) AWB CG average MSB @ (READ data) AWB YG average MSB @ (READ data) AWB CM average MSB @ (READ data)	――――――＊＊ ――――＊＊―― ――＊＊―――― ＊＊―――――――			R R R R
A1H	LSB of calculated AWB YM gain @wblpf (READ data)	＊＊＊＊＊＊＊＊			R
A2H	LSB of calculated AWB CG gain @wblpf (READ data)	＊＊＊＊＊＊＊＊			R
A3H	LSB of calculated AWB YG gain @wblpf (READ data)	＊＊＊＊＊＊＊＊			R
A4H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
A5H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
A6H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
A7H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
A8H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
A9H	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
AAH	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
ABH	LSB of calculated AWB CM gain @wblpf (READ data)	＊＊＊＊＊＊＊＊			R
ACH	MSB of calculated AWB YM gain @wblpf (READ data) MSB of calculated AWB CG gain @wblpf (READ data) MSB of calculated AWB YG gain @wblpf (READ data) MSB of calculated AWB CM gain @wblpf (READ data)	――――――＊＊ ――――＊＊―― ――＊＊―――― ＊＊―――――――			R R R R
ADH	(Not assigned)	＊＊＊＊＊＊＊＊	00H		
AEH	AWB test mode (TM8) (0h: YMave 1h: CGave 2h: YGave 3h: CMave 4h: WBYMGAIN 5h: WBYGGAIN 6h: YMgain) A/D test mode (7h: CGain 8h: YGain 9h: CMgain) (Not assigned)	――――＊＊＊＊ ―――＊―――― ＊＊＊――――	00H		W W
AFH	ALC test mode (TM9) @alcav (0h: Yave 1h: ALCcnt 2h: HSScnt 3h: AGCcnt 4h: MSCB 5h: Fgain 6h: HSSOUT 7h: HSSOS 8h: HSSO Ah: AGCOC Bh: DAGC Ch: ANAGC (0: Normal 1 1: Test)) ALC test input (Not assigned)	――――＊＊＊＊ ―――＊―――― ＊＊＊――――	00H		W W

- **Standard setting of the AWB metering area**

The delay between the MN673276 input VIN to the AWB input DATAIN (9:0) is 23T, and a total of 28.5 (29T) including delays of input PAD (1T), inside AWB (1T), CDS (1T), and A/D (2.5T).
The AWB metering area is set taking into account this video signal delay.
In regard to the H direction, the video signal delay is calculated based on the falling edge of HCLR. According to the calculation result, a metering area is set so that horizontal 480-pixel data is sampled for 510H CCD, or 720-pixel data for 768H CCD. In regard to the V direction, a metering area is set so that 230-line data is sampled for NTSC, or 280-line data for PAL, based on the falling edge of VD.

The list below shows standard mode-by-mode settings of the AWB metering area.
The modes are:

Start of full-screen averaging in the H direction (Hstart), End of full-screen averaging in the H direction (Hend)
Start of full-screen averaging in the V direction (Vstart), End of full-screen averaging in the V direction (Vend)

CCD	CCDSEL(2:0)	NT/PAL	Hstart	Hend	Vstart	Vend
510H MN39110 /210	CCDSEL(2:0)=0h	NTSC PAL	Hstart= 53(35h) Hstart= 53(35h)	Hend=539(21Bh) Hend=539(21Bh)	Vstart= 13(0Dh) Vstart= 19(13h)	Vend=243(F3h) Vend=299(12Bh)
	CCDSEL(2:0)=1h					
768H MN39143 /243	CCDSEL(2:0)=2h	NTSC PAL	Hstart= 53(35h) Hstart= 53(35h)	Hend=779(30Bh) Hend=779(30Bh)	Vstart= 12(0Ch) Vstart= 18(12h)	Vend=242(F2h) Vend=298(12Ah)
510H MN39117 /217	CCDSEL(2:0)=3h	NTSC PAL	Hstart= 53(35h) Hstart= 53(35h)	Hend=539(21Bh) Hend=539(21Bh)	Vstart= 13(0Dh) Vstart= 19(12h)	Vend=243(F3h) Vend=299(12Bh)
768H MN37140 /39241	CCDSEL(2:0)=4h	NTSC PAL	Hstart= 53(35h) Hstart= 53(35h)	Hend=779(30Bh) Hend=779(30Bh)	Vstart= 12(0Ch) Vstart= 19(13h)	Vend=242(F2h) Vend=299(12Bh)

* For PAL, the register address 82 (Addition data for full-screen averaging in the V direction 1/2 selecting: AVPAL) should be set to "H".

Correlation between CCDSEL (2:0) and CCD type

CCDSEL(2:0)=0h	510 pixels MN39110 (NTSC)	1H=606T	510 pixels MN39210 (PAL)	1H=618T
CCDSEL(2:0)=1h	———	——	———	——
CCDSEL(2:0)=2h	768 pixels MN39143 (NTSC)	1H=910T	768 pixels MN39243 (PAL)	1H=910T
CCDSEL(2:0)=3h	510 pixels MN39117 (NTSC)	1H=606T	510 pixels MN39217 (PAL)	1H=606T
CCDSEL(2:0)=4h	768 pixels MN37140 (NTSC)	1H=910T	768 pixels MN39241 (PAL)	1H=910T

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Reset Setting	R/W
B0H	Breakpoint 1 of broken line γ @gamma	＊＊＊＊＊＊＊＊	72H		W
B1H	Breakpoint 2 of broken line γ @gamma	＊＊＊＊＊＊＊＊	FFH		W
B2H	Slope α1 @gamma (determined value)	＊＊＊＊＊＊＊＊	B3H		W
B3H	Slope α2 @gamma (Slope: 1/4)	＊＊＊＊＊＊＊＊	2BH		W
B4H	Slope α3 @gamma (Slope: 1/4)	＊＊＊＊＊＊＊＊	40H		W
B5H	Y intercept β1 @gamma (determined value)	＊＊＊＊＊＊＊＊	00H		W
B6H	Y intercept β2 @gamma	＊＊＊＊＊＊＊＊	8DH		W
B7H	Y intercept β3 @gamma	＊＊＊＊＊＊＊＊	C6H		W
B8H	Broken line γ ON/OFF @gamma (0: OFF 1: ON) Negative γ control @gamma (0: Through 1: Gamma) Gamma switching @gamma (0: 0.3 1: MN67352 equivalent)	－－－－－－－＊ －－－－－－＊－ －－－－－＊－－	05H		W W W
B9H	γ characteristic switching @gamma (80H: 0.5x C0H: γ = 0.45 00H: OFF)	＊＊＊＊＊＊＊＊	FFH		W
BAH	Broken line start level @gamma	＊＊＊＊＊＊＊＊	72H		W
BBH	Edge detection threshold @prelp	＊＊＊＊＊＊＊＊	88H		W
BCH	Signal phase switching for AWB @prelp	－－－－－－＊＊	02H		W
BDH	HAP LPF ON/OFF switching @hvap (0: OFF 1: ON) VAP LPF characteristic switching @hvap (0: (1+Z-1)2 1: (1+Z-1)2(1+Z-2)) VAP LPF ON/OFF switching @hvap (0: OFF 1: ON)	－－－－－－－＊ －－－－－－＊－ －－－－－＊－－	00H		W W W
BEH	Gain for level adjustment @fgain (0 to 1x)	＊＊＊＊＊＊＊＊	FFH		W
BFH	(Not assigned)				
C0H	High-speed pulse phase setting 0 (H1, H2)	＊＊＊＊＊＊＊＊	02H		W
C1H	High-speed pulse phase setting 1 (R)	＊＊＊＊＊＊＊＊	02H		W
C2H	High-speed pulse phase setting 2 (DS1)	＊＊＊＊＊＊＊＊	02H		W
C3H	High-speed pulse phase setting 3 (DS2)	＊＊＊＊＊＊＊＊	02H		W
C4H	High-speed pulse phase setting 4 ENC block Y clock switching (0: Crystal oscillation 1: LC oscillation) CBLK, CSYNC phase adjustment (-8T to +7T (Standard: 0T)) TG output enable signal (0: Internal TG 1: External TG)	－－－－－－＊＊ －－－－－＊－－ －＊＊＊＊－－－ ＊－－－－－－－	44H		W W W W
C5H	Normal/Flicker-less/ ELC switching (00: Normal 10: Flicker-less 11: ELC) CH1, 2 pulse reversing SUB pulse reversing V1 pulse reversing V2 pulse reversing V3 pulse reversing V4 pulse reversing	－－－－－－＊＊ －－－－－＊－－ －－－－＊－－－ －－－＊－－－－ －－＊－－－－－ －＊－－－－－－ ＊－－－－－－－	00H		W W W W W W W
C6H	HSSOS setting register HSSO setting register LSB	－－－－＊＊＊＊ ＊＊＊＊－－－－	00H		W W

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Reset Setting	R/W
C7H	HSSO setting register MSB	——＊＊＊＊＊＊	80H		W
	FIN invalid signal	—＊————			W
	HSSOS, HSSO register setting switching (0: Internal connection (to ALC block) 1: Register)	＊————			W
C8H	FHRST delay switching (–15T to +16T (Standard: 0T))	———＊＊＊＊＊	10H		W
	LLDET mode switching	——＊————			W
	VD selecting signal (0: CSYNC 1: VD)	—＊————			W
	Processing when VCO is unnecessary (0: With VCO 1: Without VCO)	＊————			W
C9H	Fine adjustment of H phase in the synchronization mode SYNC	＊＊＊＊＊＊＊＊	80H		W
CAH	Fine adjustment of H phase in the synchronization mode HDVD	＊＊＊＊＊＊＊＊	80H		W
CBH	CPOB rising edge phase setting (CPOB start setting value (0T to 31T))	———＊＊＊＊＊	06H		W
	TM3 mode output control switching	——＊————			W
CCH	CPOB falling edge phase setting (CPOB stop setting value (0T to 31T))	———＊＊＊＊＊	0AH		W
CDH	CPOB rising edge phase setting (CPOB2 start setting value (0T to 31T))	———＊＊＊＊＊	06H		W
CEH	CPOB falling edge phase setting (CPOB2 stop setting value (0T to 31T))	———＊＊＊＊＊	0AH		W
CFH	CPOB/HCLR/FVD/CPOB2 output switching (00: CPOB 01: HCLR 10: FVD 11: CPOB2)	———————＊＊	00H		W
	PBLK/CBLK/WHD output switching (00: PBLK 01: CBLK 10: WHD)	————＊＊——			W
	PWM3/FCKO/F2CKO output switching (100: PWM3 01: FCKO 10: FCKO2)	——＊＊————			W
		＊＊————			W

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Reset Setting	R/W
D0H	(R-Y)/(B-Y) switching after DD (1: Rch = (B-Y) 0: Rch = (R-Y)) Rch/Bch phase switching after DD (1: Rch +1T 0: Bch +1T) YC/RGB switching (1: RGB 0: YC) 10-bit DAC output chroma SW (1: Y only 0: Y+C) 10-bit DAC output SYNC SW (1: SYNC OFF 0: SYNC ON) YC/Y, UV switching (1: Y, UV 0: YC)	―――――――＊ ――――――＊― ―――――＊―― ――――＊――― ―――＊―――― ――＊―――――	02H		W W W W W W
D1H	Y data interpolation SW after DD (00: LPF OFF (00 or 01 or 11)) C data interpolation SW after DD (00: LPF OFF (00 or 01 or 11)) Y-line delay adjustment after DD (0 to 7: -1T to +6T)	――――――＊＊ ――――＊＊―― ―＊＊＊―――	15H		W W W
D2H	(R-Y) burst level for NTSC (use at NTSC || (PAL && LSW=L))	＊＊＊＊＊＊＊＊	00H		W
D3H	(B-Y) burst level for NTSC (use at NTSC || (PAL && LSW=L))	＊＊＊＊＊＊＊＊	D6H		W
D4H	(R-Y) burst level for PAL (use at PAL && LSW=H)	＊＊＊＊＊＊＊＊	2AH		W
D5H	(B-Y) burst level for PAL (use at PAL && LSW=H)	＊＊＊＊＊＊＊＊	D6H		W
D6H	Rch/Bch high clip level (use at RGBmode Only)	＊＊＊＊＊＊＊＊	FFH		W
D7H	Gch high clip level (+300 hex)	＊＊＊＊＊＊＊＊	FFH		W
D8H	Gch low clip level (ref. = BLK level)	＊＊＊＊＊＊＊＊	2AH		W
D9H	Pedestal (ref. = BLK level)	＊＊＊＊＊＊＊＊	2AH		W
DAH	SYNC level LSB (ref. = BLK level)	―――＊＊＊＊＊	FFH		W
DBH	BLK level LSB (ref. = 00 hex)	―――＊＊＊＊＊	29H		W
DCH	SYNC level MSB (ref. = BLK level) BLK level MSB (ref. = 00 hex)	―――――――＊ ――――――＊―	02H		W W
DDH	VCO normal increment LSB (init value for 768 pixels/H NTSC)	＊＊＊＊＊＊＊＊	00H		W
DEH	VCO normal increment MSB (init value for 768 pixels/H NTSC)	＊＊＊＊＊＊＊＊	80H		W
DFH	LSB of corrective increment for each H of VCO (init value for 768 pixels/H NTSC)	＊＊＊＊＊＊＊＊	00H		W

ADR	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Reset Setting	R/W
E0H	MSB of increment for each H of VCO (init value for 768 pixels/H NTSC)	＊＊＊＊＊＊＊＊	80H		W
E1H	LSB of increment for each V of VCO (init value for 768 pixels/H NTSC)	＊＊＊＊＊＊＊＊	00H		W
E2H	MSB of increment for each V of VCO (init value for 768 pixels/H NTSC)	＊＊＊＊＊＊＊＊	80H		W
E3H	Gain adjustment for 10-bit DAC (0 to 255: GAIN = (x/64))	＊＊＊＊＊＊＊＊	B3H		W
E4H	YGGAIN 3200K center value LSB @wbcc (3200K YGGAIN reference value)	＊＊＊＊＊＊＊＊	00H		W
E5H	YMGAIN 3200K center value LSB @wbcc (3200K YMGAIN reference value)	＊＊＊＊＊＊＊＊	00H		W
E6H	YGGAIN 3200K center value MSB @wbcc YMGAIN 3200K center value MSB @wbcc (Not assigned)	――――――＊＊ ――――＊＊―― ＊＊＊＊―――――	0AH		W W
E7H	R-Y corrective gain (low color temperature) @wbcc (1x at 40H)	＊＊＊＊＊＊＊＊	40H		W
E8H	R-Y corrective gain (high color temperature) @wbcc (1x at 40H)	＊＊＊＊＊＊＊＊	40H		W
E9H	B-Y corrective gain (low color temperature) @wbcc (1x at 40H)	＊＊＊＊＊＊＊＊	40H		W
EAH	B-Y corrective gain (high color temperature) @wbcc (1x at 40H)	＊＊＊＊＊＊＊＊	40H		W
EBH	Center hysteresis part 1 @wbcc (Hysteresis valid at less than this value) Center hysteresis part 2 @wbcc (Threshold of valid hysteresis)	―――＊＊＊＊ ＊＊＊＊―――	31H		W W
ECH	Corrective gain limit @wbcc (Limit of the maximum color corrective gain)	＊＊＊＊＊＊＊＊	FFH		W
EDH	WBYGGAIN LSB @WBCC (READ data to be set in Address E4 on condition of 3200K)	＊＊＊＊＊＊＊＊			W
EEH	WBYMGAIN LSB @WBCC (READ data to be set in Address E5 on condition of 3200K)	＊＊＊＊＊＊＊＊			W
EFH	WBYGGAIN MSB @WBCC (READ data) WBYMGAIN MSB @WBCC (READ data) (To be set in Address E6 on condition of 3200K) (Not assigned)	――――――＊＊ ――――＊＊―― ＊＊＊＊―――			W W W

ADR	Data Descriptions		Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Reset Setting	R/W
F0H	When the data input PAD is occupied by another test in the test mode, signals can be sent into the circuit by using these registers.	EXTMOD	－－－－－－－＊	00H		W
		FLC	－－－－－－＊－			W
		NTPL	－－－－－＊－－			W
		CCDSEL0	－－－－＊－－－			W
		CCDSEL1	－－－＊－－－－			W
		CCDSEL2	－－＊－－－－－			W
		LLDET	－＊－－－－－－			W
		ALCELC	＊－－－－－－－			W
F1H	A/D sampling timing adjustment		－－－－＊＊＊＊	04H		W
	A/D clock phase adjustment (Adjustable from 0 to phase reverse)		－＊＊＊－－－－			W
F2H	When the data input PAD is occupied by another test in the test mode, signals can be sent into the circuit by using these registers.	ATWLOCK	－－－－－－－＊	00H		W
		APGAIN	－－－－－－＊－			W
		BLCSW	－－－－－＊－－			W
		REV	－－－－＊－－－			W
		(Not assigned)	＊＊＊＊－－－－			W
F3H	Ramp waveform start position @rampgen		＊＊＊＊＊＊＊＊	00H		W
F4H	Ramp waveform gain adjustment @rampgen (1x at 80H)		＊＊＊＊＊＊＊＊	80H		W
F5H	Ramp waveform max. value LSB @rampgen		＊＊＊＊＊＊＊＊	FFH		W
F6H	Ramp waveform max. value MSB @rampgen		－－－－－－－＊	01H		W
F7H	Color bar start position @patgen		＊＊＊＊＊＊＊＊	7EH		W
F8H	Color bar width @patgen		＊＊＊＊＊＊＊＊	80H		W
F9H	Color bar H/V switching @patgen (0: Horizontal 1: Vertical)		－－－－－－－＊	00H		W
	Color bar phase adjustment @patgen		－－－－－－＊－			W
	(Not assigned)		－－－－＊＊－－			
	CDS/AGC/AD cell test mode 1 ADCKREG 0: Normal 1: CDS/AGC power down		－－－＊－－－－			W
	CDS/AGC/AD cell test mode 3, mode 2 00: Normal 01: CDS/AGC, AD isolation mode 10: AGC DAC output (VAGCOUT pin) 11: OB DAC output (VAGCOUT pin)		－＊＊－－－－－			W
	(Not assigned)		＊－－－－－－－			
FAH	(Not assigned)		－－－－＊＊＊＊	10H		
	I2C high-speed R/W ON/OFF switching (in test mode) (0: I2C normal operation 1: I2C high-speed R/W (in test mode))		－－－＊－－－－			W
	BLCSW/DS1 switching (0: BLCSW input 1: DS1 output)		－－＊－－－－－			W
	REV/DS2 switching (Valid for other than TM3 and TM29) (0: REV input 1: DS2 output)		－＊－－－－－－			W
	(Not assigned)		＊－－－－－－－			
FBH	NHRST phase switching @plsgen		＊＊＊＊＊＊＊＊	46H		W
FCH	PWM2@pwm		＊＊＊＊＊＊＊＊	00H		W
FDH	PWM3@pwm		＊＊＊＊＊＊＊＊	00H		W

EEPROM address	Data Descriptions	Data Configuration 7 6 5 4 3 2 1 0	Standard Setting	Adjustable Range	R/W
FEH	RGB signal/YC signal switching * To be used for TM19 and TM28 1: R → RGBTO, YCTSEL(TM19, TM28) 1: G → RGBTO, YCTSEL(TM19, TM28) 1: B → RGBTO, YCTSEL(TM19, TM28) 1: YC → ALC →YCTSEL(TM28), RGBTO=0 1: YC → AWB →YCTSEL(TM28), RGBTO=0 1: YC → ENC →YCTSEL(TM28), RGBTO=0 1: YOUT → TCTSEL(TM28), RGBTO=0 1: COUT → YCTSEL(TM28), RGBTO=0 (Not assigned)	 *------- -*------ --*----- ---*---- ----*--- -----*-- ------*- -------* -------*	00H		W W W W W W W W
FFH	Slave address register @i2c (Slave address setting of this LSI (Write only)) (Not assigned)	-******* *-------	2AH		W

[Supplementary remarks]

Registers of the ENC block should be set as shown below according to the CCD mode because "***fH" and the number of pixels vary with the mode.

VCO register setting

[510NTSC:MN39110]606fH
VCOC[15:0]=C036H
VCOH[15:0]=C08EH
VCOV[15:0]=C08EH

[510PAL:MN39210]618fH
VCOC[15:0]=EB15H
VCOH[15:0]=EB54H
VCOV[15:0]=EC61H

[510PAL:MN39217] 605fH
VCOC[15:0]=F001H
VCOH[15:0]=EE94H
VCOV[15:0]=EFA1H

[768NTSC] 910fH
VCOC[15:0]=8000H
VCOH[15:0]=8000H
VCOV[15:0]=8000H

[768PAL] 908fH
VCOC[15:0]=A000H
VCOH[15:0]=A1A3H
VCOV[15:0]=A2B0H

According to the above settings, the registers of the addresses (DD, DE, DF, E0, E1, and E2) should be set as follows:

*510H	NTSC(39110)	NTSC="L",	DD=36h,	DE=C0h,	DF=8Eh,	E0=C0h,	E1=8Eh,	E2=C0h
*510H	PAL (39210)	NTPL="H",	DD=15h,	DE=EBh,	DF=54h,	E0=EBh,	E1=61h,	E2=ECh
*510H	PAL (39213)	NTPL="H",	DD=BDh,	DE=EFh,	DF=94h,	E0=EEh,	E1=A1h,	E2=EFh
*768H	NTSC	NTPL="L",	DD=00h,	DE=80h,	DF=00h,	E0=80h,	E1=00h,	E2=80h
*768H	PAL	NTPL="H",	DD=00h,	DE=A0h,	DF=A3h,	E0=A1h,	E1=B0h,	E2=A2h

7.1 Supplementary descriptions of the CG/SSG registers

Register C0	********	CGSW0	High-speed pulse phase setting
Register C1	********	CGSW1	High-speed pulse phase setting
Register C2	********	CGSW2	High-speed pulse phase setting
Register C3	********	CGSW3	High-speed pulse phase setting
Register C4	------**	CGSW4	High-speed pulse phase setting

CGSW0								Setting operation		
7	6	5	4	3	2	1	0	Adjusting signal	Operation	
*	*	*	*	*	*	L	L	H1, H2	-1/2T DLY	Coarse adjustment
*	*	*	*	*	*	L	H		-1/4T DLY	
*	*	*	*	*	*	H	L		0T DLY	
*	*	*	*	*	*	H	H		1/4 DLY	
*	*	*	L	L	L	*	*		0DLY	Fine adjustment
*	*	*	L	L	H	*	*		1DLY	
*	*	*	L	H	L	*	*		2DLY	
*	*	*	L	H	H	*	*		3DLY	
*	*	*	H	L	L	*	*		4DLY	
*	*	*	H	L	H	*	*		5DLY	
*	*	*	H	H	L	*	*		6DLY	
*	*	*	H	H	H	*	*		7DLY	
*	*	L	*	*	*	*	*	FCK(H1, H2)	Through	
*	*	H	*	*	*	*	*		Reverse	
*	L	*	*	*	*	*	*	H1, H2	Through	Output
*	H	*	*	*	*	*	*		Reverse	
L	*	*	*	*	*	*	*	R	Through	Output
H	*	*	*	*	*	*	*		Reverse	

CGSW1								Setting operation		
7	6	5	4	3	2	1	0	Adjusting signal	Operation	
*	*	*	*	*	*	L	L	R	-1/2 T DLY	Coarse adjustment
*	*	*	*	*	*	L	H		-1/4 T DLY	
*	*	*	*	*	*	H	L		0T DLY	
*	*	*	*	*	*	H	H		1/4 DLY	
*	*	*	L	L	L	*	*		0DLY	Fine adjustment
*	*	*	L	L	H	*	*		1DLY	
*	*	*	L	H	L	*	*		2DLY	
*	*	*	L	H	H	*	*		3DLY	
*	*	*	H	L	L	*	*		4DLY	
*	*	*	H	L	H	*	*		5DLY	
*	*	*	H	H	L	*	*		6DLY	
*	*	*	H	H	H	*	*		7DLY	
*	*	L	*	*	*	*	*	FCK(R)	Through	
*	*	H	*	*	*	*	*		Reverse	
L	L	*	*	*	*	*	*	R	1/4FCK	Pulse width
L	H	*	*	*	*	*	*		20 ns	
H	L	*	*	*	*	*	*		15 ns	
H	H	*	*	*	*	*	*		10 ns	

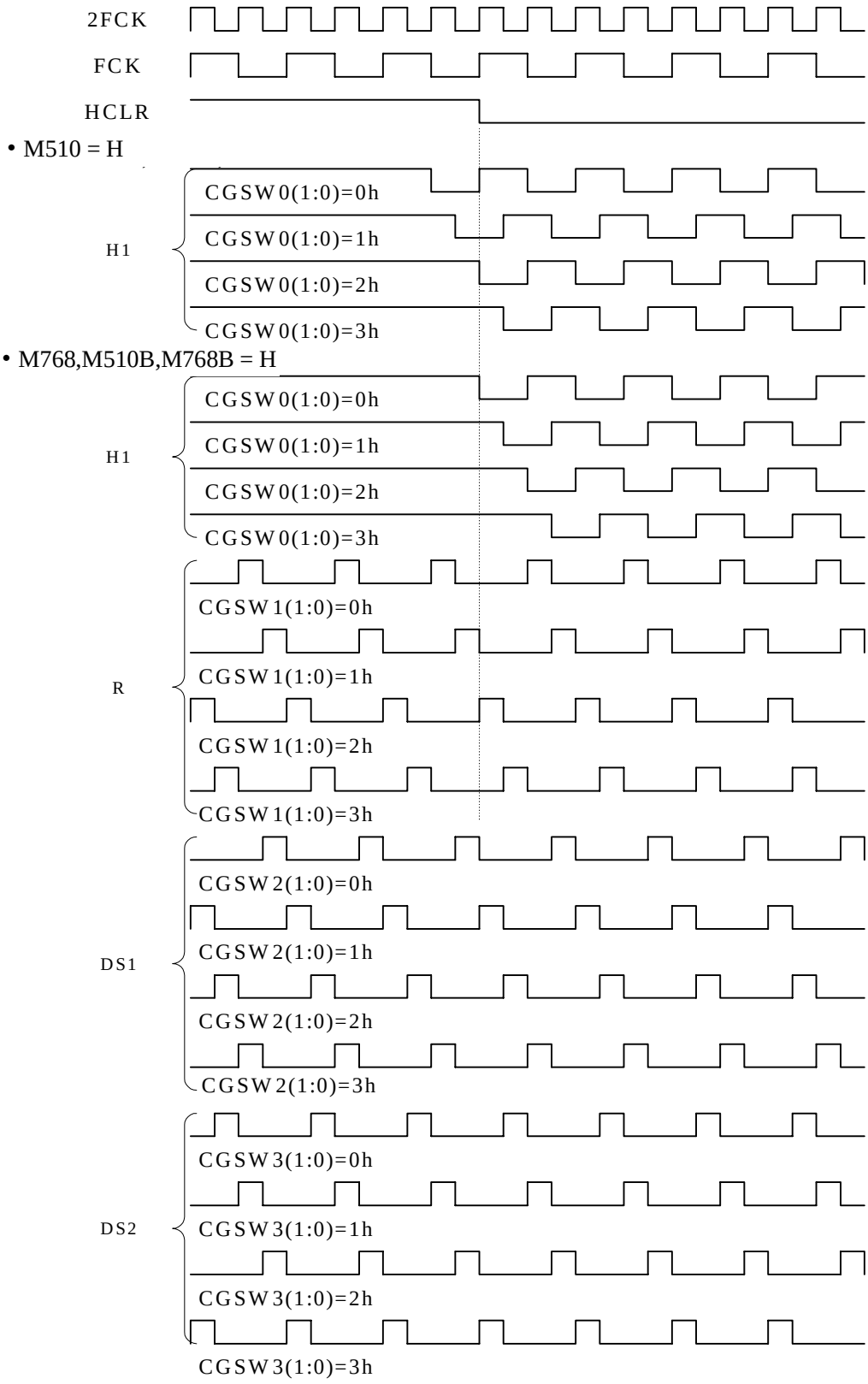
CGSW2								Setting operation		
7	6	5	4	3	2	1	0	Adjusting signal	Operation	
*	*	*	*	*	*	L	L	DS1	-1/2 T DLY	Coarse adjustment
*	*	*	*	*	*	L	H		-1/4 T DLY	
*	*	*	*	*	*	H	L		0T DLY	
*	*	*	*	*	*	H	H		1/4 DLY	
*	*	*	L	L	L	*	*		0CELL DLY	Fine adjustment
*	*	*	L	L	H	*	*		1CELL DLY	
*	*	*	L	H	L	*	*		2CELL DLY	
*	*	*	L	H	H	*	*		3CELL DLY	
*	*	*	H	L	L	*	*		4CELL DLY	
*	*	*	H	L	H	*	*		5CELL DLY	
*	*	*	H	H	L	*	*		6CELL DLY	
*	*	*	H	H	H	*	*		7CELL DLY	
*	*	L	*	*	*	*	*	FCK(DS1)	Through	
*	*	H	*	*	*	*	*		Reverse	
L	*	*	*	*	*	*	*	DS1, DS2	1/4FCK	Pulse width
H	L	*	*	*	*	*	*		1/4FCK-5 ns	
H	H	*	*	*	*	*	*		1/4FCK-10 ns	

CGSW3								Setting operation		
7	6	5	4	3	2	1	0	Adjusting signal	Operation	
*	*	*	*	*	*	L	L	DS2	-1/2 T DLY	Coarse adjustment
*	*	*	*	*	*	L	H		-1/4 T DLY	
*	*	*	*	*	*	H	L		0T DLY	
*	*	*	*	*	*	H	H		1/4 DLY	
*	*	*	L	L	L	*	*		0CELL DLY	Fine adjustment
*	*	*	L	L	H	*	*		1CELL DLY	
*	*	*	L	H	L	*	*		2CELL DLY	
*	*	*	L	H	H	*	*		3CELL DLY	
*	*	*	H	L	L	*	*		4CELL DLY	
*	*	*	H	L	H	*	*		5CELL DLY	
*	*	*	H	H	L	*	*		6CELL DLY	
*	*	*	H	H	H	*	*		7CELL DLY	
*	*	L	*	*	*	*	*	FCK(DS2)	Reverse	
*	*	H	*	*	*	*	*		Through	
*	L	*	*	*	*	*	*	DS2	Through	
*	H	*	*	*	*	*	*		DS2=DS1	
L	*	*	*	*	*	*	*	DS1, DS2	Through	Output
H	*	*	*	*	*	*	*		Reverse	

CGSW4								Setting operation		
7	6	5	4	3	2	1	0	Adjusting signal	Operation	
*	*	*	*	*	*	*	L	DS1	0 ns DLY	
*	*	*	*	*	*	*	H		2.6 ns DLY	
*	*	*	*	*	*	L	*	DS2	0 ns DLY	
*	*	*	*	*	*	H	*		2.6 ns DLY	

These registers allow the phase adjustment for H1, H2, R, DS1 and DS2. However, some CCDs require initial settings.

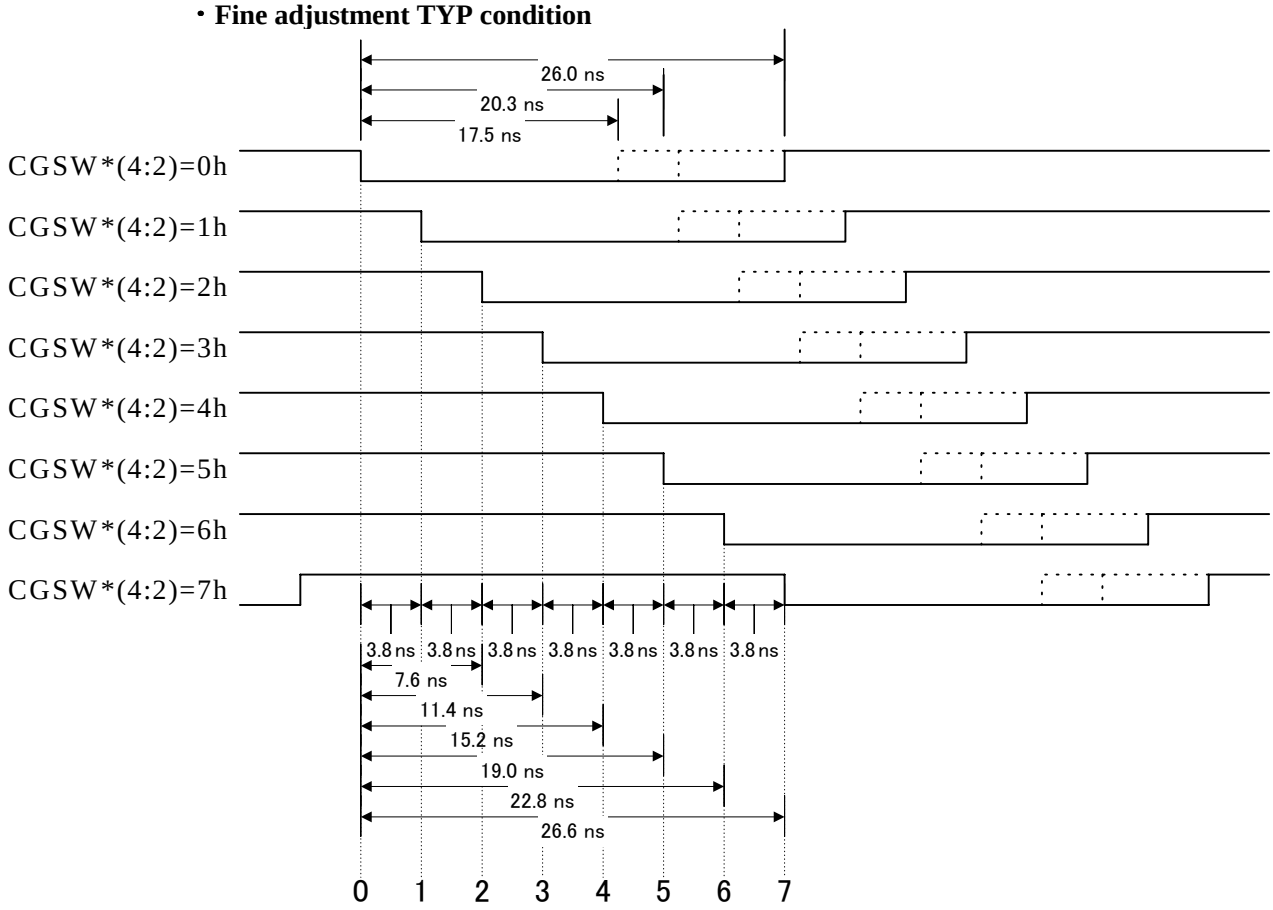
Coarse adjustment



* H2 has a waveform with a reversed polarization of H1.

Fine adjustment

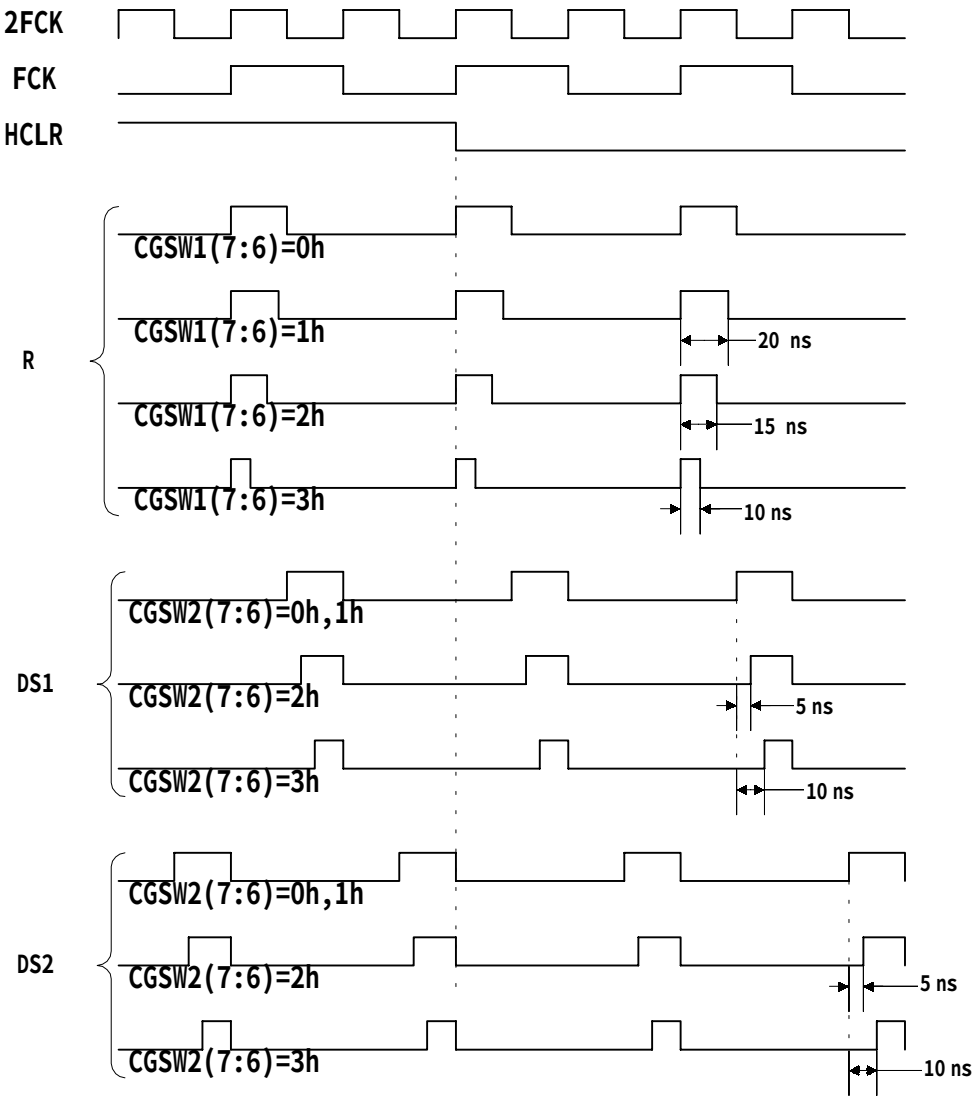
・**Fine adjustment TYP condition**



SW			Select DLY	DLY time [ns]		
2	1	0		MIN	TYP	MAX
L	L	L	0unit DELAYCELL	0	0	0
L	L	H	1unit DELAYCELL	1.9	3.8	7.6
L	H	L	2unit DELAYCELL	3.8	7.6	15.2
L	H	H	3unit DELAYCELL	5.7	11.4	22.8
H	L	L	4unit DELAYCELL	7.6	15.2	30.4
H	L	H	5unit DELAYCELL	9.5	19.0	38.0
H	H	L	6unit DELAYCELL	11.4	22.8	45.6
H	H	H	7unit DELAYCELL	13.3	26.6	53.2

3.8-ns DLY cell is used for one unit.

Width adjustment



CPOB phase switching

Register CB	---*****	CPST	CPOB start set value	(0T-31T)
Register CC	---*****	CPSP	CPOB stop set value	(0T-31T)
Register CD	---*****	CPST2	CPOB2 start set value	(0T-31T)
Register CE	---*****	CPST2	CPOB2 stop set value	(0T-31T)

External/internal TG switch

Register C4 *------- TGOE TG output enable signal

Setting	Description
0	Internal TG connected
1	External TG used

By setting this register to “1”, H1, H2 and R of the internal TG can be stopped when using the externally connected TG.

Flicker setting

Register C5 ------** MODE1, 2 Normal/flickerless/electronic aperture switching

MODE		Description
1	2	
0	∗	Normal: (NTSC) 1/60 s, (PAL) 1/50 s
1	0	Flickerless: (NTSC) 1/100 s, (PAL) 1/120 s
1	1	Electronic aperture: 1/60s (1/50s) to 1/100000s max.

Register C5 -----*-- CHREV	CH1 and CH2 pulse reversing process
Register C5 ----*--- SUBREV	SUB pulse reversing process
Register C5 ---*---- V1REV	V1 pulse reversing process
Register C5 --*----- V2REV	V2 pulse reversing process
Register C5 -*------ V3REV	V3 pulse reversing process
Register C5 *------- V4REV	V4 pulse reversing process

Setting	Description
0	Normal state (normal)
1	Pulse reversed

If it’s required to reverse some pulses depending on the CCD used, then set this register. By setting this register to “1”, the polarity of the pulses are reversed.

Register C6 -----***	RHSSOS	Register for setting HSSOS
Register C6 ****----	RHSSO	Register for setting HSSO (lower bits)
Register C7 --******	RHSSO	Register for setting HSSO (upper bits)

Setting the register HSSEL to “H” in testing allows this register to set HSSOS or HSSO.

・ HSSEL HSSOS, HSSO register setting switching

Register C7 * ------- HSSEL HSSOS, HSSO register setting switching

Setting	Description
0	Internal connection (normal)
1	Register setting (testing)

Setting this register to “1” allows HSSOS and HSSO to be set from the register.

・ FD FHRST delay time switching

Register C8 ---***** FD FHRST delay time switching

Setting	Description
00	FHRST delay time (MIN)
1F	FHRST delay time (MAX)

This register can set FHRST in accordance with the delay time on the main line. The standard delay time is set to 10h.

・ LLSEL LLDET system switching

Register C8 --*----- LLSEL LLDET system switching

Setting	Description
0	Conventional system
1	Simplified system

Setting this register to “1” can generate pulses with a simple processing not with the conventional complex pre-processing. (Test circuit to study the system).

・ VDSEL VD select signal

Register C8 -*------ VDSEL VD select signal

Setting	Description
0	Outputs CSYNC
1	Outputs VD

The CSYNC/VD output pin normally outputs CSYNC. Setting this register to “1” outputs to VD.

・ INT Processing when VCO is not required

Register C8 *------- INT Processing when VCO is not required

Setting	Description
0	With VCO
1	Without VCO

Setting this register to “1” forces the crystal oscillation mode to be operated irrespective of the availability of the external synchronization.

Register C9	********	HP	H phase fine adjustment when SYNC is synchronized
Register CA	********	HP2	H phase fine adjustment when HDVD is synchronized

Setting	Description
00	H phase adjustment for HDVD/SYNC synchronized (MIN)
FF	H phase adjustment for HDVD/SYNC synchronized (MAX)

The external SYNC signal is separated by the SYNC separation circuit. Since this causes a delay, correction is carried out before the signal is applied to the phase comparator. For adjustments, 80h is defined as standard.

- External Pin LLDET LL synchronized switching input

Setting	Description
0	LL synchronization OFF
1	LL synchronization ON

By setting this register, the drive signal corresponding to each mode is output. The MODE shown here is the CCD select signal output to be used by TG.

- External Pin NP NTSC/PAL switching pin

Setting	Description
0	NTSC system
1	PAL system

This pin allows the color TV system, NTSC or PAL, to be switched.

- External Pin REV/DS2 left-right reverse switching pin
  (Register switching, REV as default)

Setting	Description
0	Normal
1	Reversed

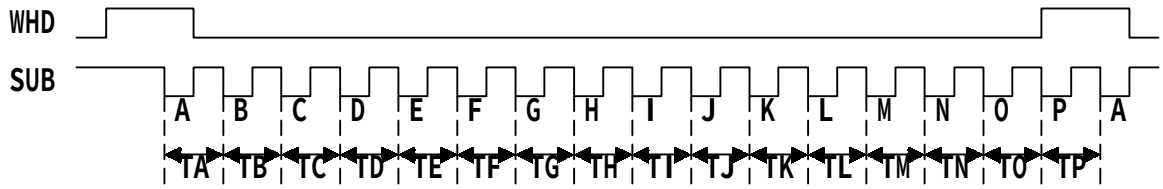
This pin allows the picture to be reversed left-right. However, this pin can be switched, using the F2 register, to the function of monitoring the DS2 output by the internal register. The REV input is default setting.

・ External pin CCDSEL0 – 2 CCD switching pin

Setting				MODE	Description
CCDSEL			NP		
2	1	0			
0	0	0	0	M510	510 pixels MN39110 series, MN39116 (NTSC)
			1		510 pixels MN39210 series, MN39216 (PAL)
0	0	1	0	———	
			1		
0	1	0	0	M768	768 pixels MN39143 (NTSC) 1/3 type
			1		768 pixels MN39243 (PAL) 1/3 type
0	1	1	0	M510B	510 pixels (NTSC)
			1		510 pixels (PAL)
1	0	0	0	M768B	768 pixels (NTSC)
			1		768 pixels (PAL)

By setting this register, the drive signal corresponding to each mode is output.
The MODE shown here is the CCD select signal output to be used by TG.

Internal connection	----****	HSSO0-3	Electronic shutter setting (SUB pulse)
Internal connection	********	HSSOS0-7	Electronic shutter setting (SUB pulse)
Internal connection	-------*	HSSOS8-9	Electronic shutter setting (SUB pulse)



SUB position	Data setting						Timing					Remarks
	HSH(8:0)	HSL3	HSL2	HSL1	HSL0		606fh	618fh	780fh	910fh	908fh	
A	*	0	0	0	0	TA	38T	39T	49T	57T	57T	VBLK period
B	*	0	0	0	1	TB	38T	39T	49T	57T	57T	
C	*	0	0	1	0	TC	38T	39T	49T	57T	57T	
D	*	0	0	1	1	TD	38T	38T	48T	57T	56T	
E	*	0	1	0	0	TE	38T	39T	49T	57T	57T	
F	*	0	1	0	1	TF	38T	38T	49T	57T	57T	
G	*	0	1	1	0	TG	38T	39T	49T	57T	57T	
H	*	0	1	1	1	TH	37T	38T	48T	56T	56T	
I	*	1	0	0	0	TI	38T	39T	49T	57T	57T	
J	*	1	0	0	1	TJ	38T	39T	49T	57T	57T	
K	*	1	0	1	0	TK	38T	39T	49T	57T	57T	
L	*	1	0	1	1	TL	38T	38T	48T	57T	56T	
M	*	1	1	0	0	TM	38T	39T	49T	57T	57T	
N	*	1	1	0	1	TN	38T	38T	49T	57T	57T	
O	*	1	1	1	0	TO	38T	39T	49T	57T	57T	
P	*	1	1	1	1	TP	37T	38T	48T	56T	56T	

Electric charge accumulation time is as follows.

NTSC: (261 - HSH(8:0))H (where $0 < n \leq 260$)

For n=0, 262 or 263H

PAL: (311 - HSH(8:0))H (where $0 < n \leq 310$)

For n=0, 312 or 313H

8. Pin Descriptions

Pin No.	Pin name	I/O	Description
1	CDSOUT	O	CDS output (for control of ALC lens)
2	VOBDAT	O	Output OB level stabilization pin Grounded via C.
3	AGCOUT	O	AGC output
4	AGCVSS	VSS	Ground for AGC block
5	VCLDAT	O	Input DC level stabilization pin Grounded via C.
6	AGCVDD	VDD	AGC block power supply 3.0 V
7	CDSVDD	VDD	CDS block power supply 3.0 V
8	VFSIG	I	CDS IN
9	VSSIG	I	CDS IN
10	CDSVSS	VSS	Ground for CDS block
11	REV/DS2	I	Left-right reverse switching, H: reversed, L: normal / CDS sampling pulse output (register switching, REV as default)
12	BLCSW/DS1	I	BLC switch, L: OFF, H: ON / CDS sampling pulse output (register switching, BLCSW as default)
13	CH1	O	Electric charge read pulse for V1
14	CH2	O	Electric charge read pulse for V3
15	SUB	O	Reset pulse output for the electronic shutter board
16	VDD1	VDD	Logic block power supply 1 2.0 V
17	VSS1	VSS	Ground for logic block, I/O block
18	VDDIO1	VDD	I/O block power supply 1 3.3 V
19	SDA	I/O	Serial data
20	SCL	I/O	Serial clock
21	COIN	I	Oscillation input (LC)
22	NTPL	I	NTSC/PAL switch, L: NTSC, H: PAL
23	CCDSEL0	I	CCD select
24	CCDSEL1	I	CCD select
25	CCDSEL2	I	CCD select
26	TGVDD	VDD	TG logic block power supply 2.0 V
27	TGIOVSS	VSS	Ground for I/O block, logic block of TG
28	RR	O	Reset pulse output
29	TGIOVDD	VDD	Power supply 3.3 V for I/O block of TG
30	H2	O	ϕ H2 horizontal register transfer clock
31	H1	O	ϕ H1 horizontal register transfer clock
32	OSCCNT	O	LC oscillation control Hi-Z in the LL mode or Low-Z, otherwise
33	CXIN	I	Oscillation input
34	CXOUT	O	Oscillation output
35	OSCVDD	VDD	Oscillation block power supply 3.3 V
36	OSCVSS	VSS	Ground for oscillation block

Pin No.	Pin name	I/O	Description
37	TEST0	I	Test mode setting (Normally, use at Low setting.)
38	TEST1	I	Test mode setting (Normally, use at Low setting.)
39	TEST2	I	Test mode setting (Normally, use at Low setting.)
40	TEST3	I	Test mode setting (Normally, use at Low setting.)
41	TEST4	I	Test mode setting (Normally, use at Low setting.)
42	V1	O	ϕ V1 vertical register transfer clock
43	V2	O	ϕ V2 vertical register transfer clock
44	V3	O	ϕ V3 vertical register transfer clock
45	V4	O	ϕ V4 vertical register transfer clock
46	VDDIO2	VDD	I/O block power supply 2 3.3 V
47	VSS2	VSS	Ground for logic block, I/O block
48	VDD2	VDD	Logic block power supply 2 2.0 V
49	FWHD	O	FWHD output
50	CPOB/HCLR /FVD/CPOB2	O	CPOB/HCLR/FVD/CPOB2 output (register switching, CPOB as default)
51	PBLK/CBLK /WHD	O	PBLK/CBLK/WHD output (register switching, PBLK as default)
52	CSYNC	O	CSYNC output
53	EXTMOD	I	Monitor/vehicle mounting mode switch, L: monitor, H: vehicle mounting
54	FLC	I	Flickerless mode (gain correction), L: OFF, H: ON
55	EXTIN0	I	External synchronization input pin, monitor mode: LP, vehicle mounting mode: CSYNC/HD
56	EXTIN1	I	External synchronization input pin, monitor mode: VD2, vehicle mounting mode: VD
57	LLDET	I	INT/LL switch, L: INT synchronization, H: LL synchronization
58	ALCELC	I	ALC/ELC switch, L: ELC, H: ALC
59	APGAIN	I	AP gain switch, L: sharp, H: soft (APGAIN = 0)
60	ATWLOCK	I	ATW lock, L: normal operation, H: lock
61	SCANT	I	Scanning test (Normally, use at Low setting.)
62	MINTEST	I	MINTEST (Normally, use at Low setting.)
63	VDDIO3	VDD	I/O block power supply 3 3.3 V
64	VOUT2		Regulator output pin outputting 2.0 V
65	VSS3	VSS	Ground for logic block, I/O block
66	VDD3	VDD	Logic block power supply 3 2.0 V
67	RESET	I	Power-ON reset input
68	PWM0	O	PWM output, ch 0
69	PWM1	O	PWM output, ch 1
70	PWM2	O	PWM output, ch 2
71	PWM3/FCK O/F2CKO	O	PWM output, ch 3/FCKO/F2CKO output (register switching, PWM as default)
72	PCO1	O	Phase comparator output (for crystal oscillation)
73	PCO2	O	Phase comparator output (for LC oscillation)
74	AREAPULS	O	BLC frame pulse output
75	IRIS	O	ALC DC control

Pin No.	Pin name	I/O	Description
76	VCXO	O	Analog SW output
77	FVR	I	VCXO control voltage input (analog SW input, DC input for frequency adjustment for INT or LL)
78	LPFI	I	VCXO control voltage input (analog SW input, monitor: V LPF, vehicle mounting: H LPF)
79	RSIG	O	R output
80	DAVDD2	VDD	DA23 power supply 3.0 V
81	DAVSS2	VSS	Ground for DA23
82	BSIG	O	C/B output
83	COMP23	I	Pin for phase correction Connects C across DAVDD2
84	IREF23	I	Resistor pin for setting bias current
85	VREF23	I	Reference voltage input pin
86	DAVDD1	VDD	DA1 power supply 3.0 V
87	DAVSS1	VSS	Ground for DA1
88	GSIG	O	Composite/Y/G output
89	COMP1	I	Pin for phase correction Connects C across DAVDD1
90	IREF1	I	Resistance pin for setting bias current
91	VREF1	I	Reference voltage input pin
92	VREFH	I	AD reference power supply VRT input
93	VREFM	I	AD reference power supply VRM input
94	VREFL	I	AD reference power supply VRB input
95	TADIN	I	AD Input
96	ADVSS	VSS	Ground for AD
97	ADVDD	VDD	AD power supply 2.0 V
98	VREFLO	O	AD reference power supply VRB output
99	VREFHO	O	AD reference power supply VRT output
100	CDSDAT	O	OB & AGC control DAC output (VDACOB, VDACGAIN)

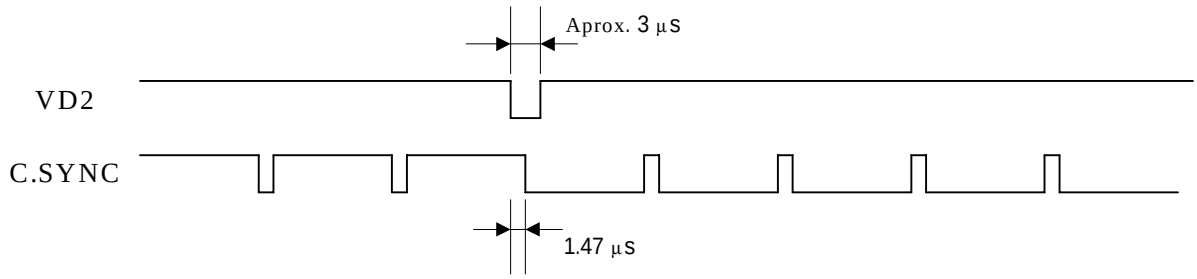
9. Pin Assignment

Please refer to the evaluation board circuit diagram.

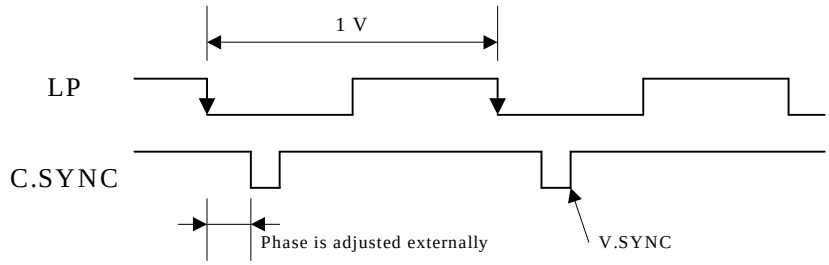
Figure 2 Pin assignment

10. Timing Chart

- VD2 synchronization



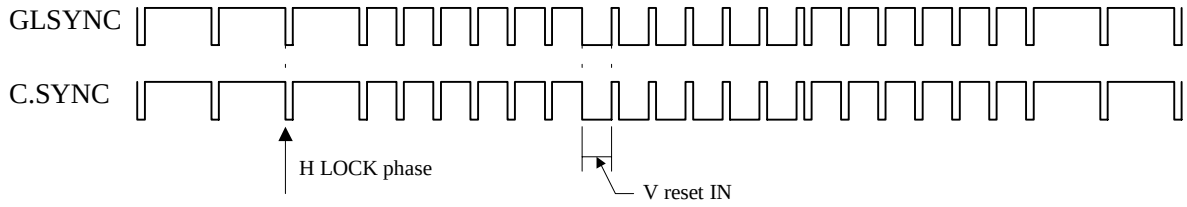
- LL synchronization (power supply synchronization)



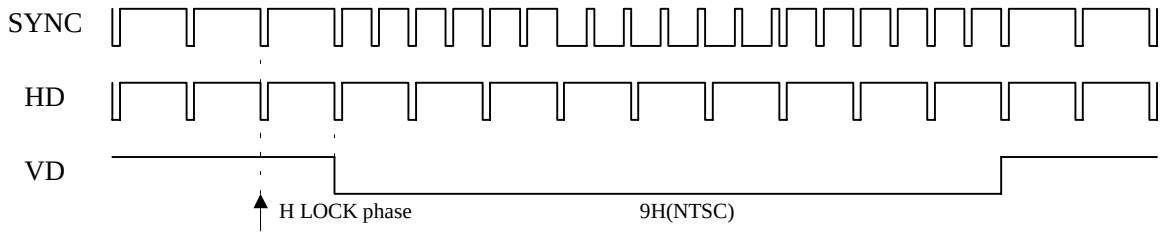
EIA 60 Hz Duty Approx. 50%
CCIR 50 Hz Duty Approx. 50%
The falling edge is reference edge.

Phase is adjusted externally by mono-multi type.

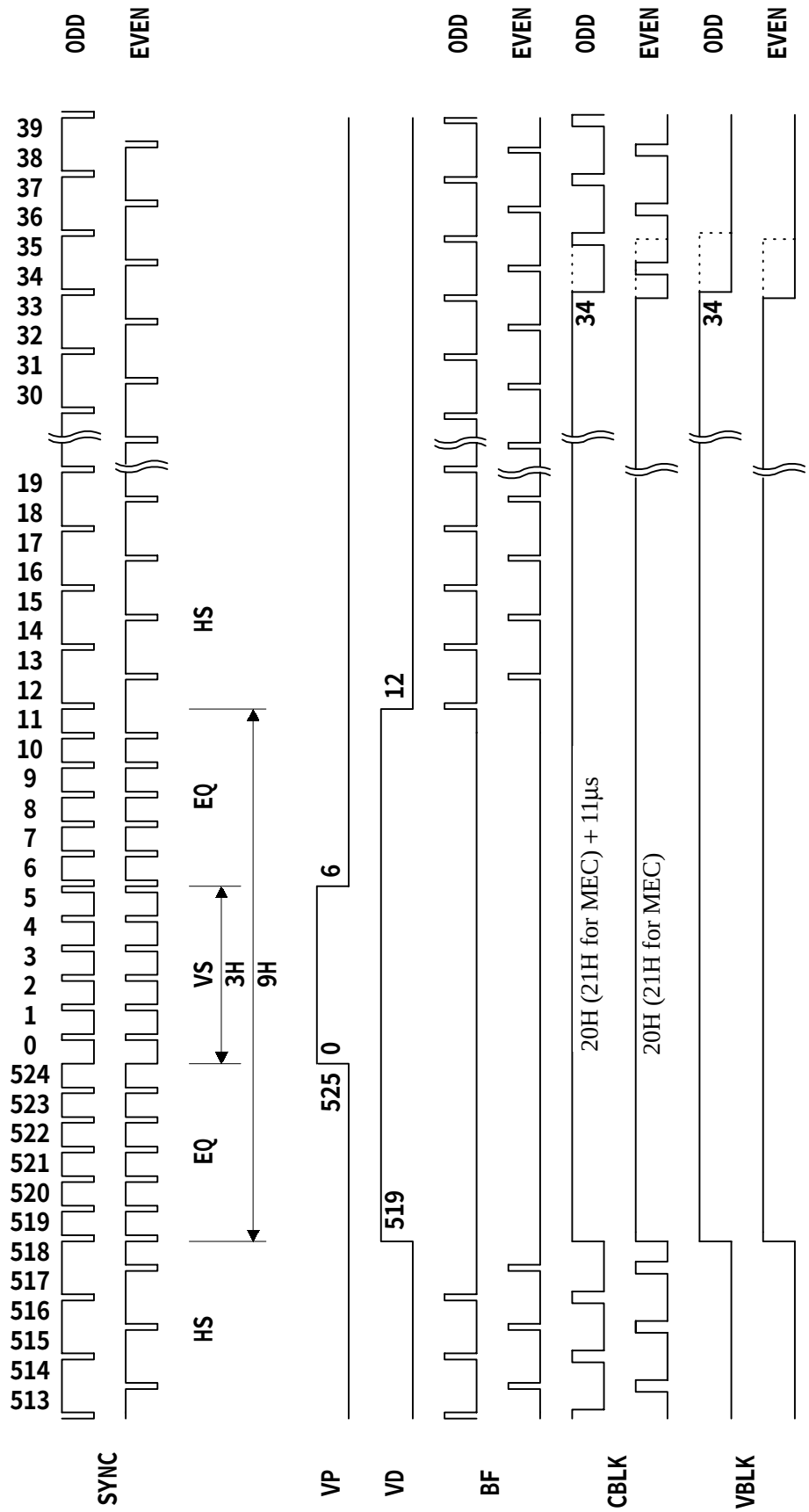
- SYNC synchronization



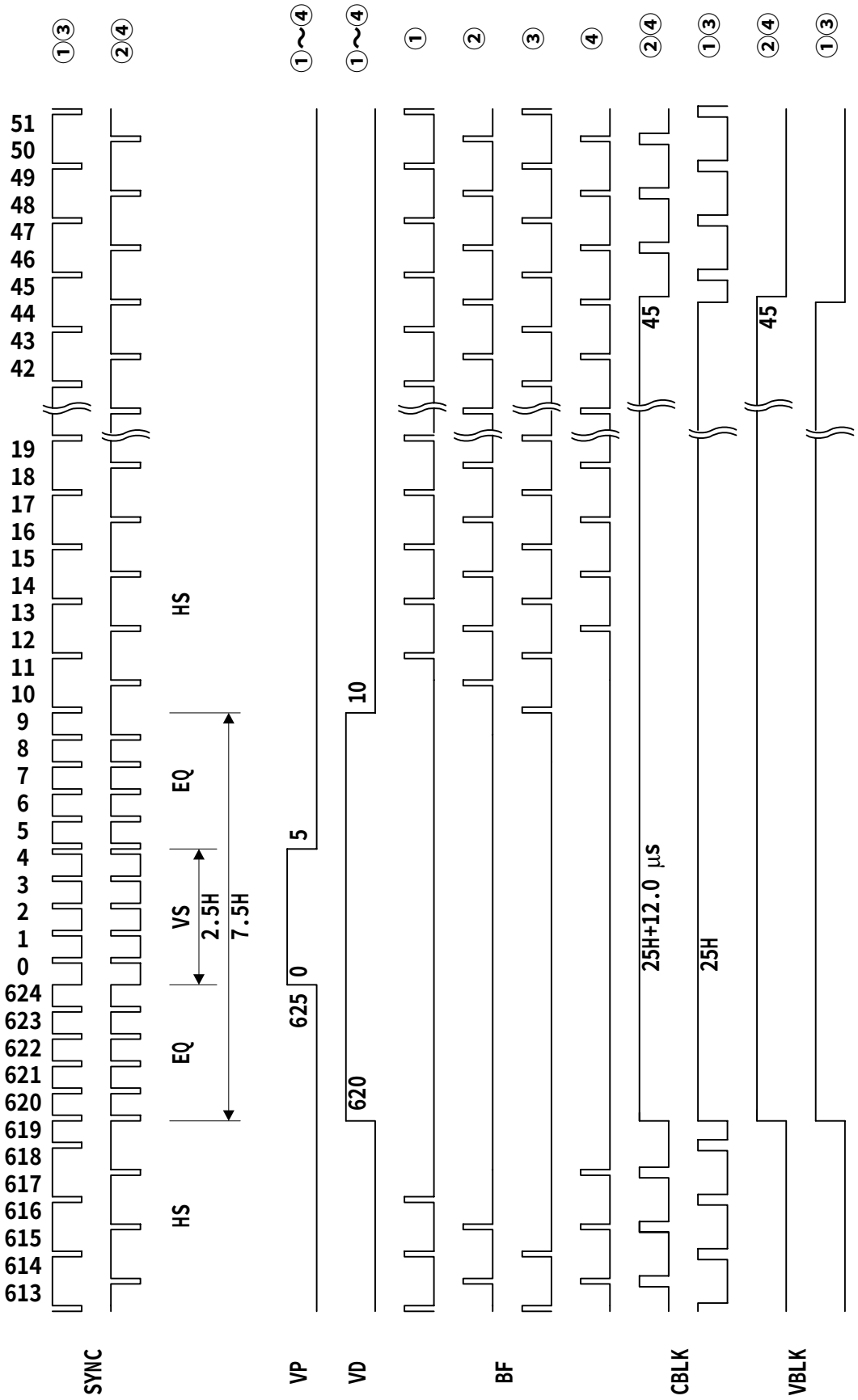
- HDVD synchronization



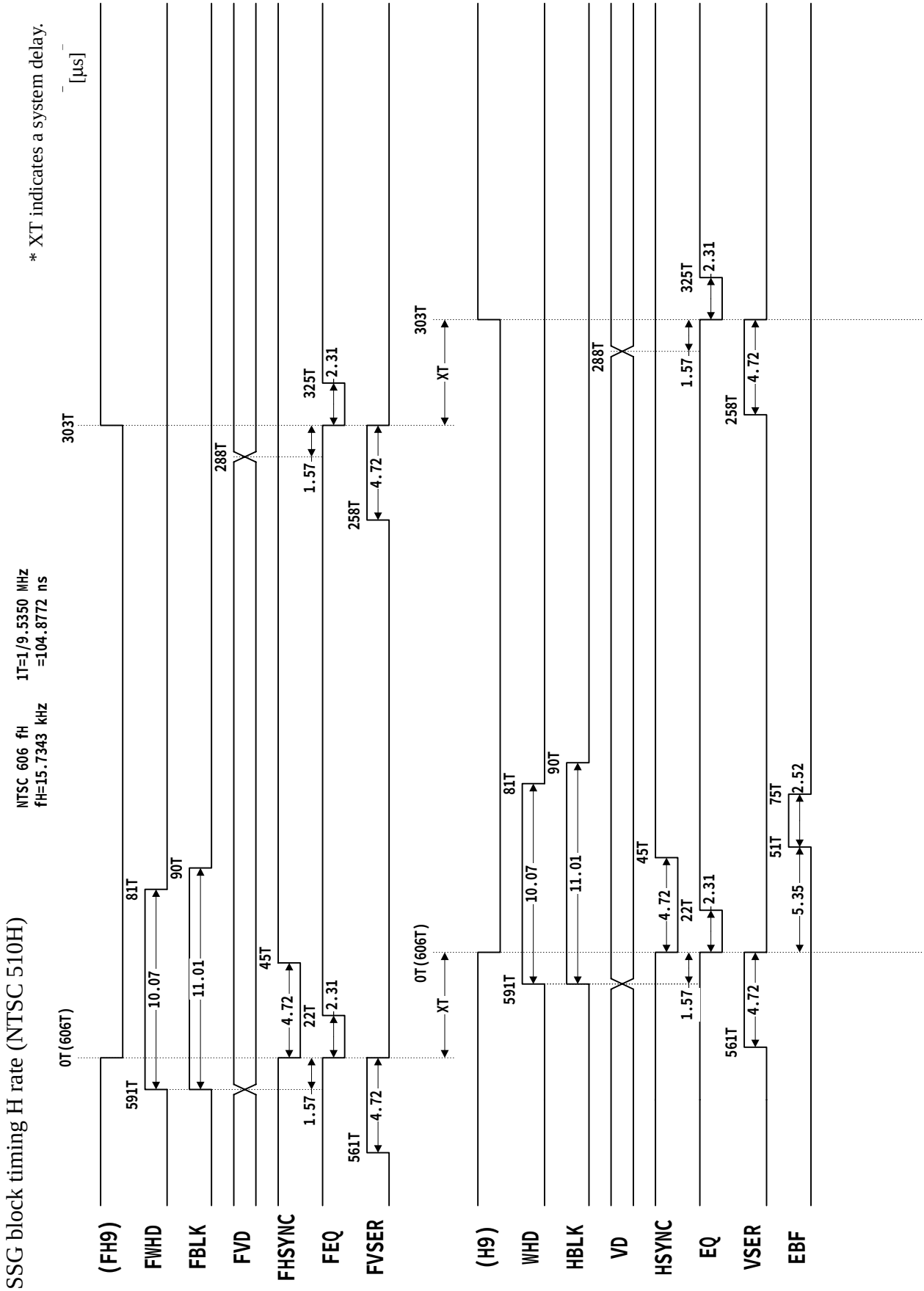
SSG block timing V rate (NTSC)



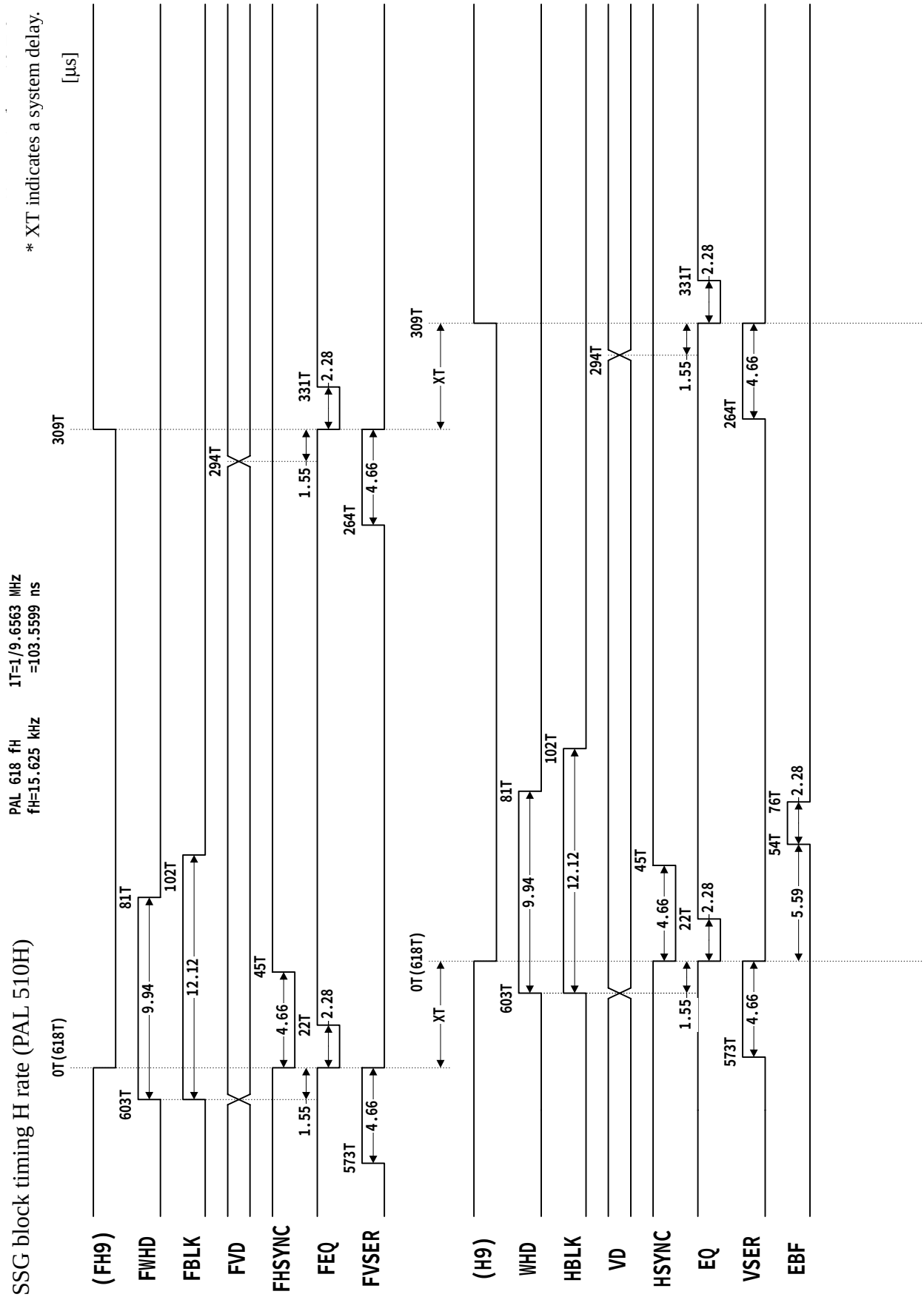
SSG block timing V rate (PAL)



SSG block timing H rate (NTSC 510H)



SSG block timing H rate (PAL 510H)



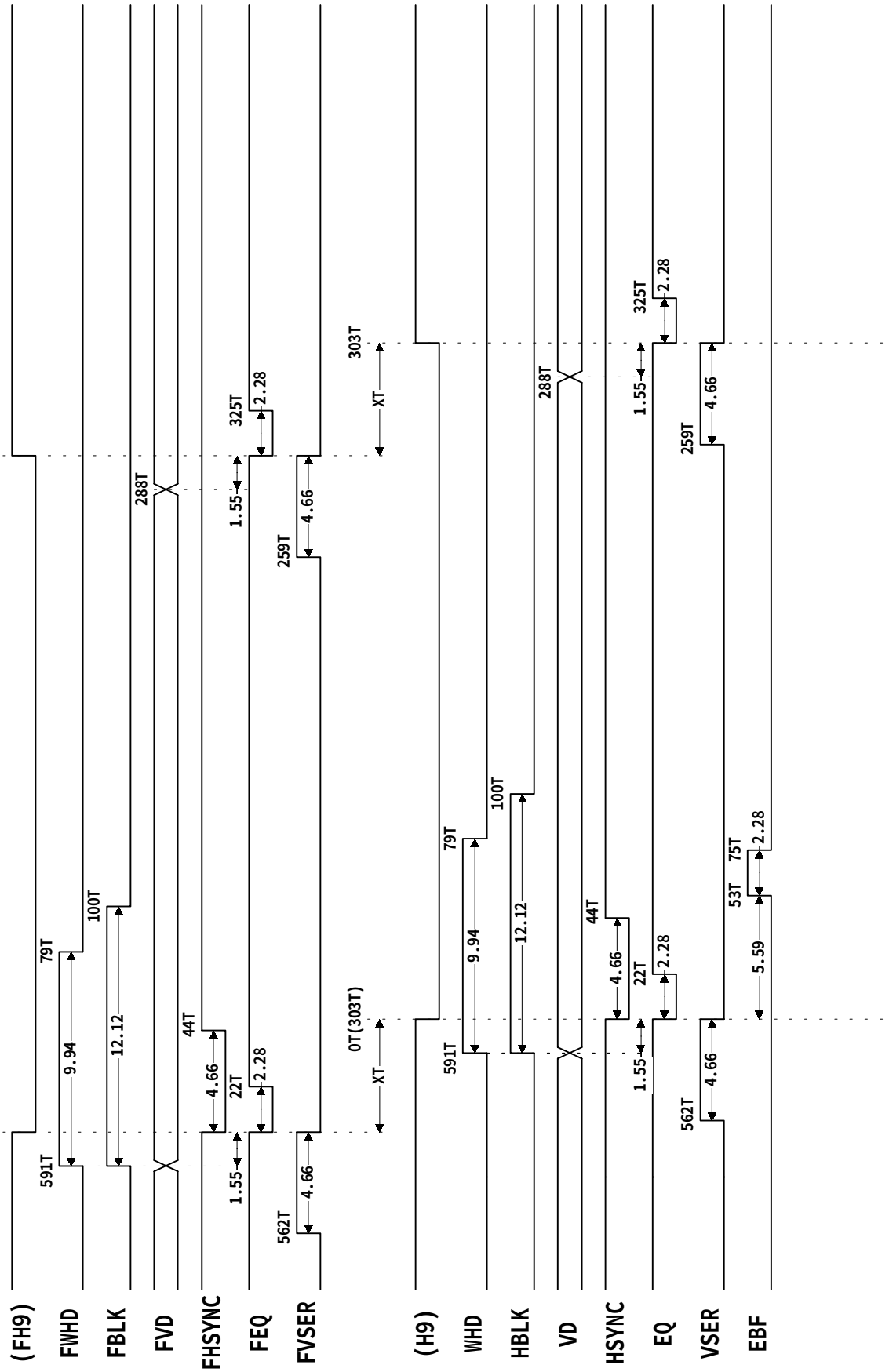
SSG block timing H rate (MN39217 PAL 510H)

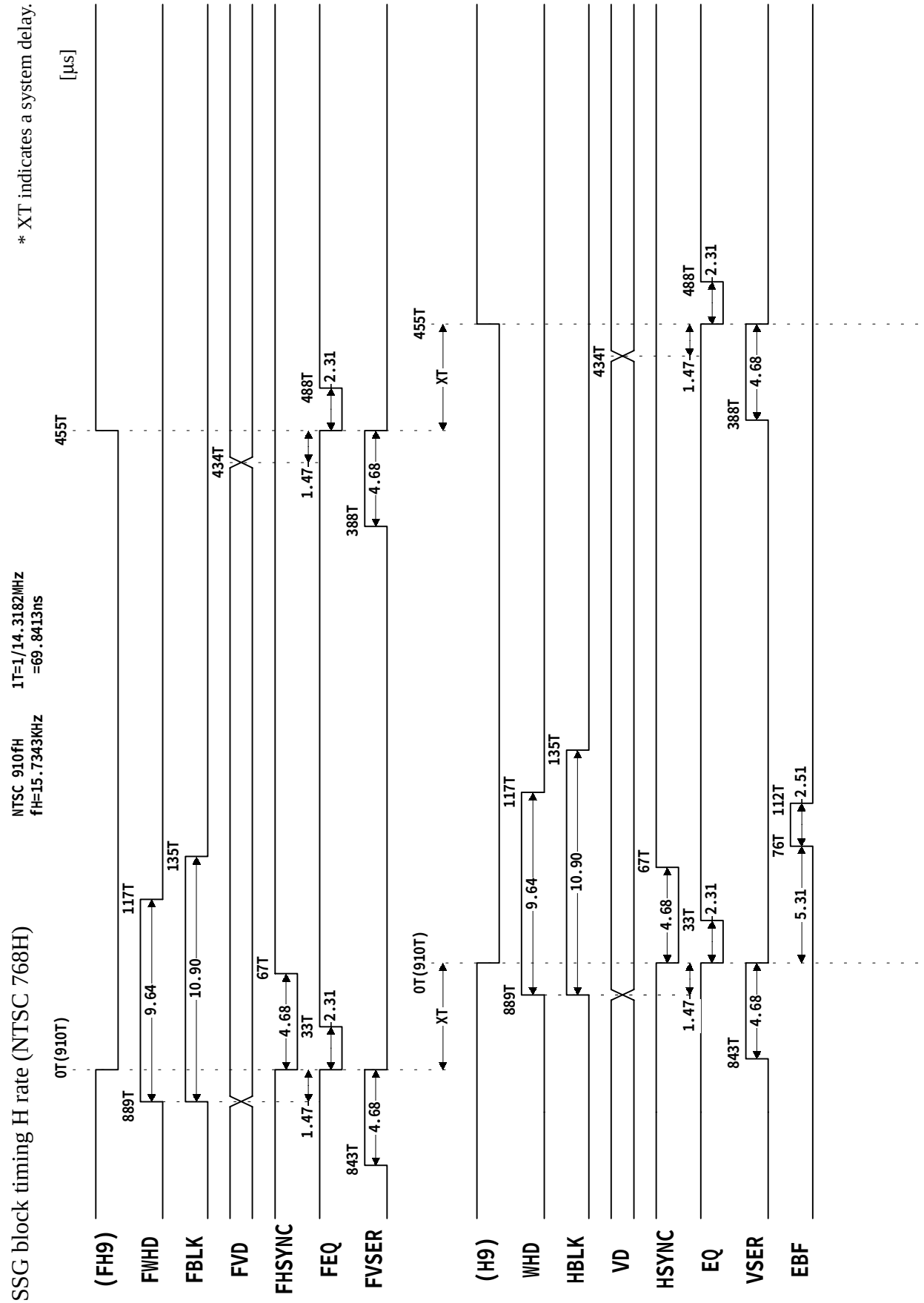
PAL 606fH
fH=15.625KHz

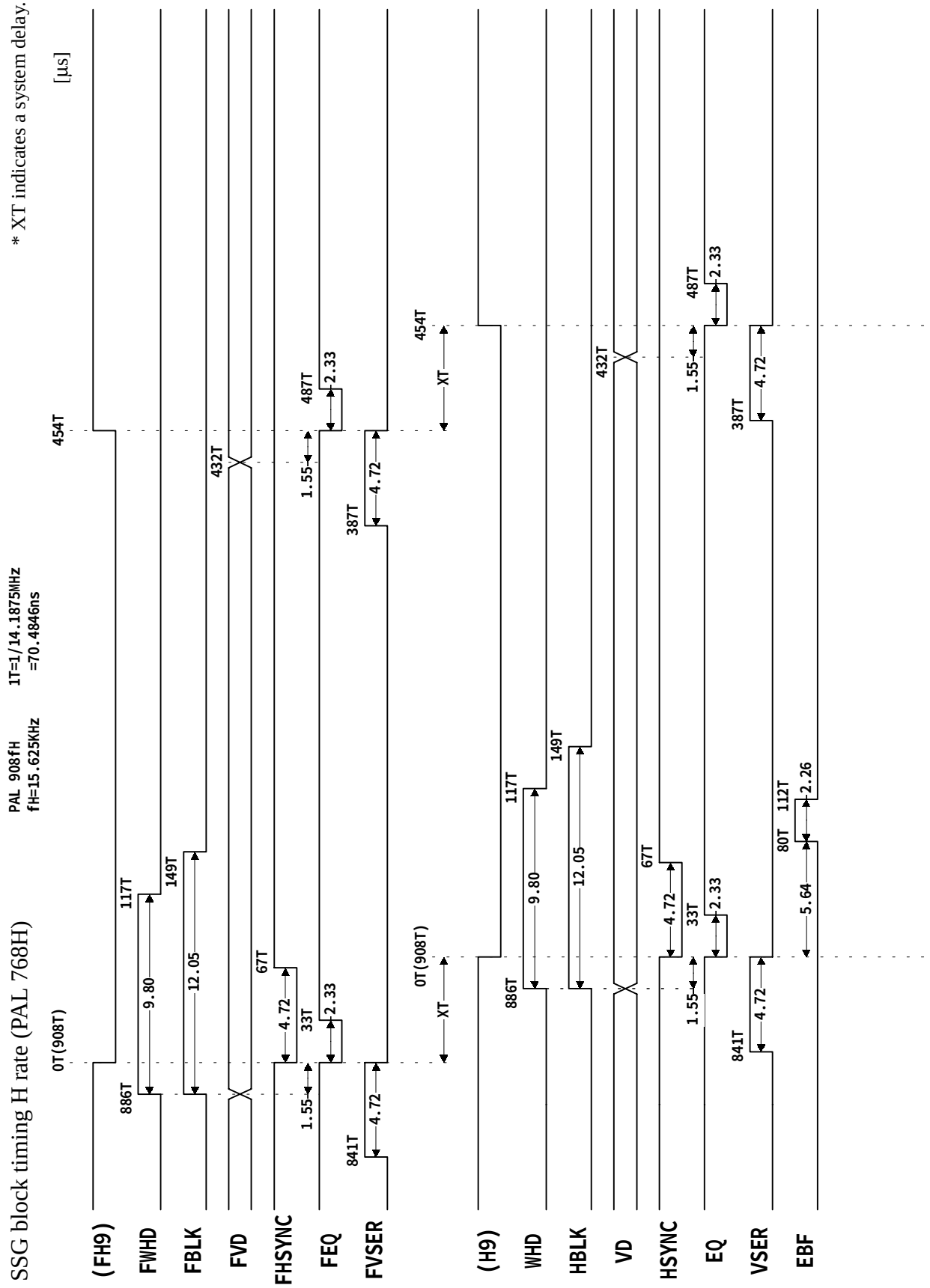
1T=1/9.4688MHz
=105.6106ns

* XT indicates a system delay.

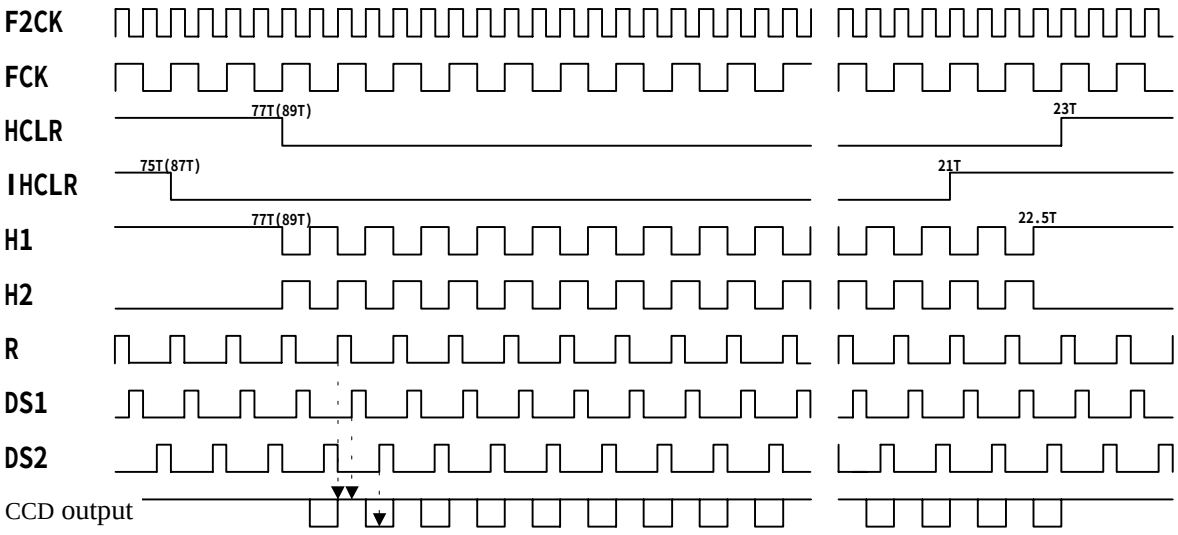
[µs]



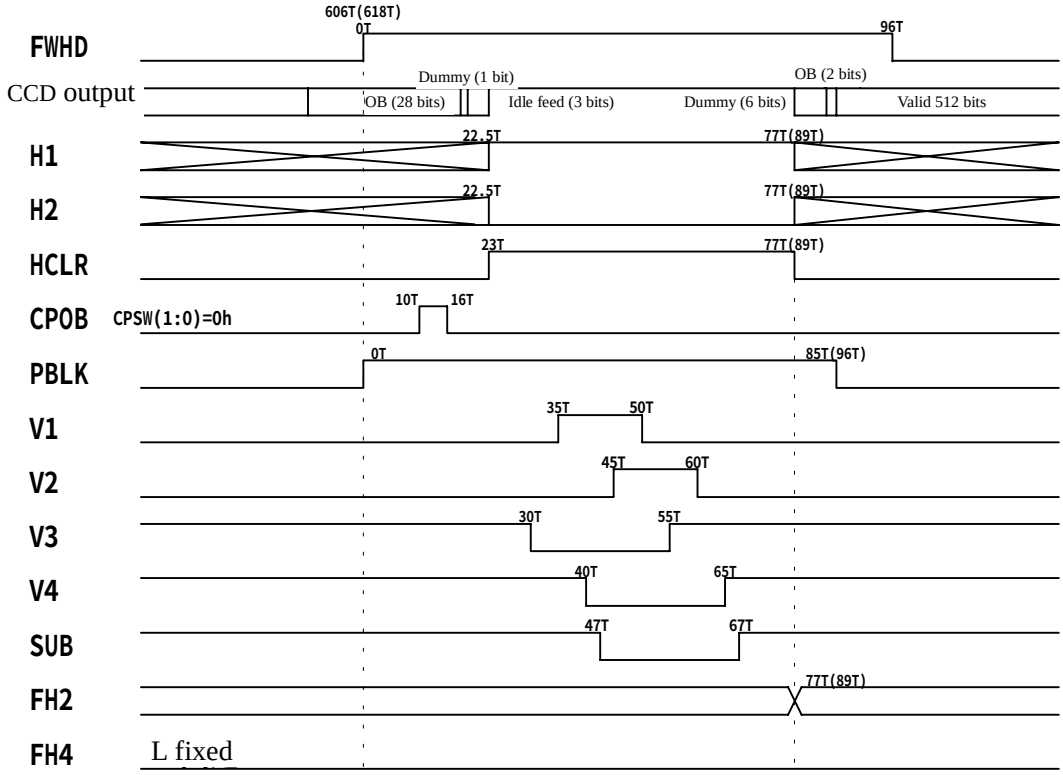

SSG block timing H rate (NTSC 768H)
NTSC 910fH
fH=15.7343KHz
1T=1/14.3182MHz
=69.8413ns
* XT indicates a system delay.
[µs]
(FH9)
FWHD
FBLK
FVD
FHSYNC
FEQ
FVSER
(H9)
WHD
HBLK
VD
HSYNC
EQ
VSER
EBF
0T(910T)
455T
434T
117T
135T
67T
33T
889T
843T
388T
488T
9.64
10.90
4.68
2.31
1.47
XT
76T
112T
2.51
5.31


SSG block timing H rate (PAL 768H)
PAL 908fH
fH=15.625KHz
1T=1/14.1875MHz
=70.4846ns
* XT indicates a system delay.
[µs]
(FH9)
FWHD
FBLK
FVD
FHSYNC
FEQ
FVSER
(H9)
WHD
HBLK
VD
HSYNC
EQ
VSER
EBF
0T(908T)
454T
886T
117T
9.80
149T
12.05
432T
67T
4.72
33T
2.33
1.55
487T
387T
841T
XT
112T
80T
2.26
5.64

O MN39110 series: High-speed pulse timing



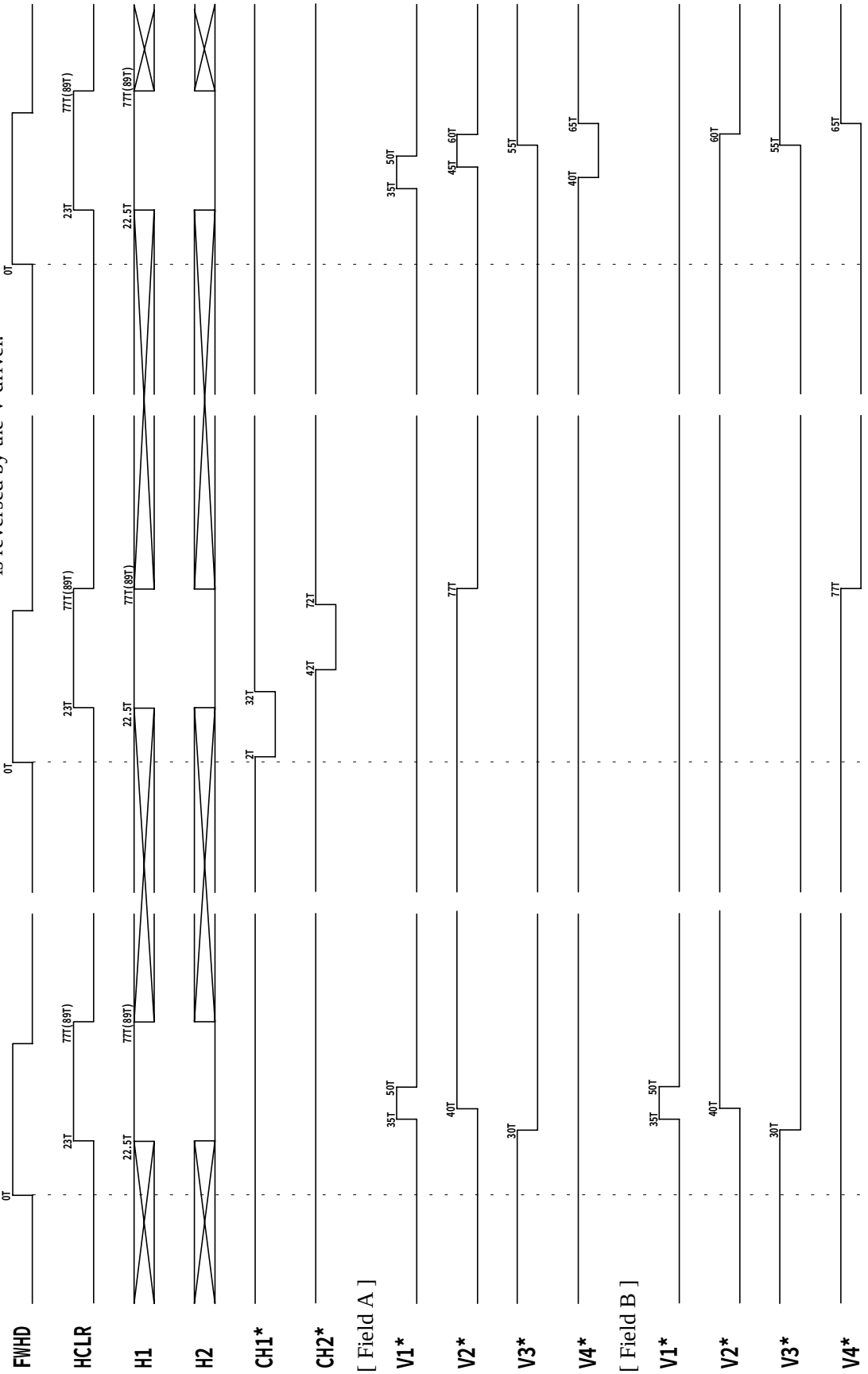
O MN39110 series: H rate timing (Enlarged view of section B)



Note) • 1 = 1/FCK (NTSC: 104.8 ns, PAL: 103.56 ns)
• OT represents the rising edge of FWHD.
• ( ) for PAL
• V1, V2, V3, V4 and SUB are reversed by the V driver and input to CCD.

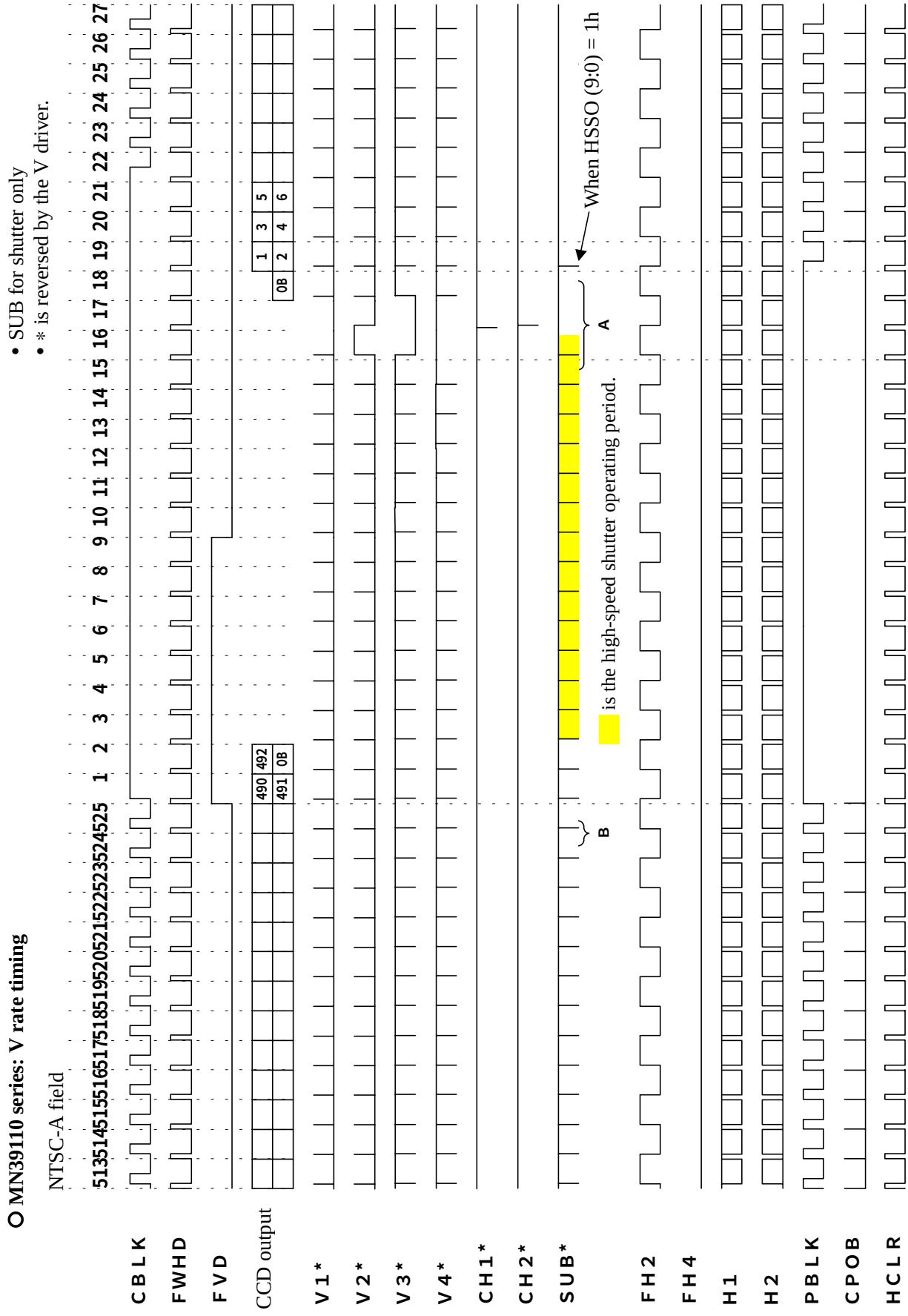
O MN39110 series: Timing in detail (Enlarged view of section A)

- 1T = 104.88 ns: NTSC, 103.56 ns: PAL
- ( ) for PAL
- * is reversed by the V driver.



O MN39110 series: V rate timing

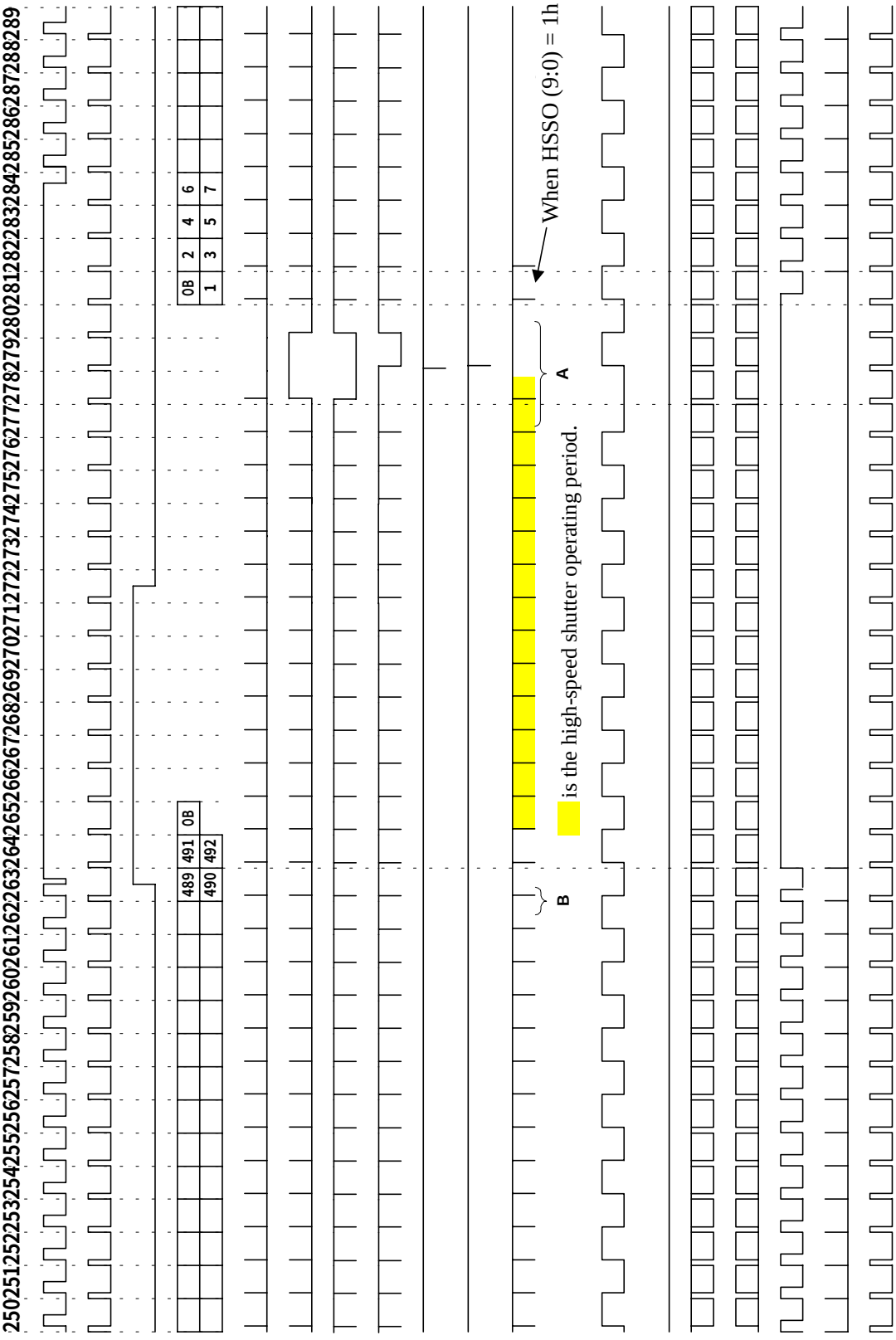
NTSC-A field



O MN39110 series: V rate timing

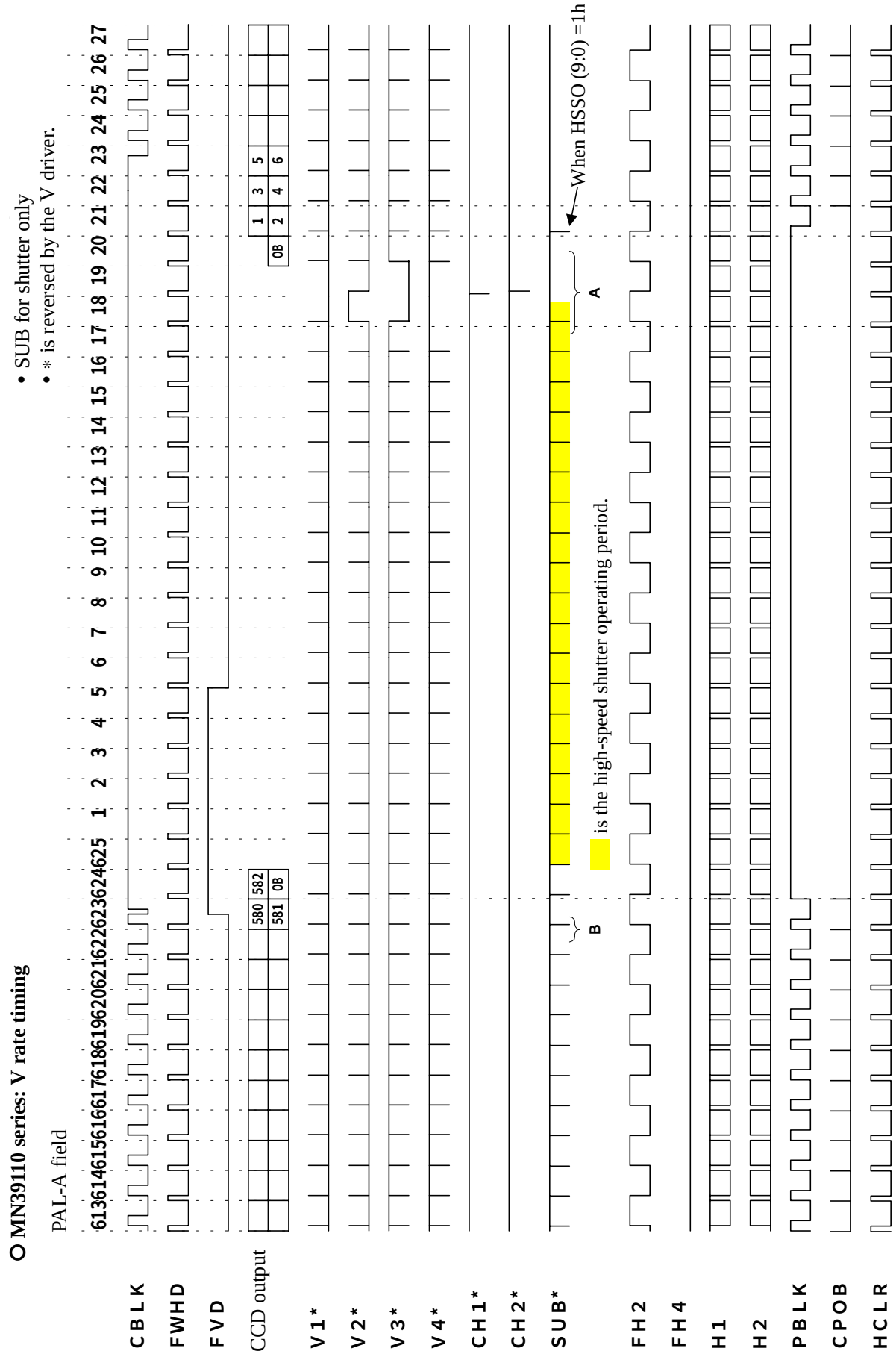
NTSC-B field

• SUB for shutter only
• * is reversed by the V driver.



O MN39110 series: V rate timing

PAL-A field



- SUB for shutter only
- * is reversed by the V driver.

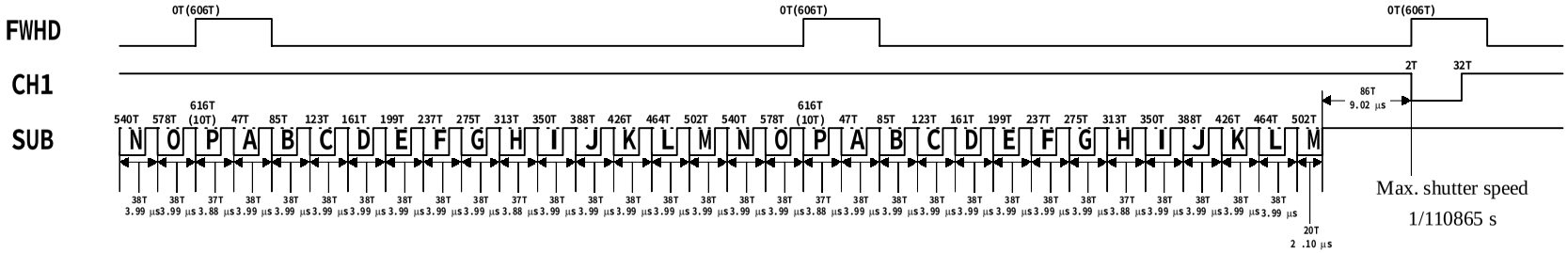
O MN39110 series: V rate timing

PAL-B field

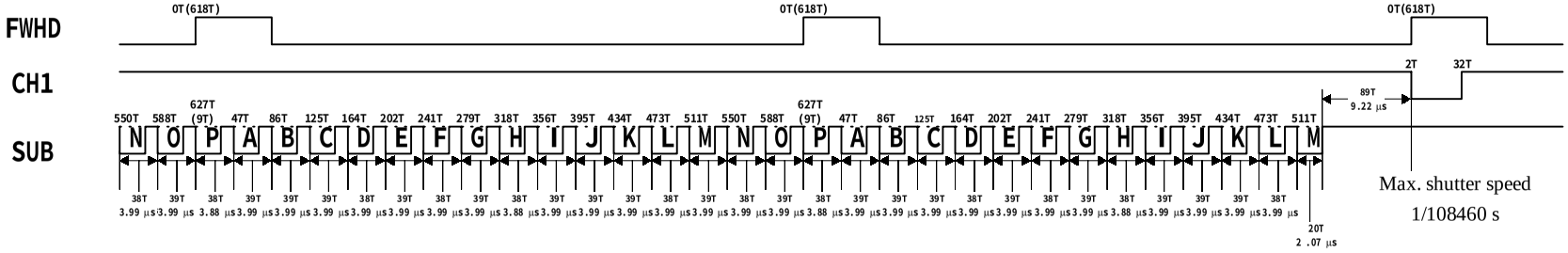
- SUB for shutter only
- * is reversed by the V driver.

○ MN39110 series: Electronic aperture SUB pulse timing chart (high-speed mode)

[NTSC mode: 1T=1/FCK=104.88 ns]

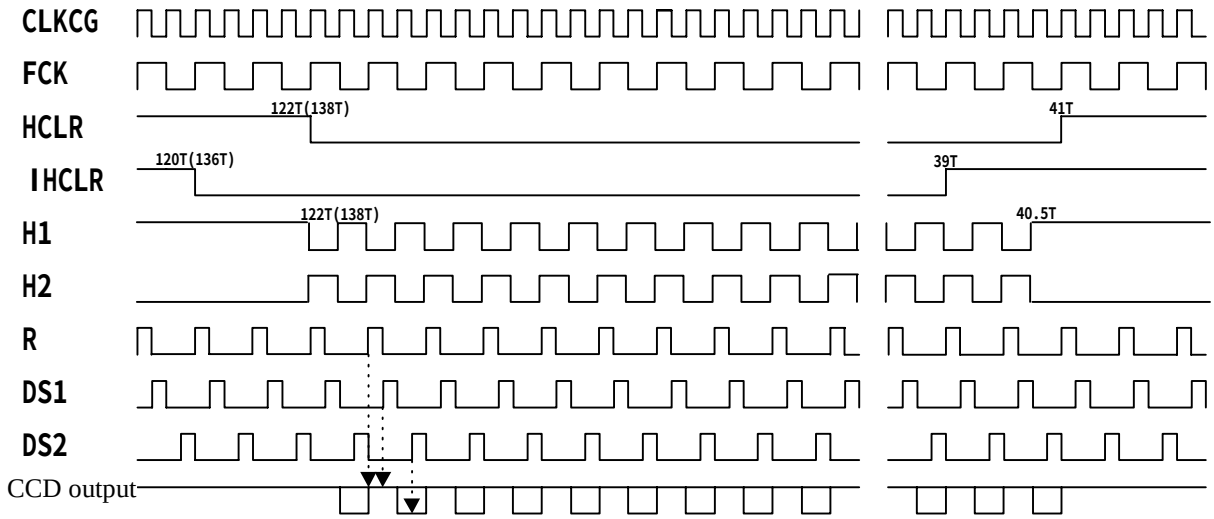


[PAL mode: 1T=1/FCK=103.56 ns]



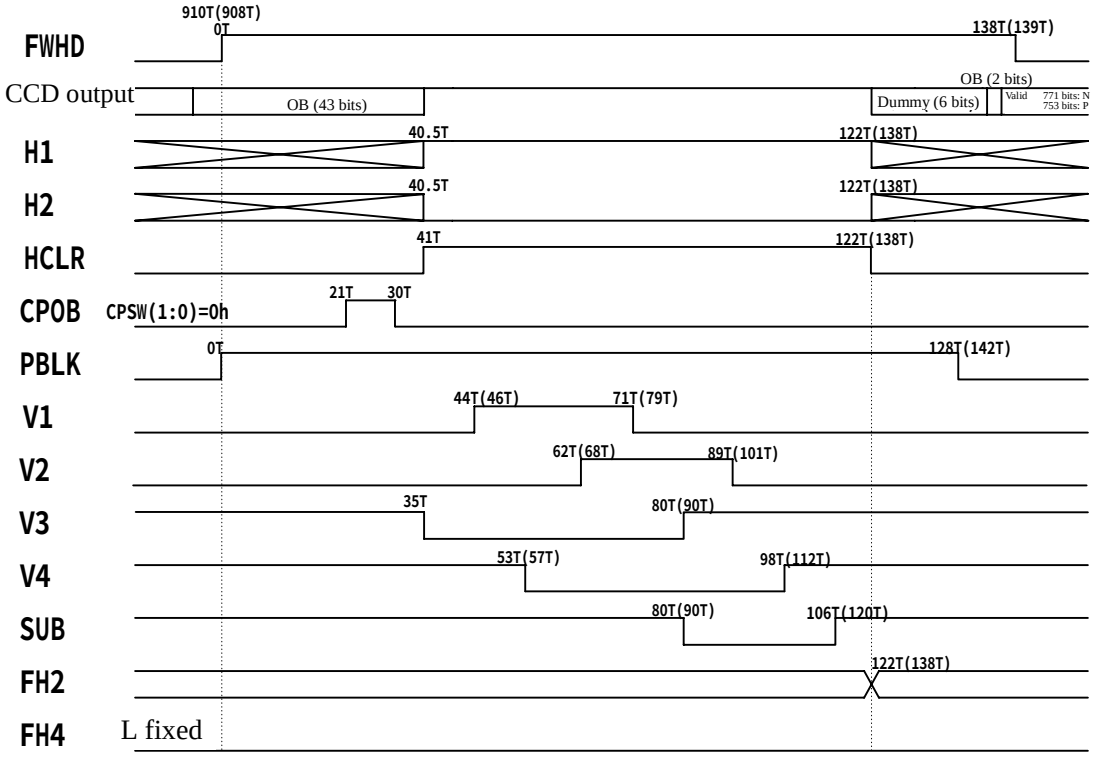
	HSSO(9:0)	HSSOS(3:0) 4	3	2	1	Operating condition
A	If defined as n = HSSO(9:0), the electric charge accumulation time is defined by the following equation: NTSC: (261 – n)H (where 0 < n ≤ 260) For n = 0, 262 or 263 PAL: (311 – n)H (where 0 < n ≤ 310) For n = 0, 312 or 313	L	L	L	L	Output every H both within the valid period and VBLK until the horizontal timing specified by HSSO(9:0).
B		L	L	L	H	Only one pulse specified by HSSOS(3:0) in B through P is output if it falls in one horizontal operating period immediately following pulse A specified by HSSO(9:0) and the line falls in VBLK before CH1 is applied.
C		L	L	H	L	
D		L	L	H	H	
E		L	H	L	L	
F		L	H	L	H	
G		L	H	H	L	
H		L	H	H	H	
I		H	L	L	L	
J		H	L	L	H	
K		H	L	H	L	
L		H	L	H	H	
M		H	H	L	L	
N		H	H	L	H	In addition to the condition mentioned above: If pulses N through P are specified only in one horizontal scanning period immediately before the CH1 pulse, a pulse is generated at position M.
O		H	H	H	L	
P		H	H	H	H	

O MEC 1/3 type 768H CCD high-speed pulse timing



O MEC 1/3 type 768H CCD H rate timing

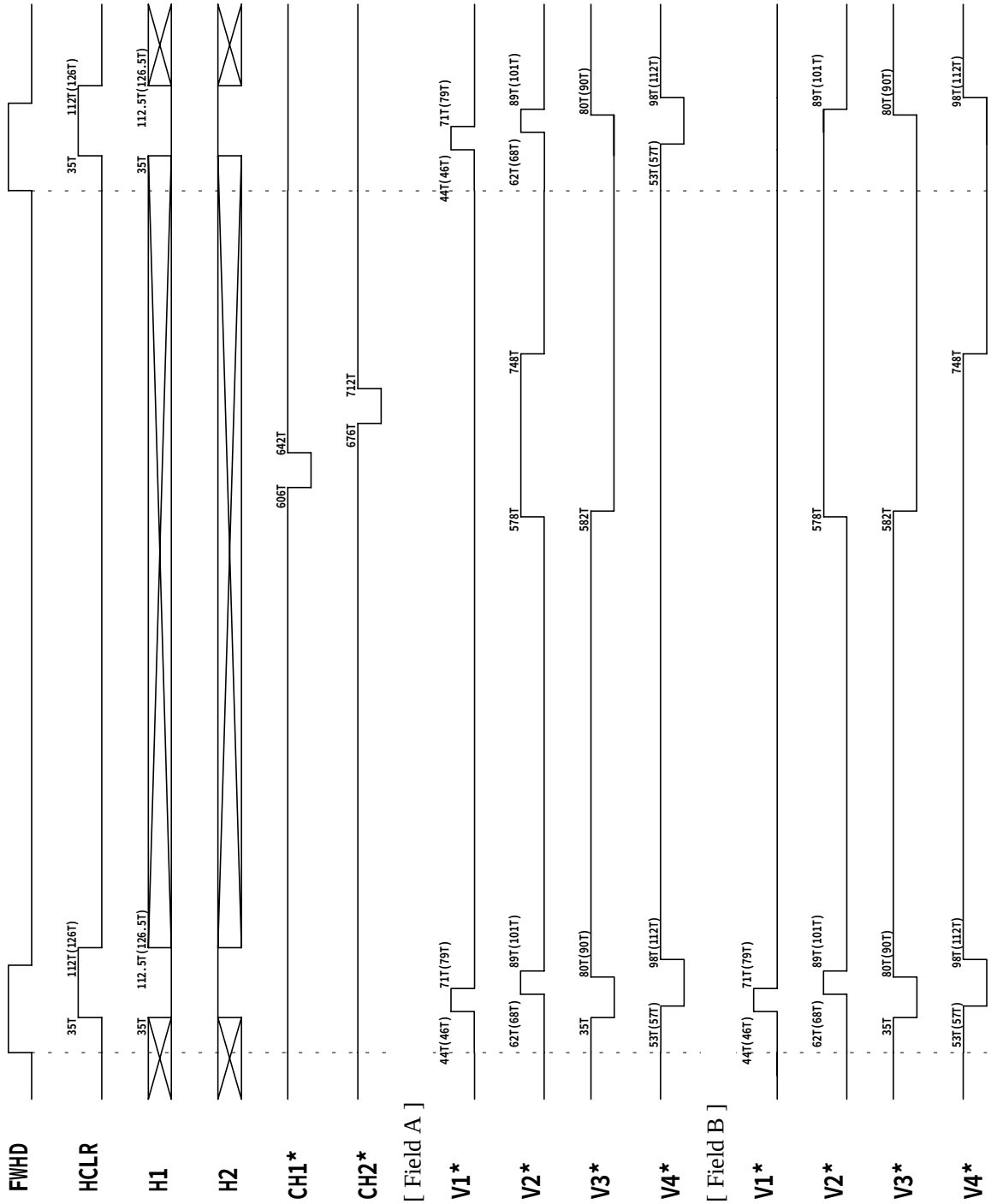
(Enlarged view of section B)



(Note)
- 1T=1/FCK (69.8 ns: NTSC, 70.4 ns: PAL)
- 0T is the rising edge of FWHD.
- ( ) for PAL
- V1, V2, V3, V4 and SUB are reversed by the V driver and input to CCD.

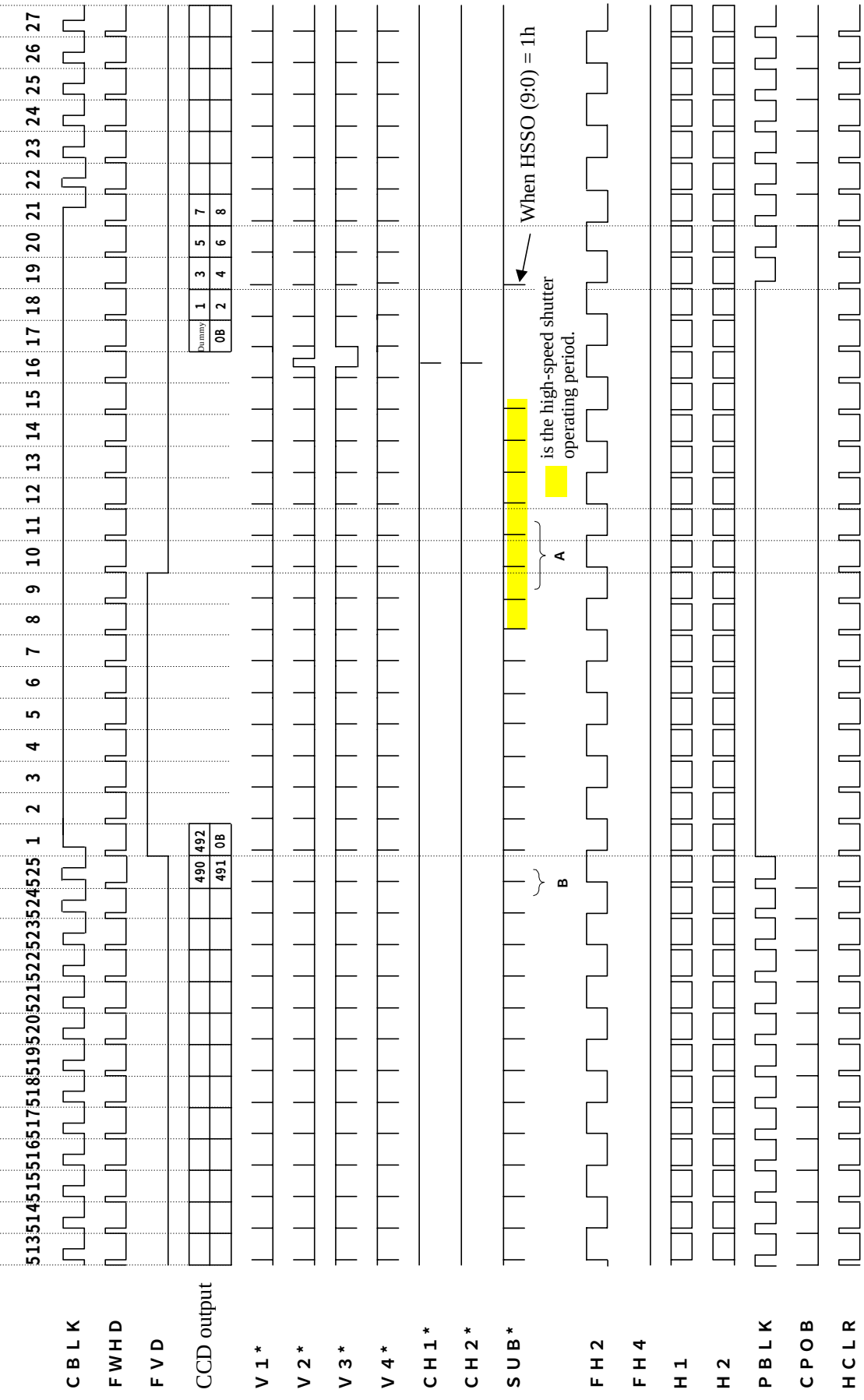
O MEC 1/3 type 768H CCD V rate timing in detail (Enlarged view of section A)

- 1T=1/FCK=69.8 ns: NTSC, 70.4 ns: PAL
- ( ) for PAL
- * is reversed by the V driver.

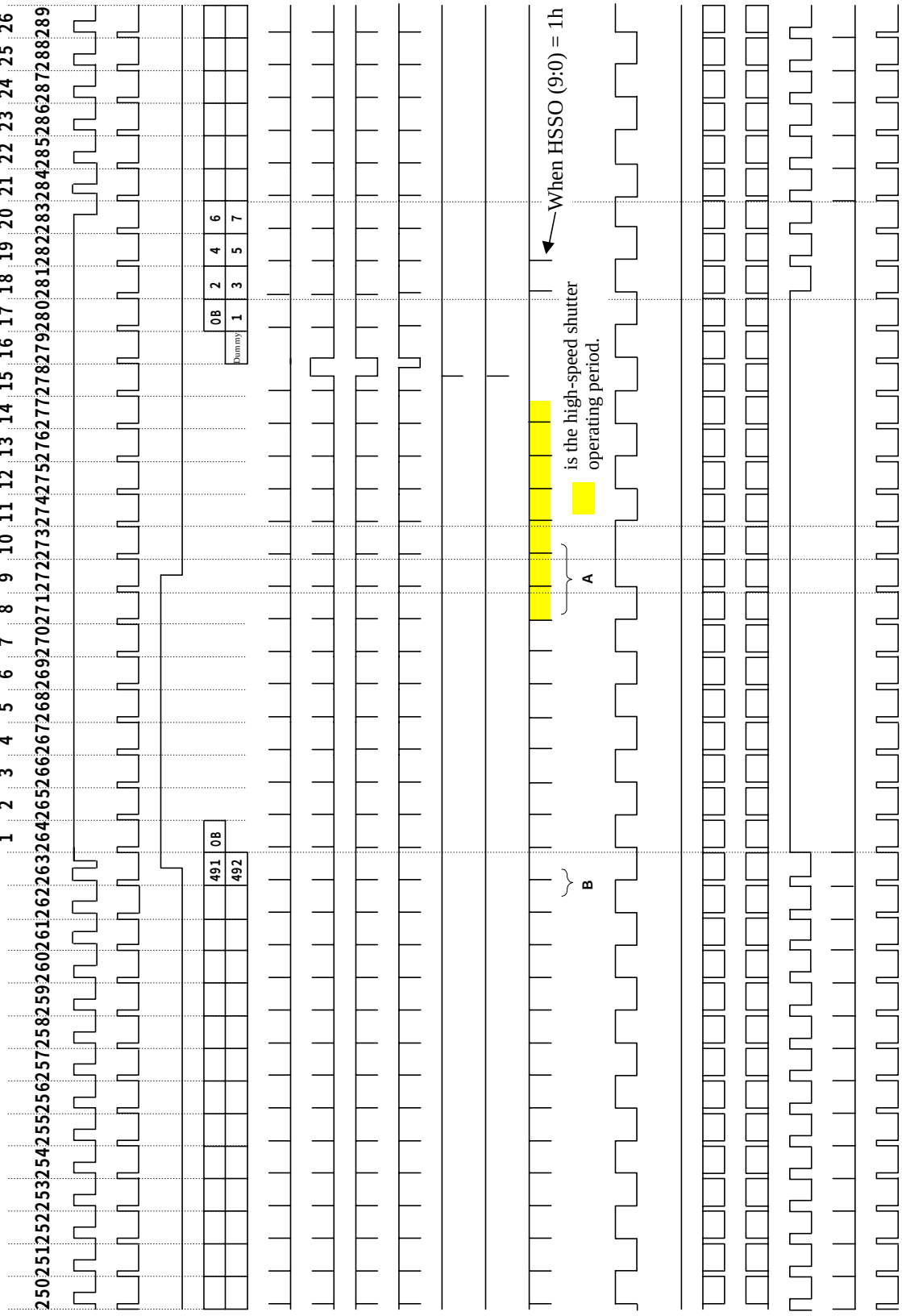


O MEC 1/3 type 768H CCD V rate timing

NTSC-A field



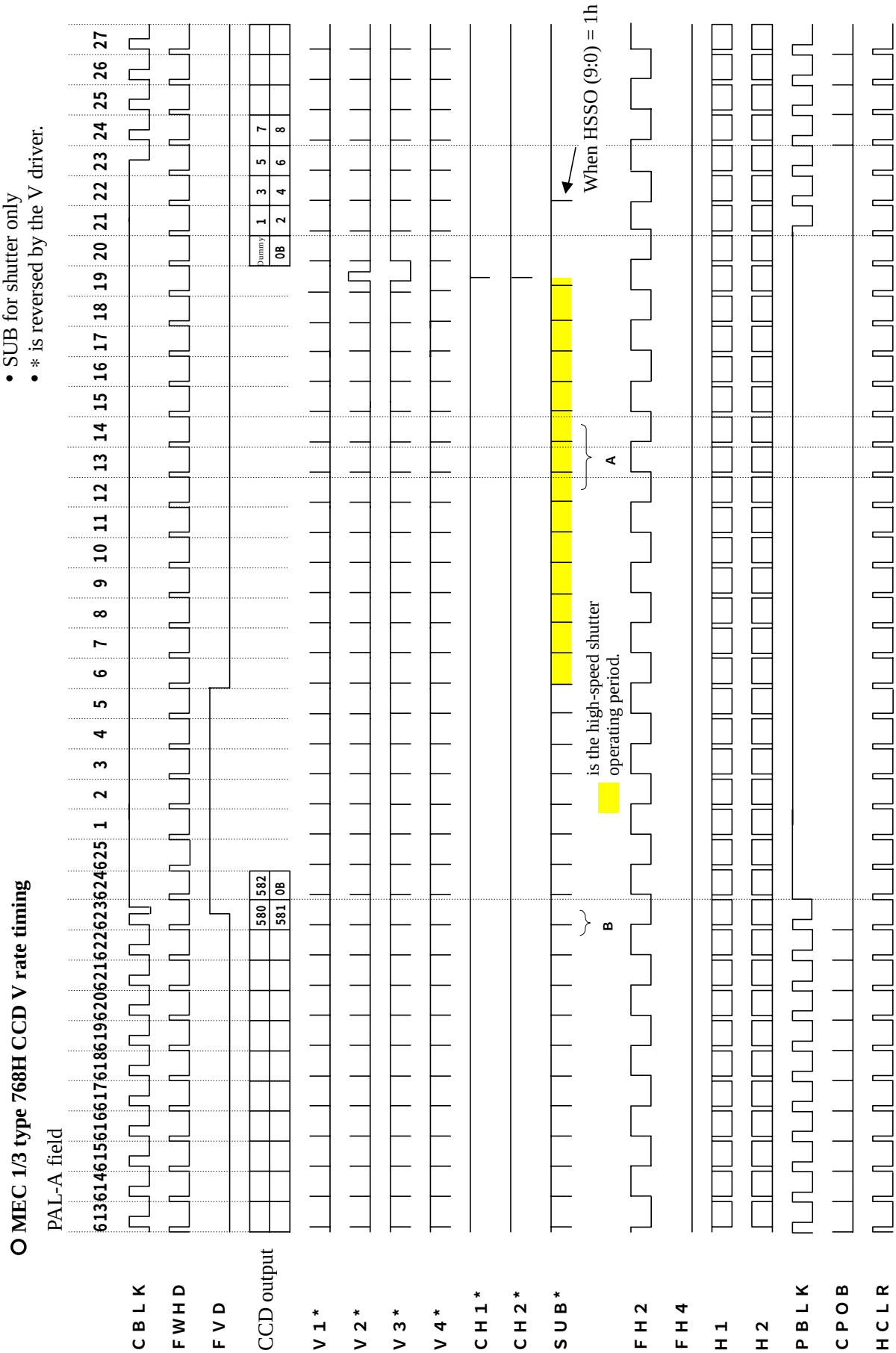
O MEC 1/3 type 768H CCD V rate timing



- SUB for shutter only
- * is reversed by the V driver.

O MEC 1/3 type 768H CCD V rate timing

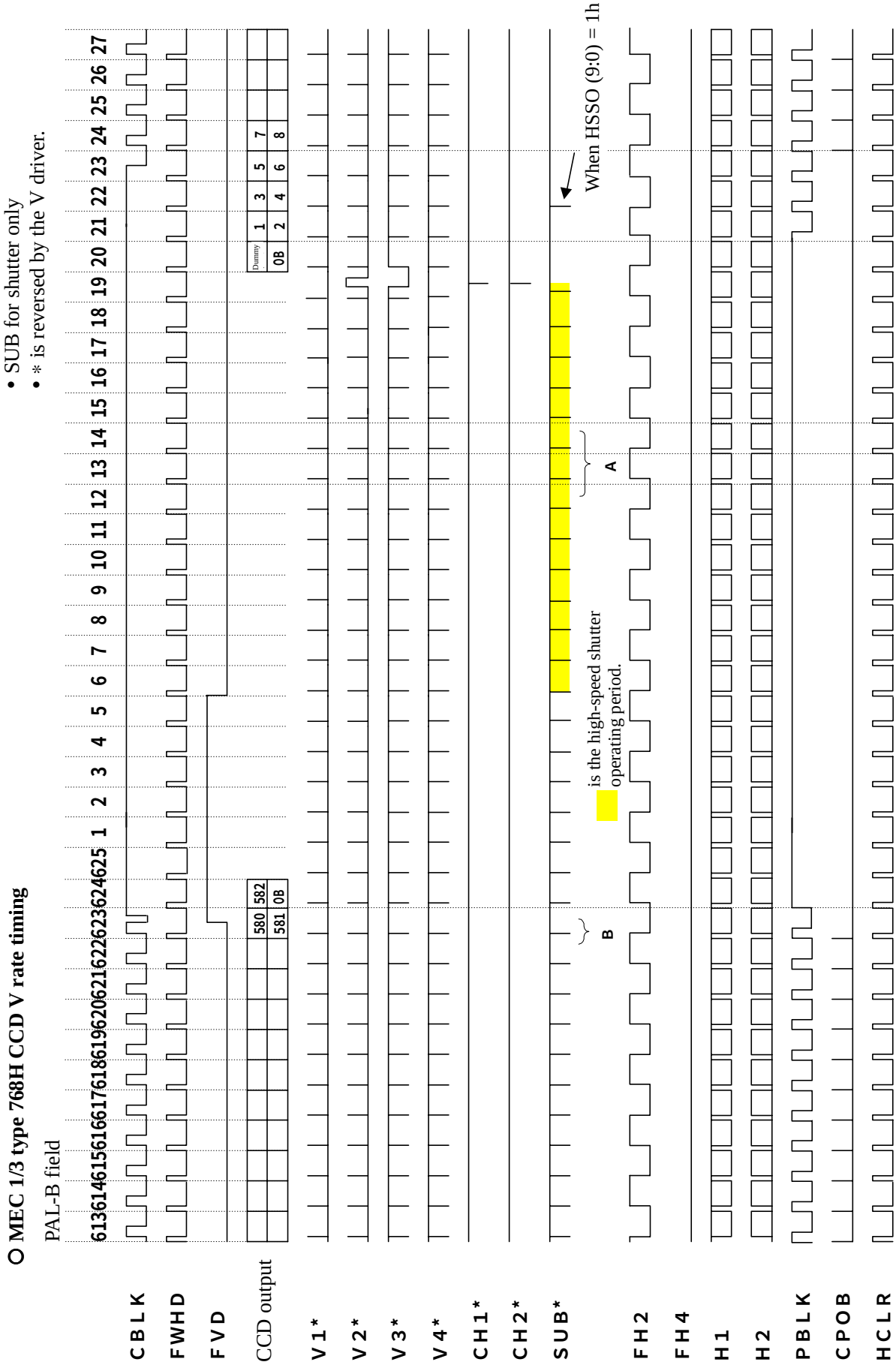
PAL-A field



O MEC 1/3 type 768H CCD V rate timing

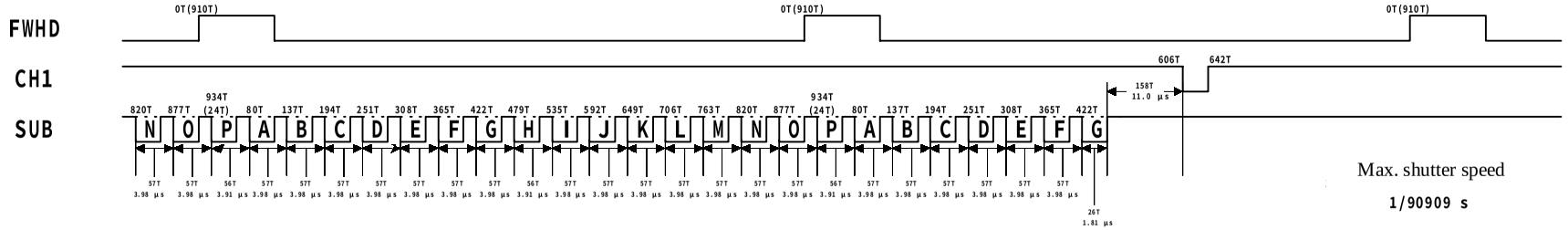
PAL-B field

- SUB for shutter only
- * is reversed by the V driver.

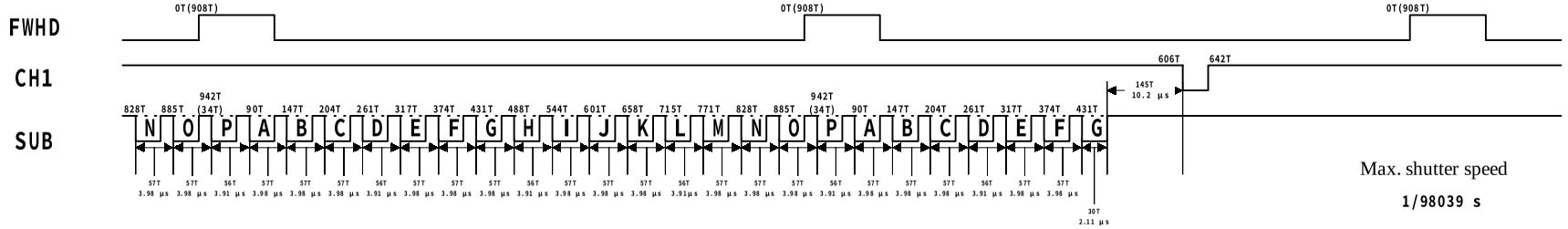


○ MEC 1/3 type 768H CCD: Electronic aperture SUB pulse timing chart (high-speed mode)

[NTSC mode: 1T=1/FCK=69.8 ns]



[PAL mode: 1T=1/FCK=70.4 ns]

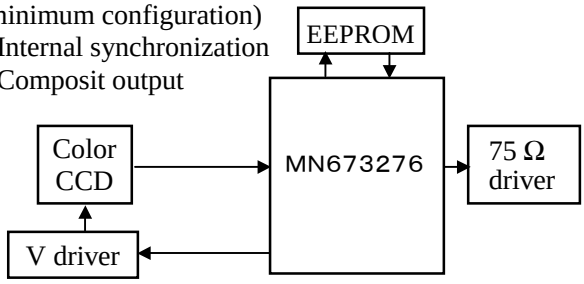


	HSSO(9:0)	HSSOS(3:0) 4	3	2	1	Operating condition
A	If defined as n = HSSO(9:0), the electric charge accumulation time is defined by the following equation: NTSC: (261 – n)H (where 0 < n ≤ 260) For n = 0, 262 or 263 PAL: (311 – n)H (where 0 < n ≤ 310) For n = 0, 312 or 313	L	L	L	L	Output every H both within the valid period and VBLK until the horizontal timing specified by HSSO(9:0).
B		L	L	L	H	Only one pulse specified by HSSOS(3:0) in B through P is output if it falls in one horizontal operating period immediately following pulse A specified by HSSO(9:0) and the line falls in VBLK before CH1 is applied.
C		L	L	H	L	
D		L	L	H	H	
E		L	H	L	L	
F		L	H	L	H	
G		L	H	H	L	
H		L	H	H	H	In addition to the condition mentioned above: If pulses H through P are specified only in one horizontal scanning period immediately before the CH1 pulse, a pulse is generated at position G.
I		H	L	L	L	
J		H	L	L	H	
K		H	L	H	L	
L		H	L	H	H	
M		H	H	L	L	
N		H	H	L	H	
O		H	H	H	L	
P		H	H	H	H	

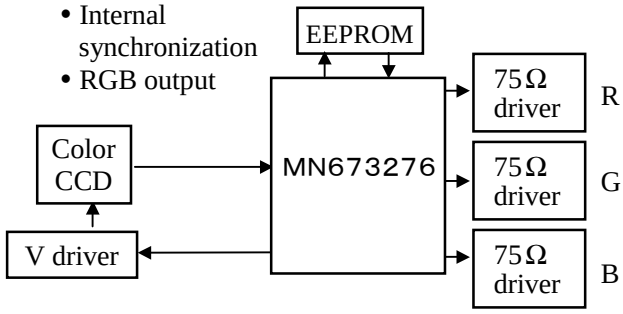
11. Application Examples

11.1 System configuration examples

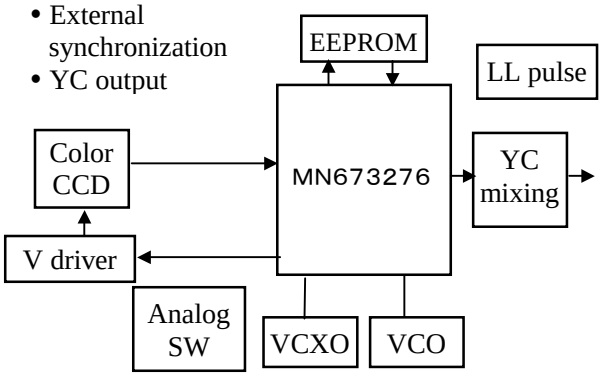
(1) Configuration A
(minimum configuration)
• Internal synchronization
• Composit output



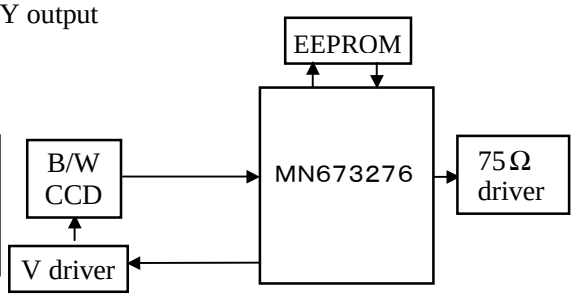
(2) Configuration B
• Internal synchronization
• RGB output



(3) Configuration C
(Monitor camera)
• External synchronization
• YC output

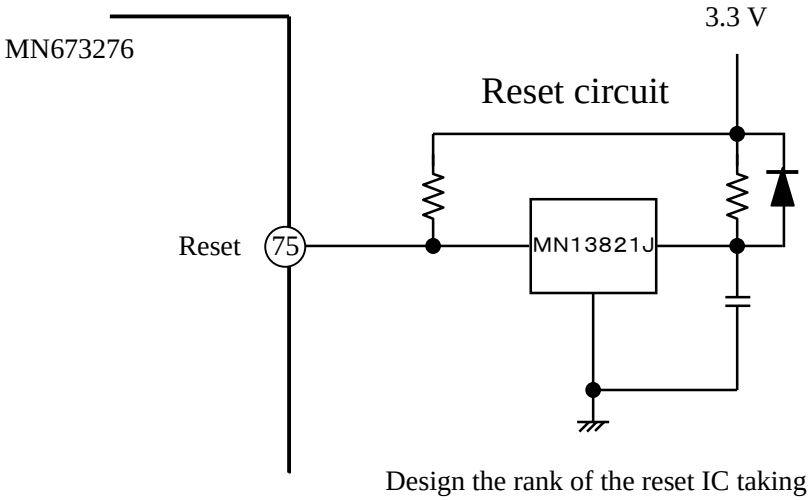


(4) Configuration D
• Internal synchronization
• Y output



11.2 Reset

It is recommended to use an exclusive reset IC to reset the system securely when the power is turned ON/OFF.

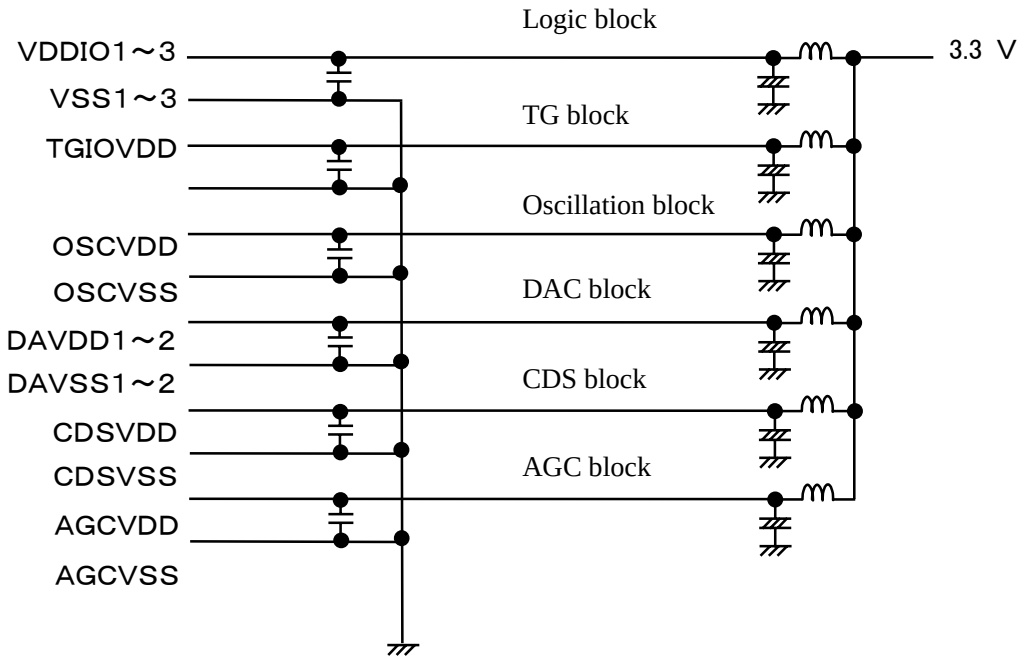


Design the rank of the reset IC taking the allowance of the system into consideration.

11.3 Power supply and grounding

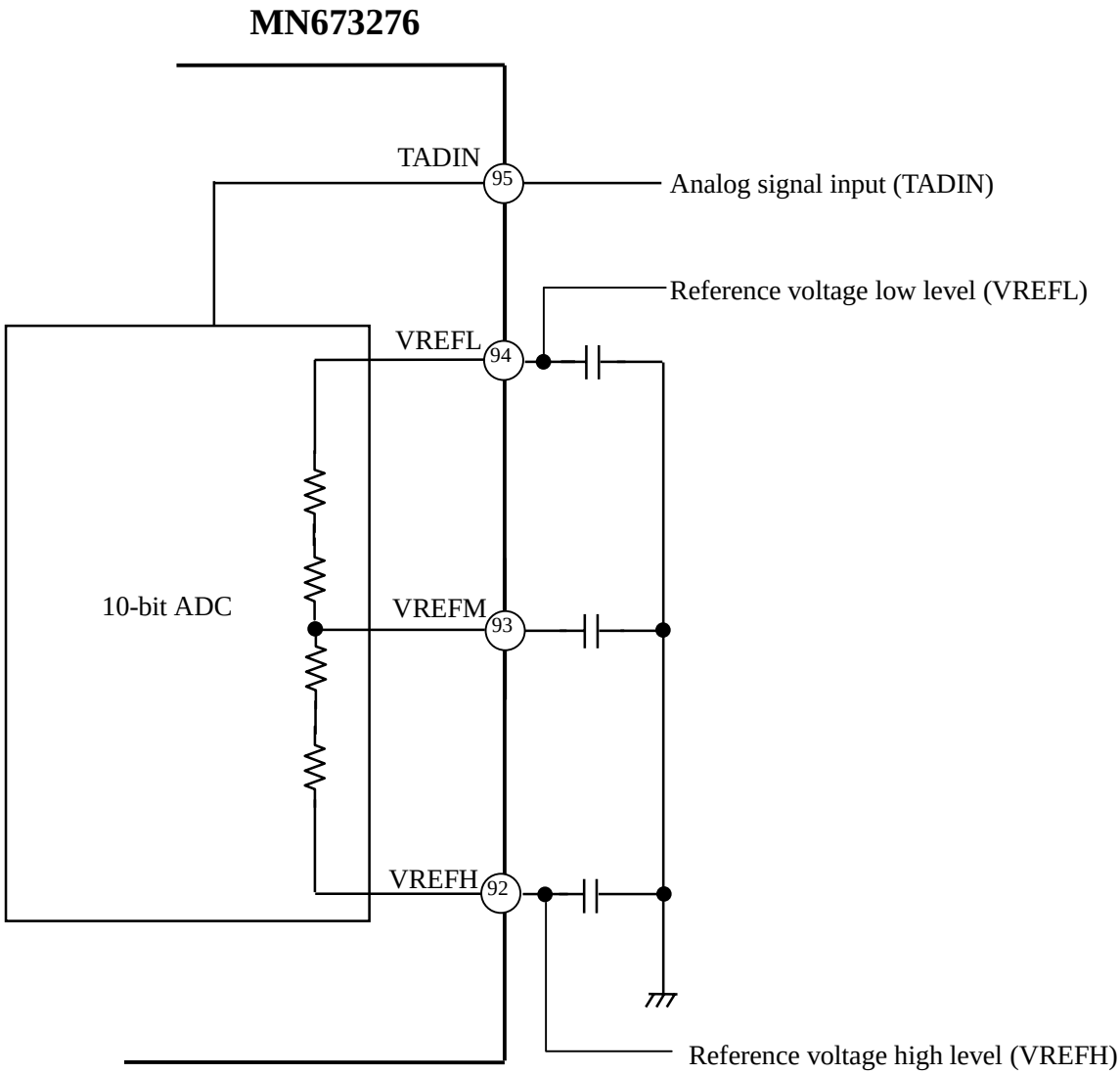
The power supply pins are isolated from one another as listed below to prevent noise from being induced inside the LSI.
When connecting a power supply on a board, it is recommended to isolate the blocks from one another using LC filters as shown below.
The figure shows a diagram in which a 3.3 V power supply is used.

Name	Power supply (3. 3 V)	Name	Power supply (2. 0 V)
VDDIO1-3	Logic block (IO)	VDD1-3	Logic block (internal)
TGIOVDD	CG(IO)	TGVDD	CG (internal)
OSCVDD	Oscillation pin (IO)	ADVDD	ADC
DAVDD1-2	DAC＋AnaSW		
CDSVDD	Analog CDS		
AGCVDD	Analog AGC		



* If a large power supply noise is generated in the TG block, a fixed pattern noise may be generated in the CCD. Therefore, it is recommended to reserve an entire internal layer of a multi-layer board for grounding.

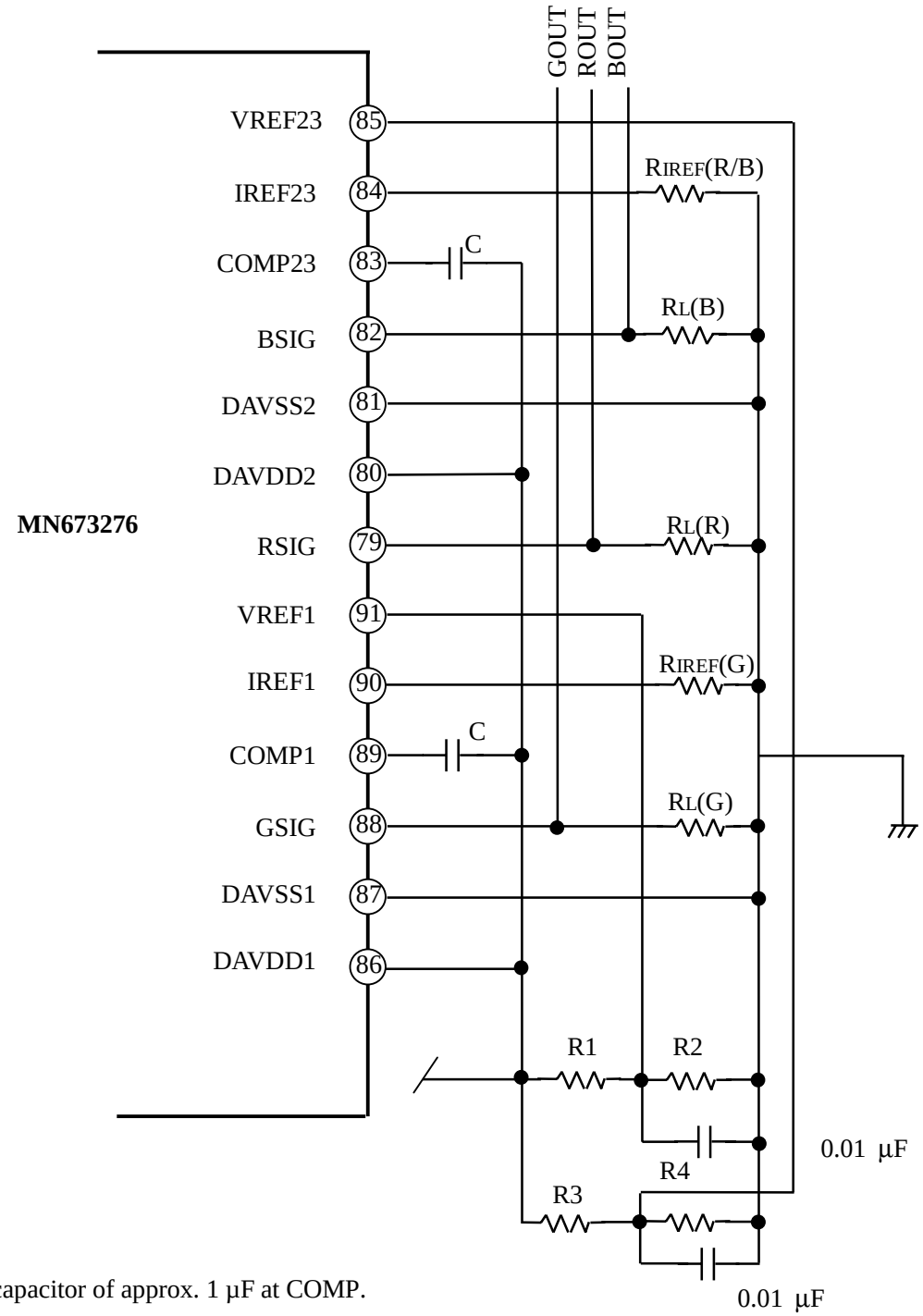
11.4 ADC reference voltage pin



	Min.	Typ.	Max.	Unit
VREFL	ADVSS	0.5		V
VREFH		2.0	ADVDD	V

The dynamic range of the input signal is determined by VREFH – VREFL. It is recommended to use it with a minimum of 1.5 V [P-P].
The direct current resistance across VREFH and VREFL is 240 Ω to 740 Ω. Design the power supply so that its impedance is low enough not to cause voltage variations.
The maximum conversion speed of the A/D converter built in this LSI is 20 MSPS.

11.5 DAC reference voltage pin



- Fit a capacitor of approx. 1 µF at COMP.

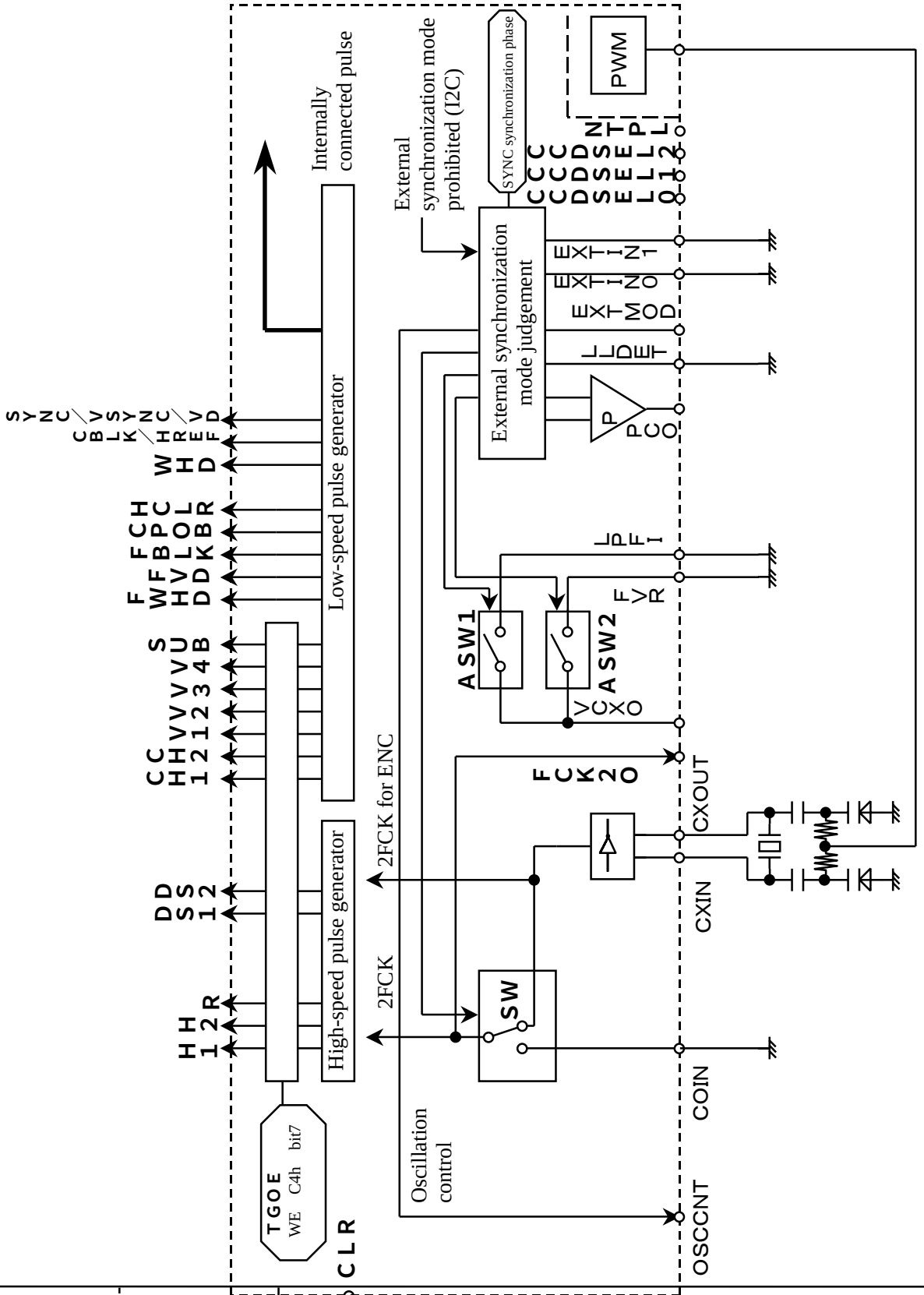
- With RL = 120 Ω and R_{IREF} = 4.7 kΩ, adjust R1/R2 and R3/R4 so that the desired amplitude of the video signal is obtained with VREF = 1.23 V.

- 10-bit DAC (Gch, Y, composite)
  The equation holds: VOUT = (9.84 x VREF/R_{IREF} x RL x N/1023)

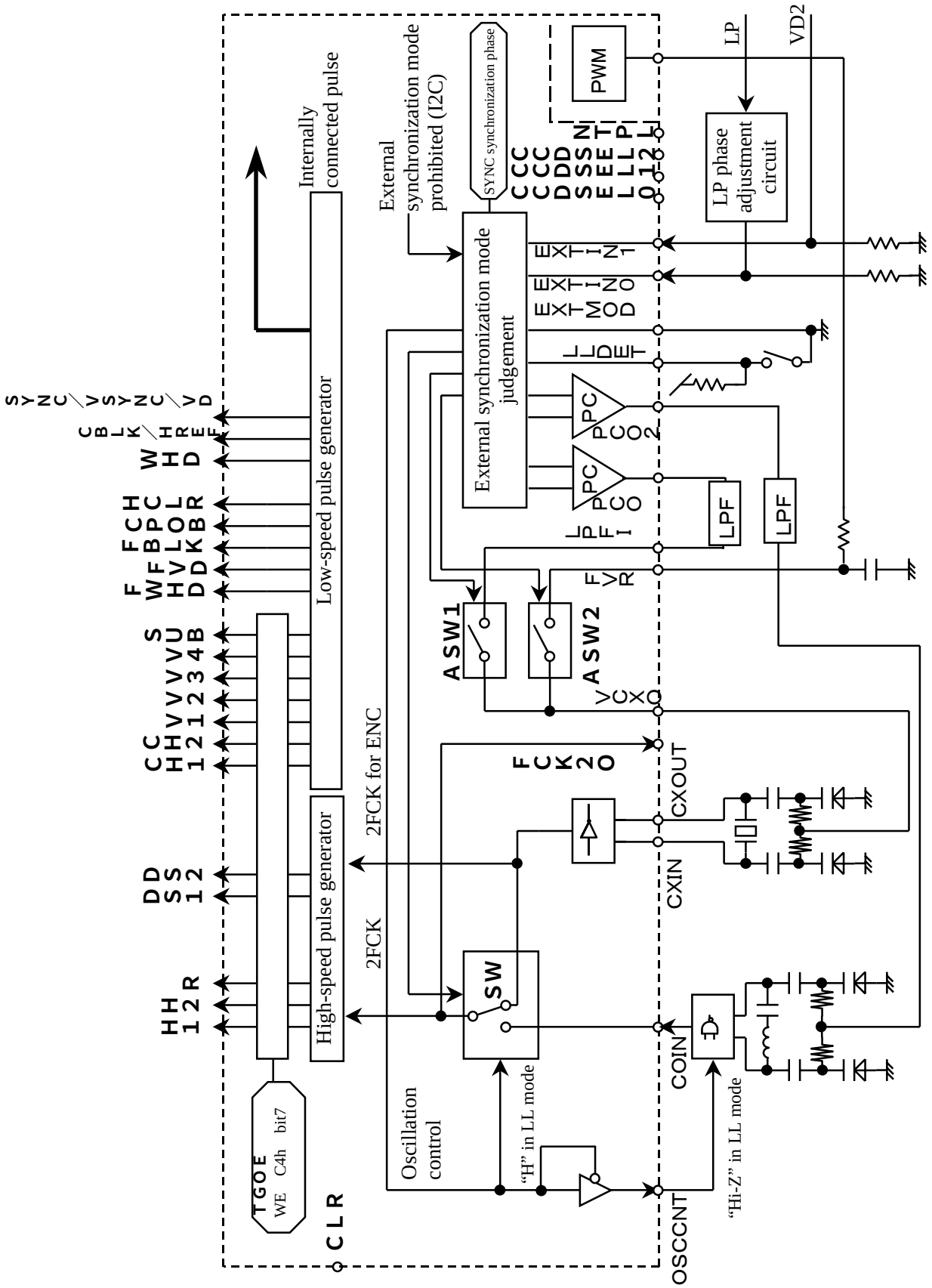
- 8-bit DAC (Rch/Bch, C)
  The equation holds: VOUT = (7.96875 x VREF/R_{IREF} x RL x N/255)

11.6 Clock oscillation system

(1) Internal synchronization

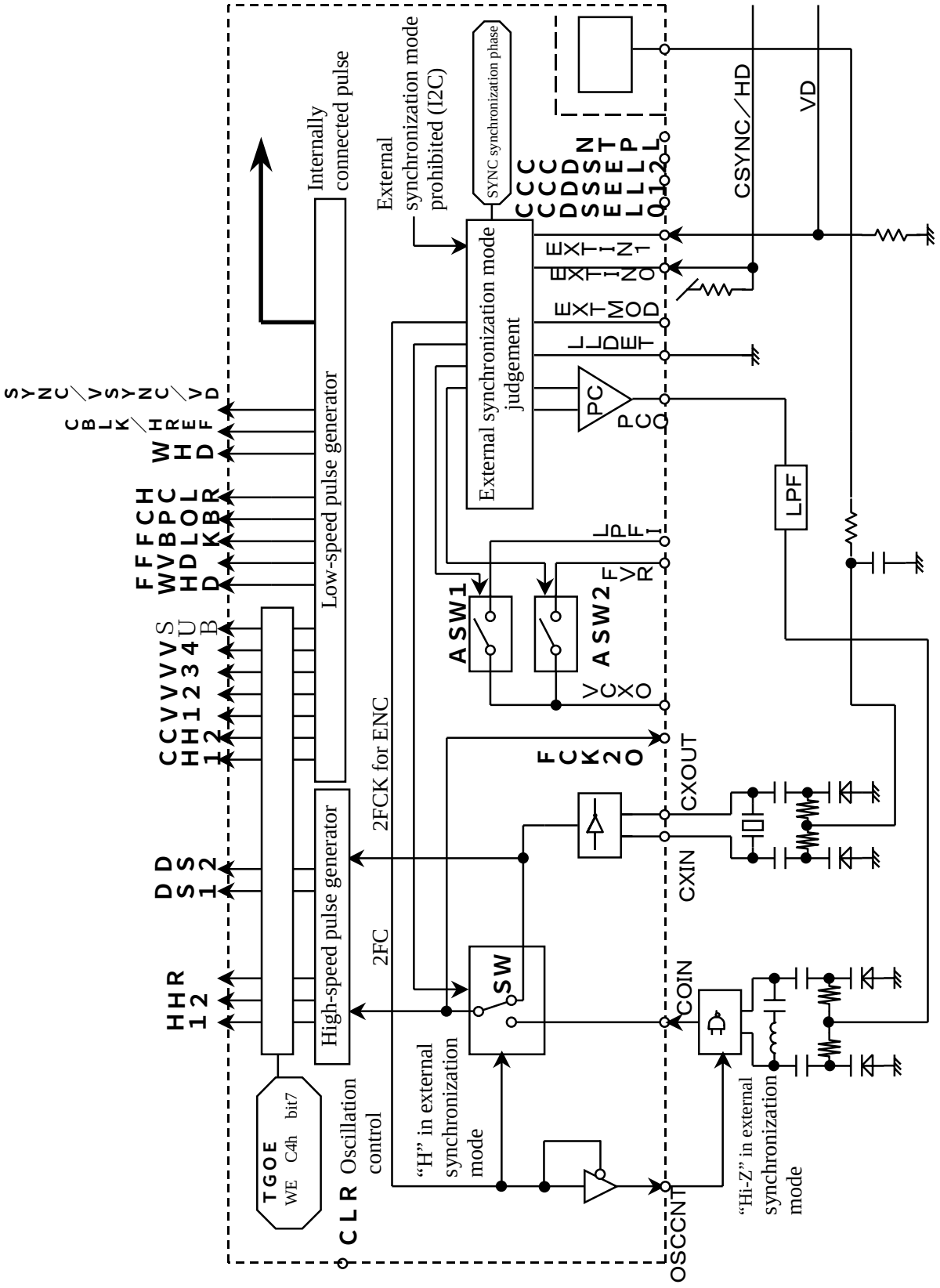


(2) Monitor camera mode (LL and VD2 synchronization)

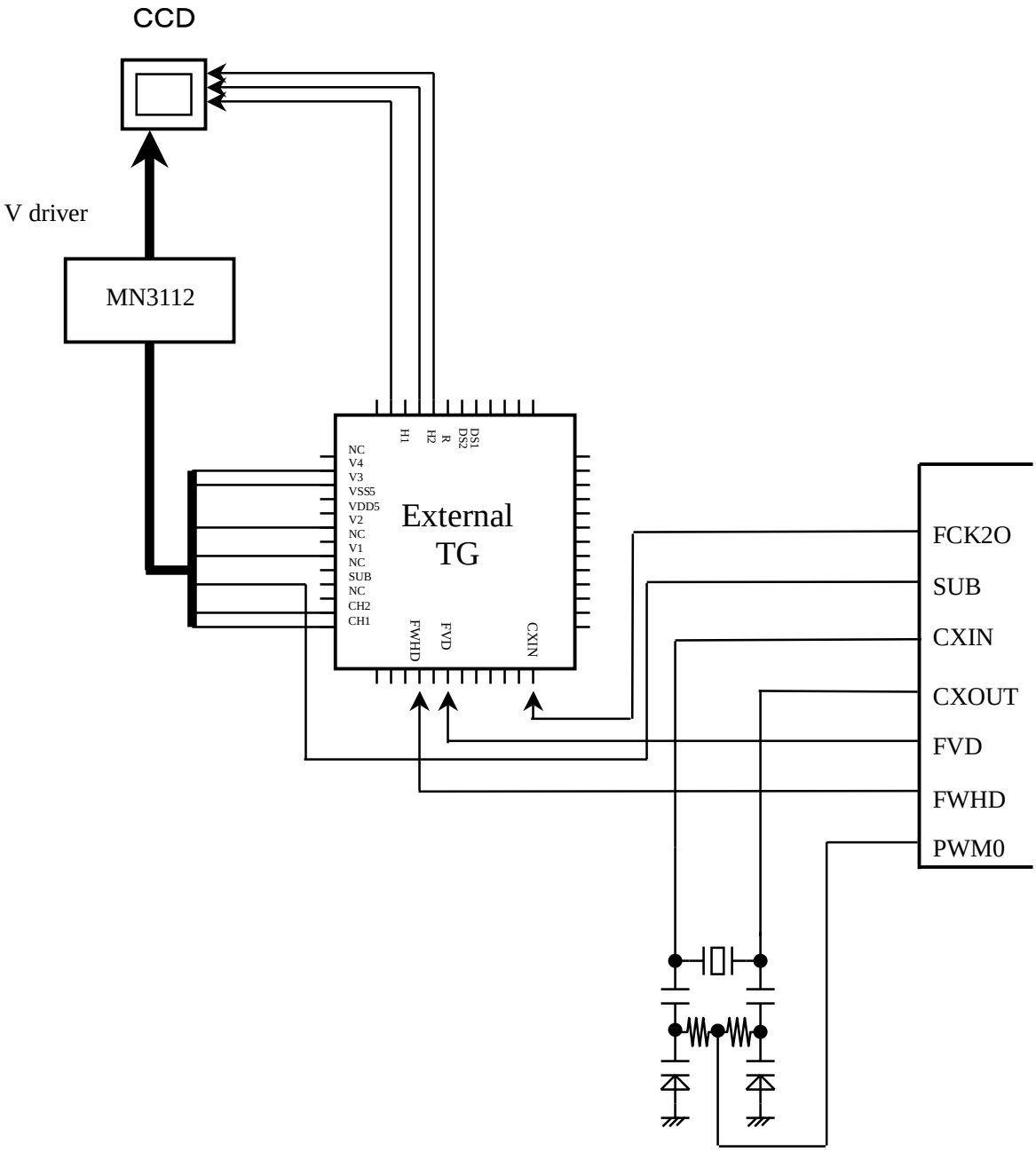


(3) Vehicle mounting mode

For HD/VD synchronization or SYNC synchronization, the horizontal phase can be varied by the internal register setting. Variation of the horizontal phase acts on both the composite output and RGB output. The variable range is ±5 µs.



11.7 External TG mode



To drive a CCD not supported by the MN673276, the external TG mode can be used. Set bit 7 of the address C4 of the register to “H”.
The MN673276 supplies FCK2O, FWHD, and FVD to the external TG. The CCD is driven with the CCD drive pulses except SUB of the external TG.
SUB of the MN673276 must be used. Otherwise, ELC will not operate.

11.8 External synchronization and input pin

Since the logic of the external synchronization input pin to be pulled up or down (depending on the mode) varies as follows, a pull-up/-down resistor is not built in. Set as shown in the table below. The monitor/vehicle mounting mode is switched by the external pin (EXTMOD).

Mode	EXTMOD
Vehicle mounting mode	1
Monitor mode	0

Monitor mode

The external synchronization supports the VD2 synchronization and LL synchronization. The priority is VD2, LL, and INT in order.

Mode	Input signal	Pin setting
EXTIN0	LP	Pull-down
EXTIN1	VD2	Pull-down

(1) VD2 synchronization
When VD2 is input to the EXTIN1 pin, the VD2 synchronization automatically becomes active.

(2) LL synchronization
The internal synchronization/LL synchronization are switched by the external pin (LLDET).
When the LP pulse is input to the EXTIN0 pin with LLDET being “H”, the LL synchronization becomes active.
This LSI does not have an LL-phase variation function as a DSP. An external phase adjustment is necessary by a mono-multivibrator, etc.

Vehicle mounting mode

The external synchronization supports the SYNC synchronization and HD/VD synchronization. The priority is SYNC, HD/VD, and INT in order.

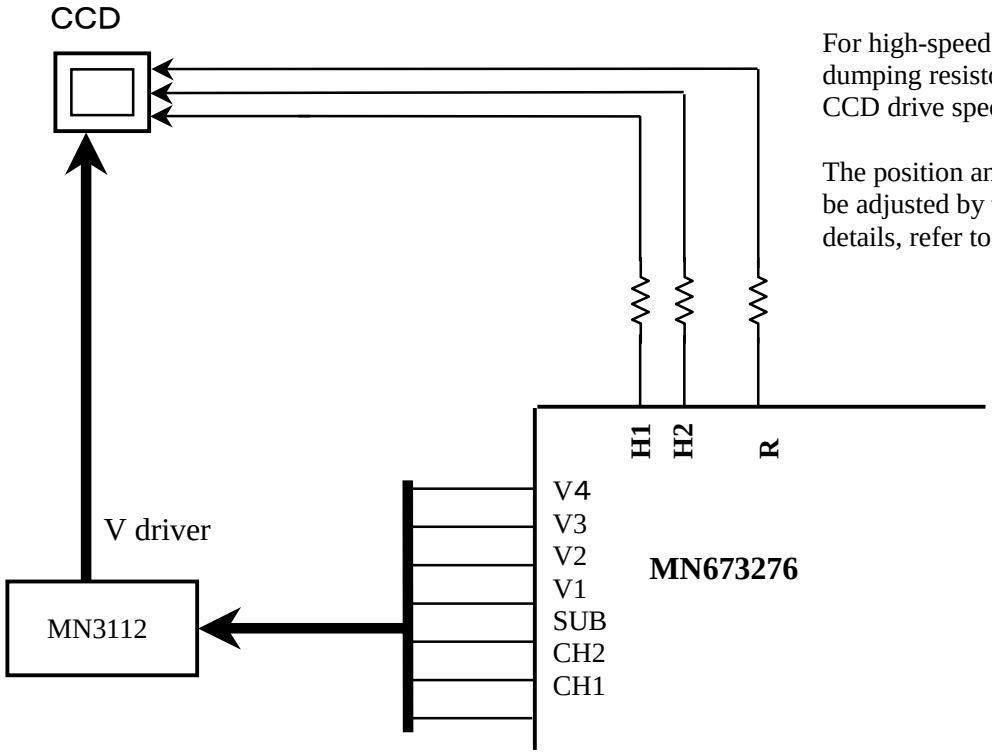
Mode	Input signal	Pin setting
EXTIN0	CSYNC/HD	Pull-up
EXTIN1	VD2	Pull-down

(1) SYNC synchronization
When EXTSYNC is input to the EXTIN0 pin, the SYNC synchronization automatically becomes active.

(2) HD/VD synchronization
When EXTHD is input to the EXTIN0 pin and EXTVD is input to the EXTIN1 pin, the HD/VD synchronization becomes active.

11.9 CCD drive circuit

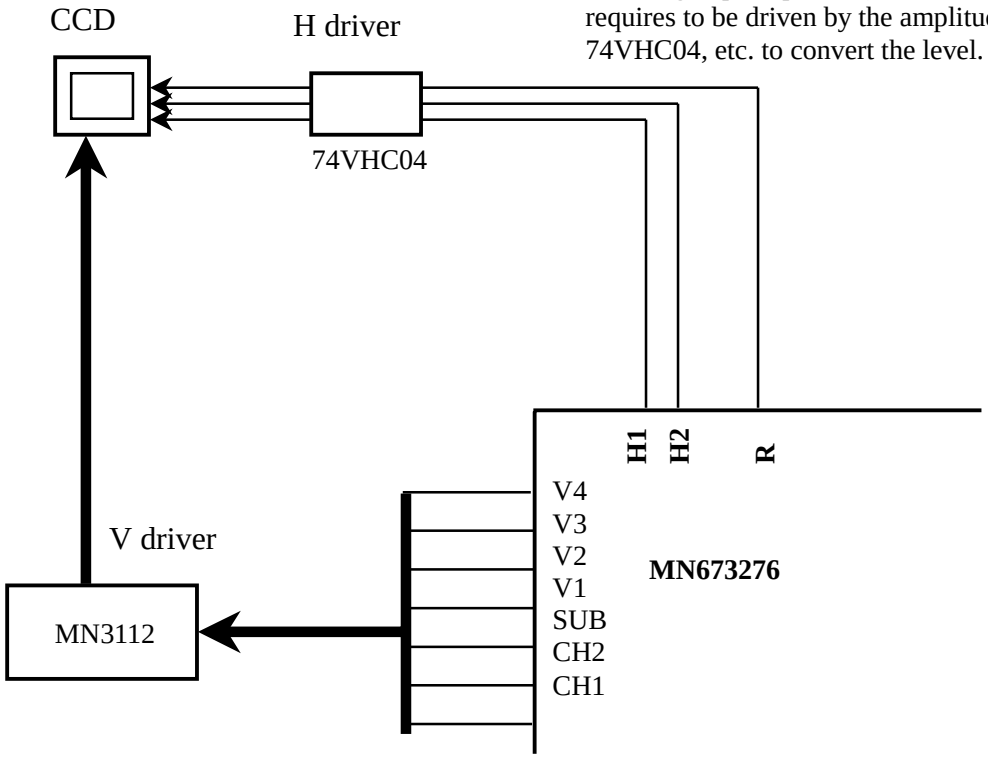
(1) H1, H2 and R, 3.3 V drives



For high-speed pulses, insert a dumping resistor, etc. to meet the CCD drive specifications.

The position and width of the R can be adjusted by the register. For details, refer to the register map.

(2) H1, H2 and R, 5 V drives



If the high-speed pulses (H1, H2 and R) of the CCD requires to be driven by the amplitude of 5 V, use 74VHC04, etc. to convert the level.

11.10 Mode setting pin

The mode setting pin is logically fixed to reduce the number of externally fitted components supposing that this LSI is used for PC or vehicle mounting, or to realize a frequently used state.

Pin name	Logic	Description
NYPL	L	NTSC system
FLC	H	Flicker correction ON
EXTMOD	H	Vehicle mounting mode (HD or VD/SYNC synchronization mode)
SCANT	L	Normal operation

L: pull-down, H: pull-up

11.11 External control signal

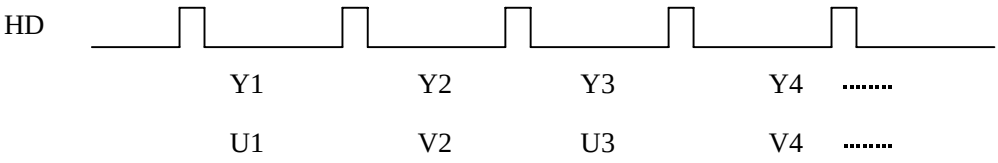
Six types of input pins are provided to allow the functions of the LSI to be controlled externally. These controls can also be switched by I2C.

Pin name	Description		
LLDET	Switching internal synchronization/LL synchronization L: internal synchronization	H: LL synchronization	
ALCELC	Switching mechanical iris fixed/ELC L: ELC	H: mechanical iris fixed	
ATWLOCK	Stopping ATW	L: normal	H: ATWLOCK
APGAIN	Switching aperture gain	L: sharp	H: soft (APGAIN=0)
BLCSW	Switching target value	L: normal	H: Switches target value
REV	Executing left-right reverse	L: normal	H: reversed

11.12 Output specifications

Supports the following analog outputs. No digital output is provided.

- Composite output
- YC separated outputs
- RGB outputs
- Y/UV outputs (U and V are alternately output every 1H as shown below.)

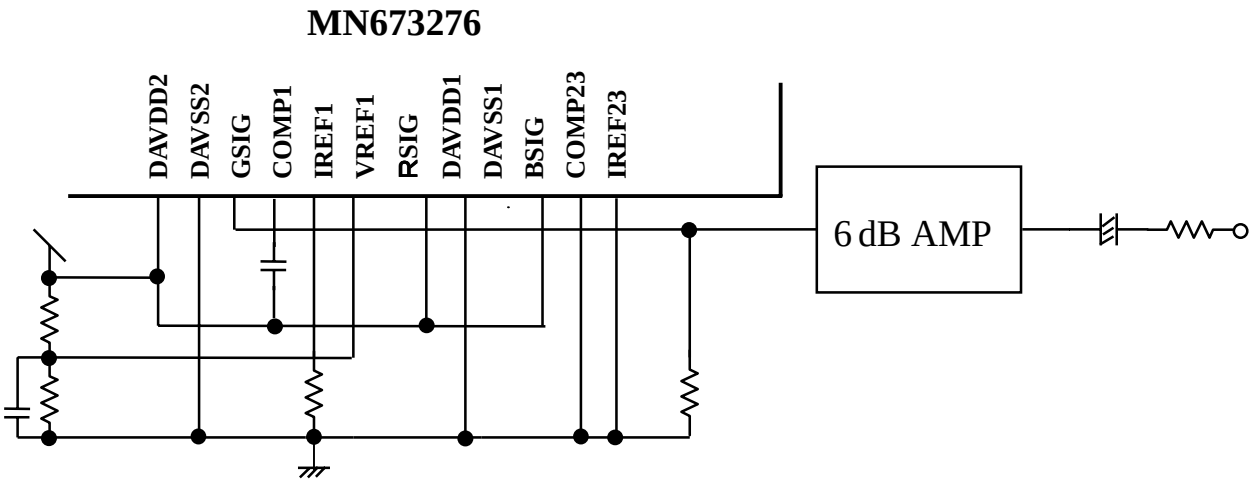


11.13 Signal processing back-end circuit

Setting the register carries out the output mode switching.

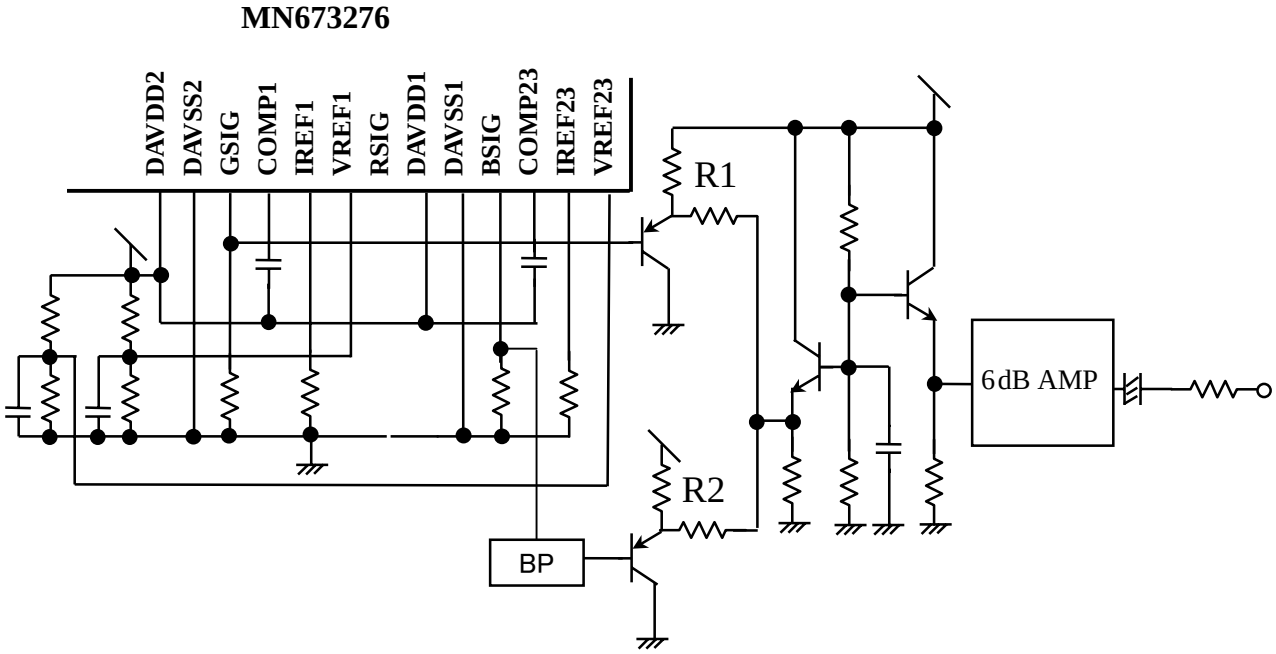
(1) Composite output

The modulated color signal does not pass a BPF to reduce the number of components nor form a typical sine wave. If a certain level of signal quality is required, then provide a BPF in the C block using the YC output mode shown below.



Note) If a D/A converter is not used, set COMP23 = Vdd and IREF23 = VREF23 = 0.

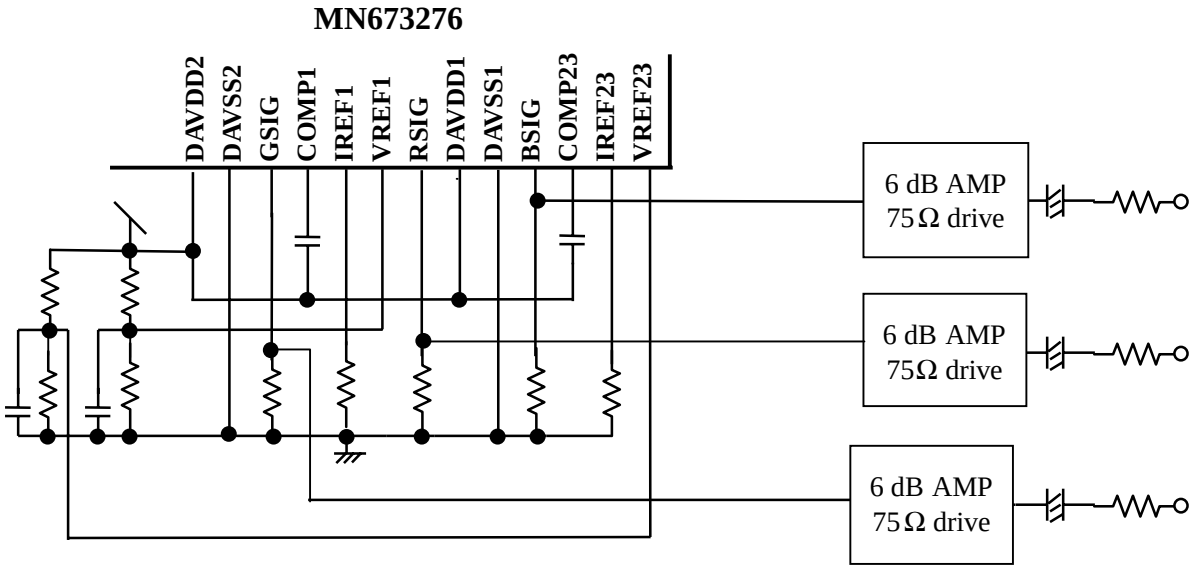
(2) YC output



The YC output can be adjusted (±5T) by the register WE17h.

Register 17 ---- **** YCDSEL YC phase adjustment

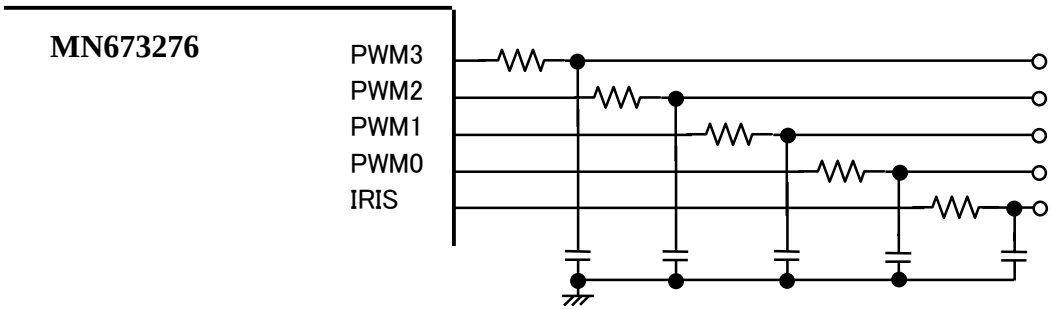
(3) RGB



Note) With regard to (1), (2), and (3) above, if the high-bright part of the video signal is clipped due to the register setting or the dynamic range of the output amplifier, the density of each line of the color signal may be inconsistent.

11.14 External PWM output

Five PWM outputs are provided. They can be used for any purpose, including the adjustment of the oscillation frequency.
Since the output voltages of the PWM outputs depend on VDD (digital power supply voltage), care should be taken in the design of the power supply if accuracy is required for the output voltages.



Example of application)

PWM0	(Internal synchronization/frequency adjustment for SC block in the LL mode)
PWM1	(DAC1 gain)
PWM2	(DAC2 and DAC3 gains)
PWM3	Free
IRIS	ALCDC adjustment

11.15 Control block

Aperture control

The aperture is controlled by a combination of electronic shutter controls and digital AGC.

(1) High-speed mode
A high-speed mode is provided so that the target value is attained at power-ON.
Note that the high-speed mode is activated only for a certain period immediately after the power is turned ON. (Register variable range: 1 s max.)
The response speed in the high-speed mode is switched by 1 V/3 V.

(2) Mechanical iris control
The MN673276 is not provided with a mechanical iris control function but is provided with PWM output to adjust DC. An external circuit detecting the CDS output signal performs the iris control.

(3) Flicker correction
A flicker correction function with a 3-V averaging method is provided. Refer to ADR15 in the description of registers.

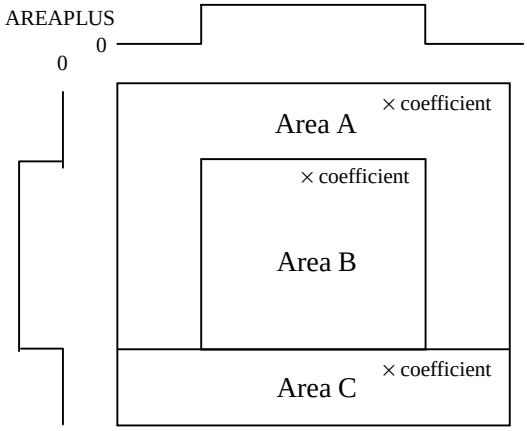
(4) Maximum ELC speed
Settable between 1/60 s and 1/100000 s. The maximum value can be varied by a register.

(5) Backlight correction

To enable metering with a backlight taken into consideration, the target value switching, weighting coefficient switching, and frame pulse output are available in an interlock with the backlight correction SW (BLCSW).

[Specifications of a frame pulse]

When BLC is ON, a frame pulse (AREAPULS) is output which becomes “H” only for the central area. This allows the ALC (Galvano lens) control to be performed only with the brightness information obtained in the central area. This is beneficial in the backlight condition.



As the above frame pulse alone is not effective in the ELC mode or in the AGC area, the weighting coefficient can be varied with BLC-ON. (x 0.5, x 0.6, x 1, etc.)

BLC	Target value	Weighting	Register	Area	Frame pulse	ALC DC
OFF	Target value 1	Weighting coefficient 1 Weighting coefficient 2 Weighting coefficient 3	67 h 6A h 6C h	A B C	Not output (fixed at H)	Set value 1
ON	Target value 2	Weighting coefficient 4 Weighting coefficient 5 Weighting coefficient 6	68 h 6B h 6D h	A B C	Output	Set value 2

Acts on AGC/ELC control

Acts on ALC (Galvano lens) control

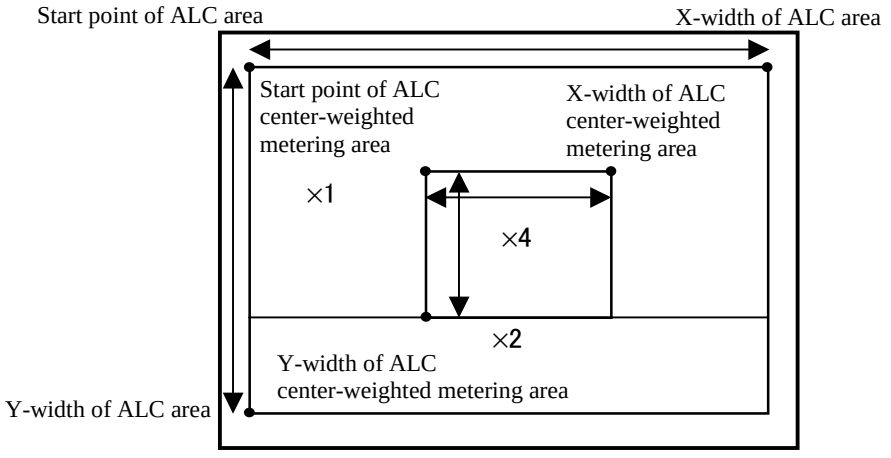
11.16 White balance

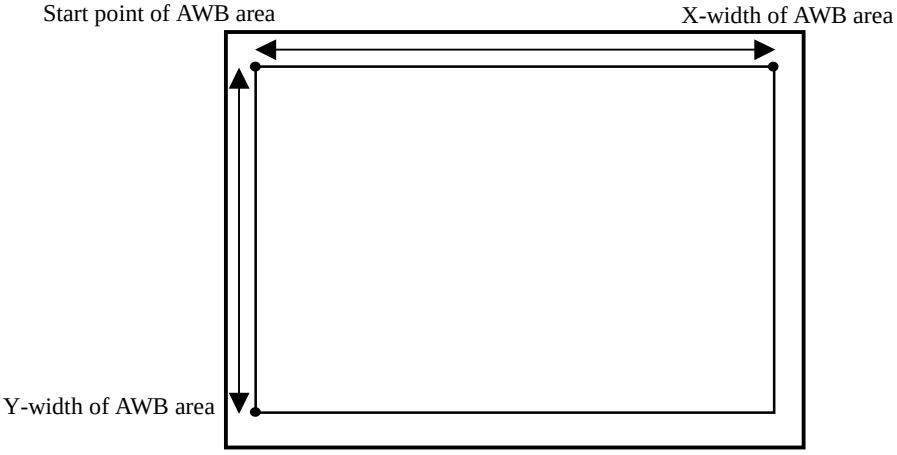
The white balance is determined by the average of an entire screen's data. By processing the average data in 2's complement, the deviance of the increase in AGC gain on white balancing is reduced. By changing the bit expansion of the ATW block from 9 bits to 10 bits, the accuracy of white balance is improved.
(Major functions)

- There are two modes: ATW and MANUAL. The mode is set by a register.
- In the ATW mode, a limiter value for high color temperature/low color temperature can be set.
- In the ATW mode, a LOCK function is provided. Setting the external pin ATWLOCK fixes the white balance. For example, when shining a light source on a piece of white paper and setting ATWLOCK after the ATW takes the data, the white balance is set.
- In the MANUAL mode, a value is set in the internal register.
- In the ATW mode, a high-speed mode is provided so that white balance converges at the moment of power-ON. Note that the high-speed mode is activated only for a certain period immediately after the power is turned ON. (Register variable)
- The response speed in the high-speed mode is the maximum speed (or less) settable by the MN673276.
- The ULI function provided stops ATW in the high-brightness mode.

Note) Suppose that the camera set (LSI) is shut down with ULI in operation after ATW is locked. The next time the camera is turned ON, the colors may vary because the information of white balance was not retained.

ALC (aperture control)/AWB (white balance) metering area
Settable values for the area are limited. Refer to the register map for details.



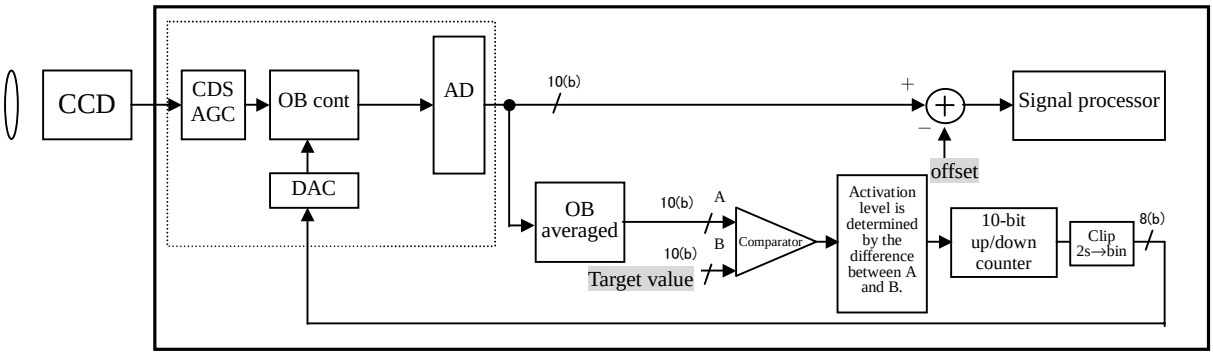


11.17 OB control

The OB control consists of an analog and a digital controls.
The analog control is the method in which the clamping voltage for the analog CDS/AGC is controlled so that the OB level detected internally by this LSI remains constant.
The digital control is the method in which the signal level within the LSI is controlled so that the OB level detected internally by this LSI remains constant.

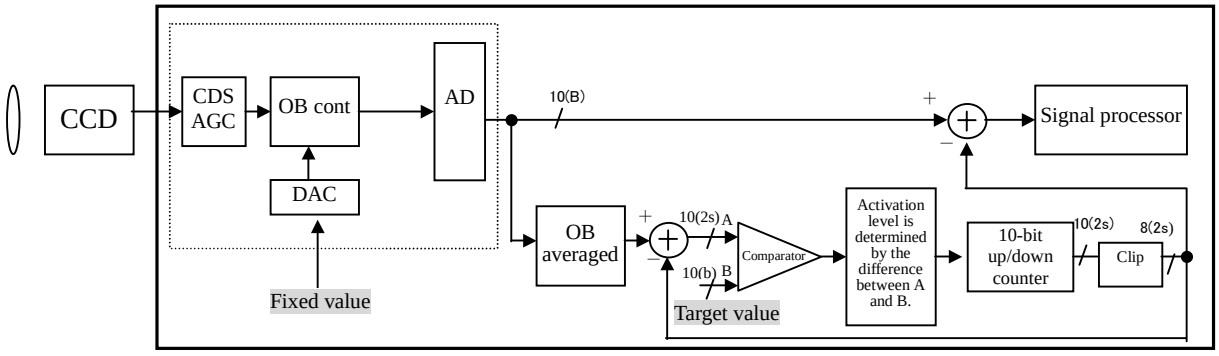
Analog OB control

MN673276



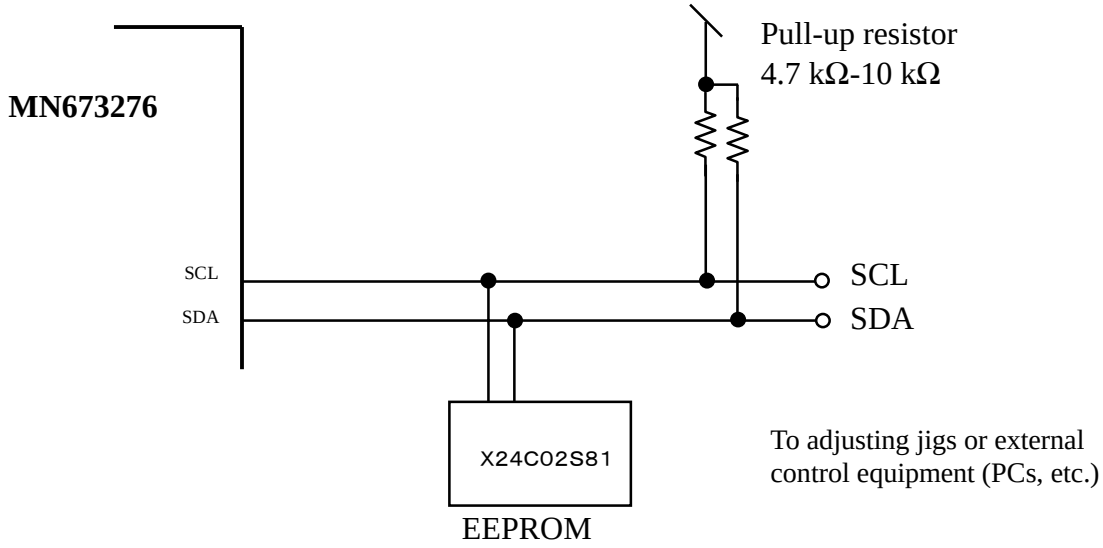
Digital OB contorol

MN673276



11.18 External interface

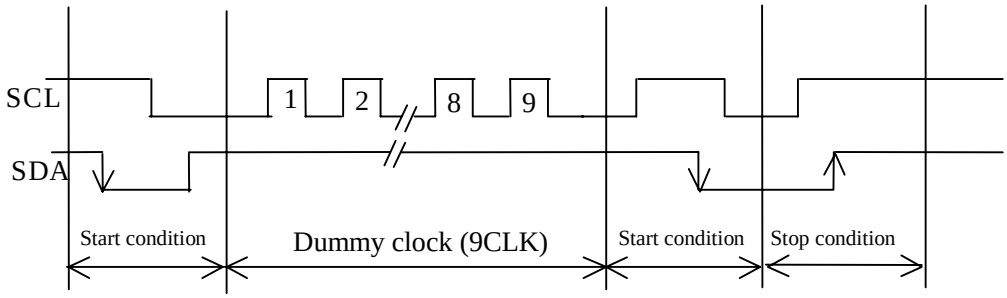
The I2C interface is used to connect the external control of the MN673276 with the EEPROM for storage of the register value used for adjustment.



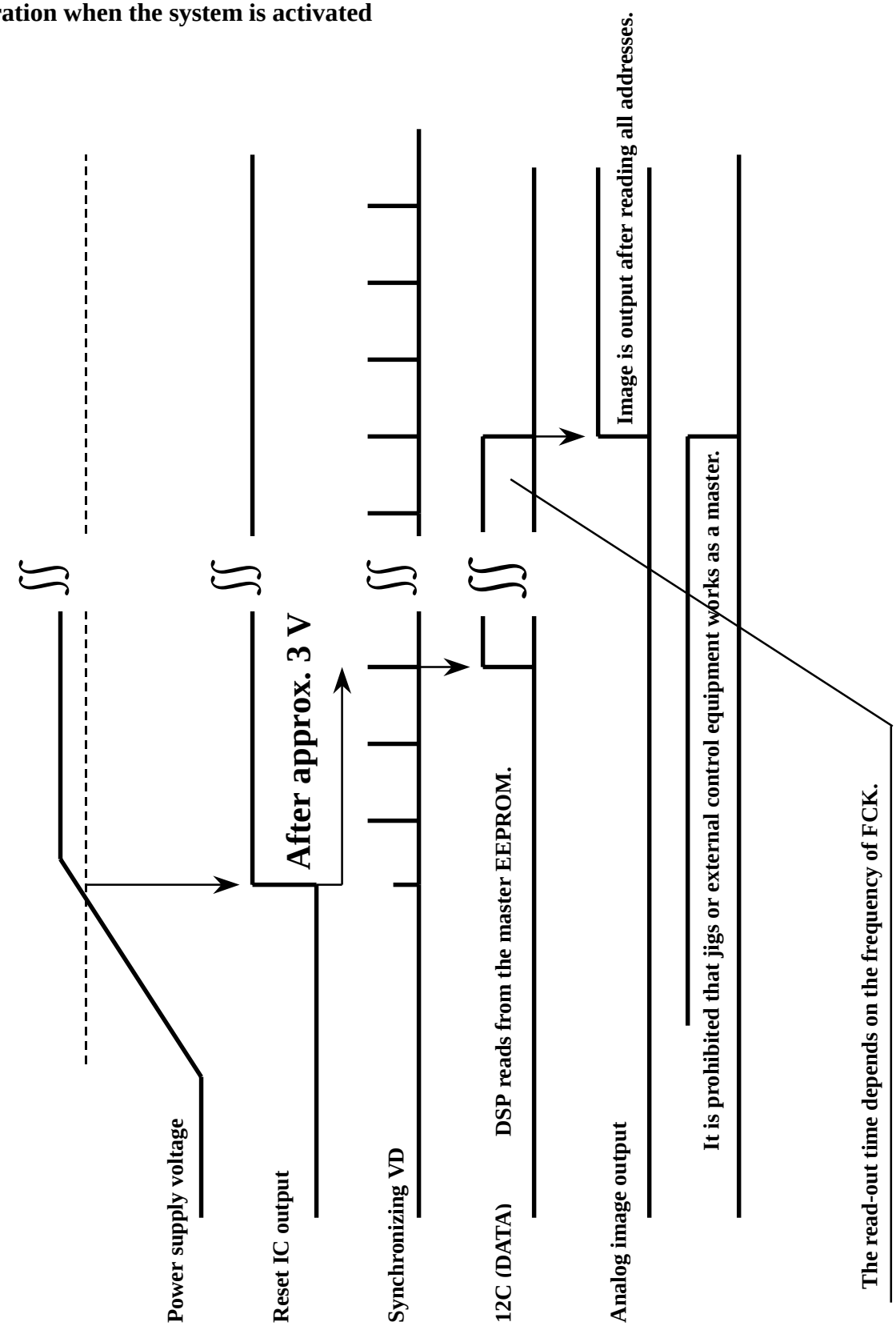
- The I2C control modes supported by the MN673276 are as follows.
  At power-ON: Sequential read (random read) of all addresses (256 bytes) of the EEPROM
  Others: Random read and byte-order write
- Concerning mode

	DSP	EEPROM	Adjusting PC
At activation	MR, Master Receiver	ST, Slave Transmitter	×
While adjusting	SR, Slave Receiver	×	MT, Master Transmitter
While adjusting and writing	×	SR, Slave Receiver	MT, Master Transmitter
At RST after adjustment	MR, Master Receiver	ST, Slave Transmitter	×

- The slave address of the EEPROM is 55h and that of the MN673276 is fixed at 2Ah. The adjusting PC, etc. may change the slave address of the MN673276 after activation but it is not retained in the EEPROM.
- Since SCL is generated by the system clock with a fixed frequency dividing ratio, it is 100 kHz for 768 pixels. However, SCL will become slower when a 510-pixel CCD is used.
- Before reading the data in the EEPROM when the power is turned ON, it is necessary to execute the following initialization sequence to initialize the EEPROM.



Operation when the system is activated



12. CCD Drive/Synchronization Mode

		510H NTSC	510H PAL	510H PAL	768H NTSC	768H PAL
CCD supported		MN37110	MN37210	MN37213	MN37140	MN37241
FCK		606fH	618fH	606fH	910fH	908fH
External pin setting	CCDSEL2	0	0	0	1	1
	CCDSEL1	0	0	1	0	0
	CCDSEL0	0	0	1	0	0
	NTPL	0	1	1	0	1
Internal pin setting	VCOC DEh: DDh	C036h	EB15h	EFBDh	8000h	A000h
	VCOH E0h: DFh	C08Eh	EB54h	EE94h	8000h	A1A3h
	VCOC E2h: E1h	C08Eh	EC61h	EFA1h	8000h	A2B0h
	AWB area setting	The setting values in the register WE80 to 84 for AWB and WE40 to 44 for ALC depending on the mode.				
	ALC area setting					
Synchronization	Internal synchronization	○	○	○	○	○
	HD and VD synchronization	○	○	○	○	○
	VD2 and LL synchronization	○	○	○	○	○
Output	Composite	○	○	○	○	○
	YC separation	○	○	○	○	○
	RGB	○	○	○	○	○
	YUV time-division multiplex	○	○	○	○	○

All corresponding color filters for the CCD support complementary colors, as well as black and white elements.