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INTEGRATED CIRCUITS

OBJECTIVE DEVICE SPECIFICATION

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TDA8932

2x15W class D Power Amplifier

Confidential

Objective Device Specification

Date: Sept 13, 2005
Version: 1.7
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Philips Semiconductors

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Change history		
1.0	22-sep-04	Initial version
1.1	21-oct-04	Updated after feedback design team
1.2	17-nov-04	Redefinition of TDA8932: 1xBTL or 2xSE
1.3	24-nov-04	Updated after feedback design team
1.4	13-Dec-04	Updated after feedback customer
1.5	8-April-05	Updated with new pinning
1.6	7-July-05	Updated with test results and pin configuration
1.7	13-Sept-05	General update

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 FEATURES

- High efficiency
- Application without heatsink using thermally enhanced small outline package
- Operating voltage from 10V to 36V asymmetrical or +/-5V to +/-18V symmetrical
- Thermally protected
- Thermal foldback
- Full short circuit proof across load and to supply lines (using advanced current protection)
- Switchable internal / external oscillator (master-slave setting)
- No pop noise
- Low quiescent current
- Low sleep current
- Mono bridged tied load (full bridge) or stereo single ended (half bridge) application
- Full differential inputs

2 APPLICATIONS

- Television sets CRT/LCD/plasma TV/projection TV
- Monitors

3 GENERAL DESCRIPTION

The TDA8932 is a high efficiency class-D amplifier with low dissipation.
The maximum output power is 2x25W in stereo half-bridge application (Rl=4 ohm) or 1x50W in mono full bridge application (Rl=8 ohm). Due to the high efficiency the device can be used without any external heat sink when playing music. If proper cooling via the PCB is implemented, a continuous output power of 2 x 15W is feasible. Due to the implementation of thermal foldback even for high supply voltages and/or lower load impedances the device can be operated with considerable music output power without the need for an external heat sink.
The device has two full differential inputs driving four integrated power switches, combined in two independent outputs. It can be used as mono full bridge (BTL) or as stereo half bridge (SE).

4 QUICK REFERENCE DATA

Table 1: Quick reference data

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
General; Vp=29V						
V_p	Operating supply voltage		10	29	36	V
I_{sleep}	Sleep current	$V_{power\ up}$ < 0.8 V V_{engage} < 0.8 V		80		μA
I_p	Quiescent current	Without load, snubbers, output filter		20		mA
Stereo SE channel						
P_{outSE}	Continuous-time RMS Output power per channel	RL= 4Ω; THD = 10% Vp=22V	14	15		W
		RL= 8Ω; THD = 10% Vp=29V	14	15		W
	Peak output power (short-time)	RL= 4Ω; THD = 10% Vp=29V	23	25		W
Mono BTL channel						
P_{outBTL}	Continuous RMS Output power	RL= 8Ω; THD = 10% Vp=22V	28	30		W
		RL= 4Ω; THD = 10% Vp=12V	14	15		W
	Peak output power (short-time)	RL= 8Ω; THD = 10% Vp=29V	48	50		W

5 ORDERING INFORMATION

Table 2: Ordering information

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8932T	SO32	Plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

6 BLOCKDIAGRAM

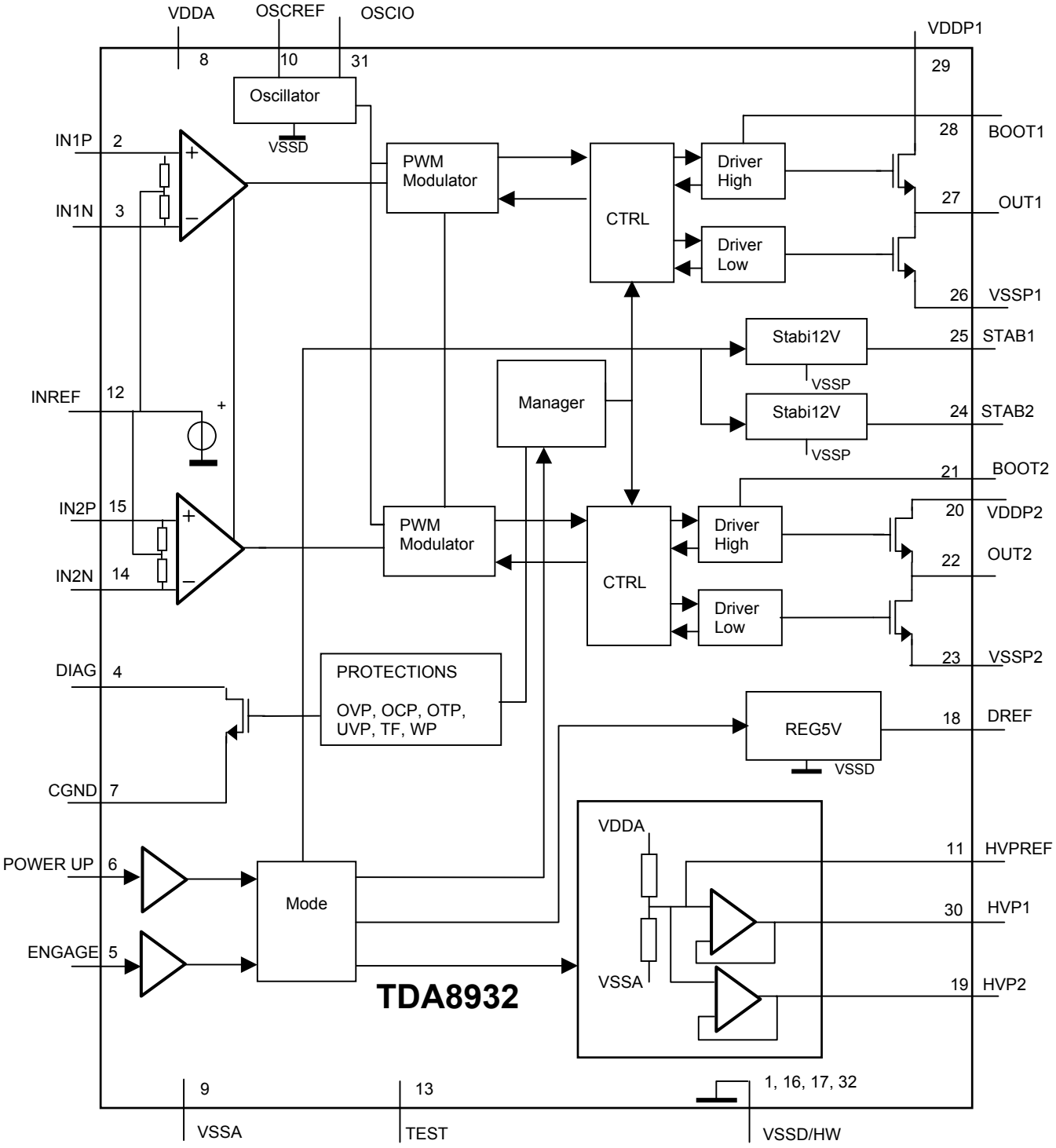


Figure 1: Block diagram

7 PINNING INFORMATION

7.1 Pinning

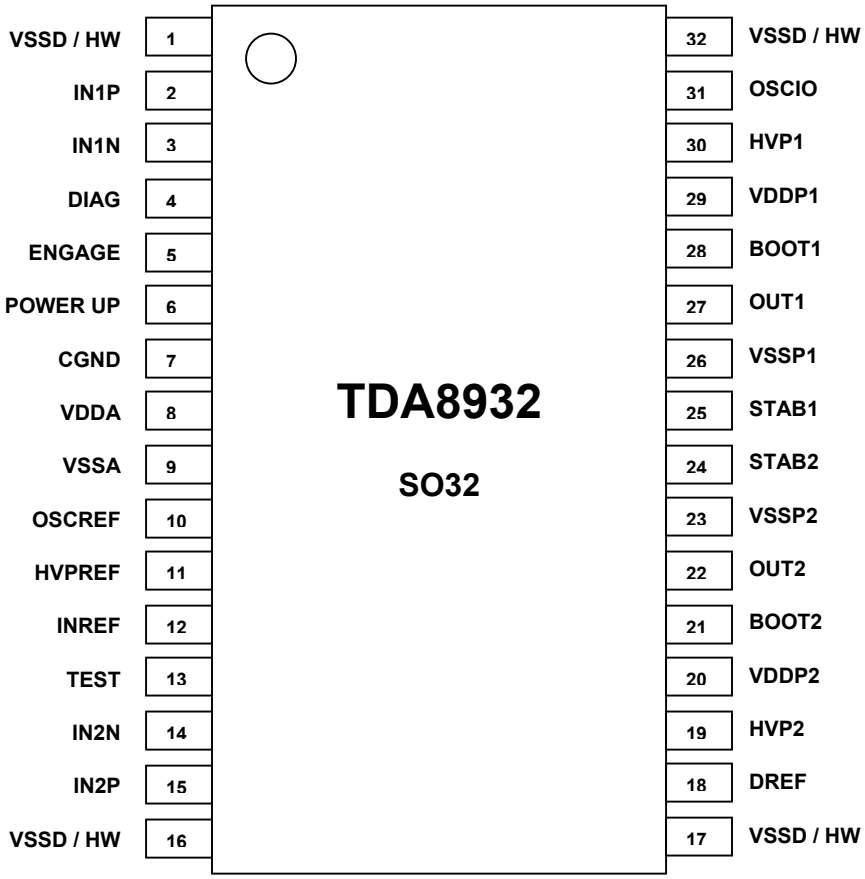


Figure 2: Pin configuration

7.2 Pin description

Table 3: Pinning description

Pin name	Pin no.	Description
VSSD / HW	1	Negative digital supply voltage and handle wafer connection
IN1P	2	Positive audio input for channel 1
IN1N	3	Negative audio input for channel 1
DIAG	4	(Open-drain) diagnostic output
ENGAGE	5	Engage input; switch between mute and operating mode
POWER UP	6	Power up input; switch between sleep and mute mode
CGND	7	Control ground; reference for POWER UP, ENGAGE, DIAG
VDDA	8	Positive analog supply voltage
VSSA	9	Negative analog supply voltage
OSCREF	10	Master/slave setting oscillator. Set internal oscillator frequency (only master-setting)
HVPREF	11	Decoupling for internal half supply voltage reference
INREF	12	Decoupling for input reference voltage
TEST	13	Test signal input; for testing purpose only
IN2N	14	Negative audio input for channel 2
IN2P	15	Positive audio input for channel 2
VSSD / HW	16	Negative digital supply voltage and handle wafer connection
VSSD / HW	17	Negative digital supply voltage and handle wafer connection
DREF	18	Decoupling internal 5V regulator for logic supply
HVP2	19	Half supply voltage output for charging single-ended capacitor for channel 2
VDDP2	20	Positive power supply voltage for channel 2
BOOT2	21	Bootstrap capacitor for channel 2
OUT2	22	PWM output channel 2
VSSP2	23	Negative power supply voltage for channel 2
STAB2	24	Decoupling internal 12V regulator for the drivers channel 2
STAB1	25	Decoupling internal 12V regulator for the drivers channel 1
VSSP1	26	Negative power supply voltage for channel 1
OUT1	27	PWM output channel 1
BOOT1	28	Bootstrap capacitor for channel 1
VDDP1	29	Positive power supply voltage for channel 1
HVP1	30	Half supply voltage output for charging single-ended capacitor for channel 1
OSCIO	31	Input/output for external oscillator (slave-setting)
VSSD / HW	32	Negative digital supply voltage and handle wafer connection

8 FUNCTIONAL DESCRIPTION

8.1 General

The TDA8932 is a mono full bridge (BTL) or stereo half bridge (SE) audio power amplifier using class-D technology. The audio input signal is converted into a Pulse Width Modulated (PWM) signal via an analog input stage and PWM modulator. To enable the output power DMOS transistors to be driven, this digital PWM signal is applied to a control and handshake block and driver circuits for both the high side and low side. A 2nd-order low-pass filter converts the PWM signal to an analog audio signal across the loudspeakers.

The TDA8932 contains two independent half bridges with full differential input stages. The loudspeakers can be connected in the following configurations:

- Mono full bridge (Bridge-Tied Load, BTL)
- Stereo half-bridge (Single-Ended, SE)

The TDA8932 contains common circuits to both channels such as the oscillator, all reference sources, the mode functionality and a digital timing manager. The following protections are built-in: thermal fold back, temperature, current and voltage protections.

8.2 Mode selection / interfacing

The TDA8932 can be switched in three operating modes via POWER UP and ENGAGE inputs:

- Sleep mode; with a very low supply current
- Mute mode; the amplifiers are switching idle (50% duty cycle), but the audio signal at the output is suppressed by disabling the VI-converter input stages. In this mode the reference currents and voltages are present. The HVP capacitors have been charged to half the supply voltage (asymmetrical supply only).
- Operating mode; the amplifiers are fully operational with output signal.

Both pins POWER UP and ENGAGE refer to pin CGND.
In the table 4 below the different modes are given as function of the voltages on the POWER UP and ENGAGE pins.

Mode selection	POWER UP	ENGAGE
Sleep	$V_{power\ up}$< 0.8 V	X (don't care)
Mute	2 V < $V_{power\ up}$ < 6.5 V Note1	V_{engage}< 0.8 V Note1
Operating	2 V < $V_{power\ up}$ < 6.5 V Note1	3 V < V_{engage} < 6.5 V Note1

Table 4: Mode selection TDA8932

Note 1 in case of symmetrical supply conditions the voltage applied on the POWER UP and ENGAGE inputs must never exceed the supply voltage VDDx

If the transition between mute and operating mode is controlled via a time-constant, the start-up will be pop-free since the DC output offset voltage is applied gradually to the output between mute mode and operating mode. The bias current setting of the VI converters is related to the voltage on the ENGAGE pin; in mute mode the bias current setting of the VI converters is zero (VI converters disabled) and in operating mode the bias current is at maximum.
The time constant required to apply the DC output offset voltage gradually between mute and operating can be generated by applying a decoupling capacitor on the ENGAGE pin.
The value of the time-constant should be dimensioned for 500 ms using a capacitor of 1μF on the ENGAGE pin.

8.3 Pulse width modulation frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approximately 320 kHz. Using a 2nd-order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. The PWM switching frequency can be set by an external resistor R_{osc} connected between pin OSCREF and V_{SSD}. The carrier frequency can be set between 300 kHz and 500 kHz. Using an external resistor of 39kΩ on the OSCREF pin, the carrier frequency is set to an optimized value of 320 kHz.
If two or more TDA8932 devices are used in the same audio application, it is recommended to synchronize the switching frequency of all devices. This is described in chapter 17.4 External Clock.

8.4 Protections

The following protections are included in TDA8932:

- Thermal foldback (TF)
- Over temperature protection (OTP)
- Over current protection (OCP)
- Window protection (WP)
- Supply voltage protections
  - Under voltage protection (UVP)
  - Over voltage protection (OVP)
  - Un Balance Protection (UBP)

The reaction of the device on the different fault conditions differs per protection and is described in the following sections.

8.4.1 Thermal foldback

If the junction temperature Tj > 140 ^{0}C, then the gain is gradually reduced resulting in a smaller output signal and less dissipation. At Tj > 150^{0}C the outputs are fully muted.

8.4.2 Over temperature protection (OTP)

If the junction temperature Tj > 160^{0}C, then the power stage will shut down immediately.

8.4.3 Over current protection (OCP)

When the loudspeaker terminals are short-circuited or if one of the demodulated outputs of the amplifier is short-circuited to one of the supply lines, this will be detected by the over current protection (OCP).

If the output current exceeds the maximum output current of 4A, this current will be limited by the amplifier to 4A while the amplifier outputs remain switching (the amplifier is NOT shut-down completely).

The amplifier can distinguish between an impedance drop of the loudspeaker and low-ohmic short across the load or to one of the supply lines. This impedance threshold (Z_{th}) depends on the supply voltage used.

When a short is made across the load causing the impedance to drop below the threshold level (<Zth) the audio amplifier is switched off completely and after a time of 100ms it will try to restart again. If the short circuit condition is still present after this time this cycle will be repeated. The average dissipation will be low because of this low duty cycle.
A short to one of the supply lines will trigger the over current protection (OCP) and the amplifier will be shut down. During restart the window protection will be activated. As a result the amplifier will not start-up after 100ms until the short to the supply lines is removed.

In case of impedance drop (e.g. due to dynamic behavior of the loudspeaker) the same protection will be activated; the maximum output current is again limited to 4A, but the amplifier will NOT switch-off completely (thus preventing audio holes from occurring). Result will be a clipping output signal without any artifacts.

8.4.4 Window protection (WP)

The window protection (WP) checks the PWM output voltage before switching from sleep to mute mode (outputs switching) and is activated:

- During the start-up sequence, when pin POWER UP is switched from sleep to mute. In the event of a short-circuit at one of the output terminals to V_{DD} or V_{ss} the start-up procedure is interrupted and the TDA8932 waits for open-circuit outputs. Because the check is done before enabling the power stages, no large currents will flow in the event of a short-circuit.

- When the amplifier is completely shut-down due to activation of the over current protection (OCP) because a short to one of the supply lines is made, then during restart (after 100ms) the window protection will be activated. As a result the amplifier will not start-up until the short to the supply lines is removed.

8.4.5 Supply voltage protections

If the supply voltage drops below 10V, the under voltage protection circuit (UVP) is activated and the system will shut down correctly. If the internal clock is used, this switch-off will be silent and without pop noise. When the supply voltage rises above the threshold level, the system is restarted again after 100 ms.
If the supply voltage exceeds 36V the over voltage protection circuit (OVP) is activated and the power stages will shut down. It is re-enabled as soon as the supply voltage drops below the threshold level. So in this case no timer of 100ms is started.
Note that supply voltages above the maximum voltage of 40V may damage the TDA8932. Two conditions should be distinguished:
1. If the supply voltage is pumped to higher values by the TDA8932 application itself (see also section 17.6), the OVP is triggered and the TDA8932 is shutdown. The supply voltage will decrease and the TDA8932 is protected against any overstress.
2. If a supply voltage > 40V is caused by other/external causes than the TDA8932 will shut down, but the device can still be damaged since the supply voltage will remain > 40V in this case. The OVP protection is not a supply clamp.

An additional Un Balance Protection (UBP) circuit compares the positive analog (VDDA) and the negative analog (VSSA) supply voltage and is triggered if the voltage difference between them exceeds a certain level. This level depends on the sum of both supply voltages. An expression for the unbalance threshold level is as follows:
$V_{th(ubp)} \approx 0.25 \times (V_{DDA} + V_{SSA})$

In table 5 below an overview is given of all protections and the effect on the output signal

Protection name	Complete shut-down	Restart when fault is removed	Restart every 100ms	DIAG active LOW minimal 50ms
Thermal foldback (TF)	N	Y[3)]	N	N
Over temperature protection (OTP)	Y	N	Y	Y
Over current protection (OCP)	N[1)]	Y[1)]	N[1)]	Y[1)]
Window protection (WP)	Y[2)]	Y	N	Y
Under voltage protection (UVP)	Y	N	Y	Y
Over voltage protection (OVP)	Y	N	Y	Y
Un Balance Protection (UBP)	Y	N	Y	Y

Table 5: Overview protections TDA8932

Notes:
1. Only complete shutdown of amplifier if short-circuit impedance is below the threshold of TBF. In all other cases current limiting: resulting in clipping output signal.
2. Fault condition detected during (every) transition between sleep-to-mute and during restart after activation of OCP (short to one of the supply lines)
3. Amplifier gain will depend on junction temperature and heat sink size.

8.5 Diagnostic Output

Whenever one of the protections is triggered except for thermal foldback (TF) as summarized in table 5, the DIAG output is activated low. The diagnostic output signal during different short conditions is illustrated in figure 3. The DIAG pin refers to CGND. An internal reference supply will pull-up the open-drain DIAG output to approximately 2.4V. This internal reference supply can deliver approximately 50μA. Using the DIAG as input a voltage smaller than 0.8V will put the device into sleep mode.

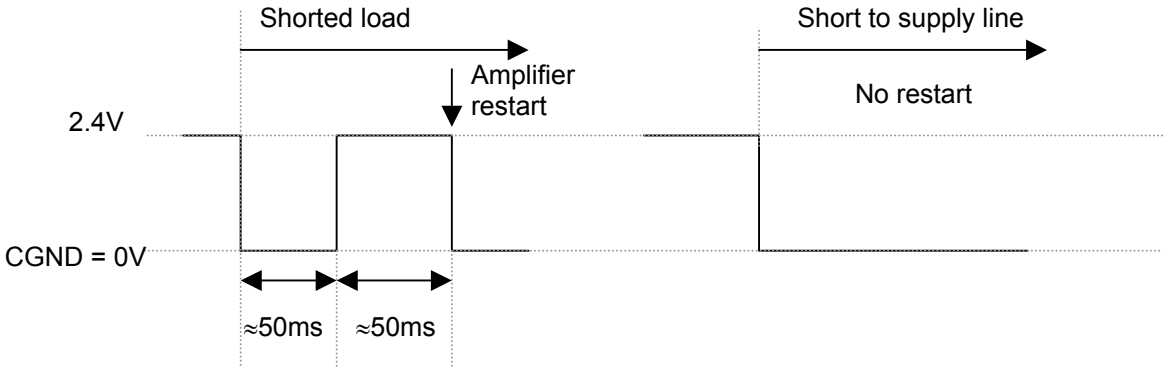


Figure 3: Diagnostic Output for different kind of short circuit conditions.

8.6 Differential inputs

For a high common mode rejection ratio and a maximum of flexibility in the application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the two channels can be inverted, so that a load can be connected between the two sets of output filters. In this case the system operates as a mono BTL amplifier.

The input configuration for a mono BTL application is illustrated in Fig.4.
In single-ended configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies and minimizes supply pumping (see also section 17.6).

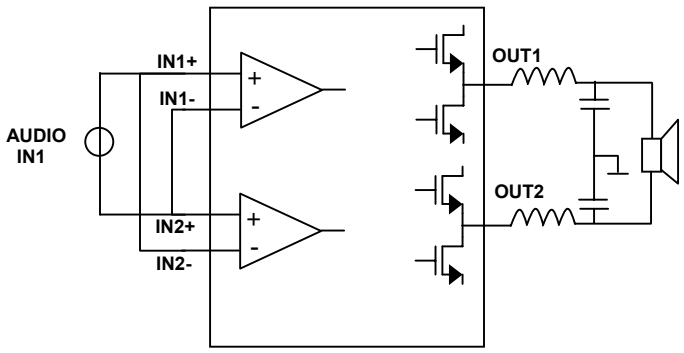


Figure 4: Input configuration for mono BTL application.

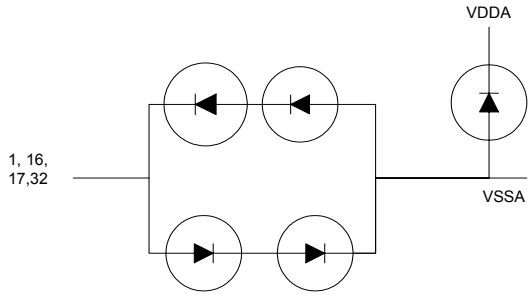
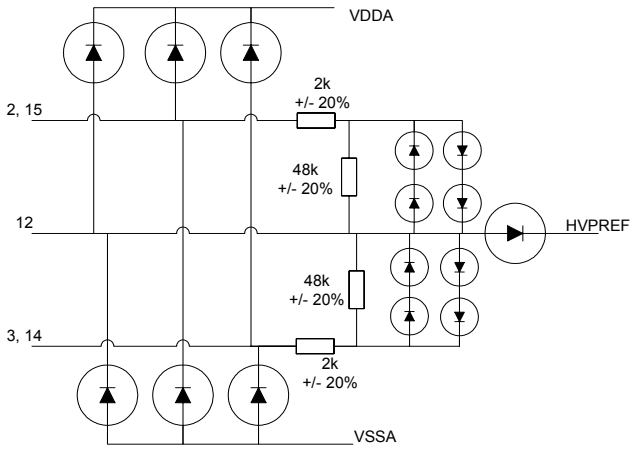
8.7 Half supply voltage output

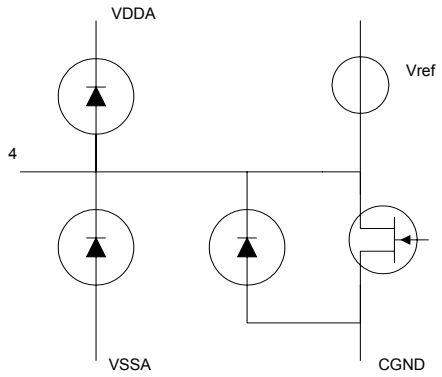
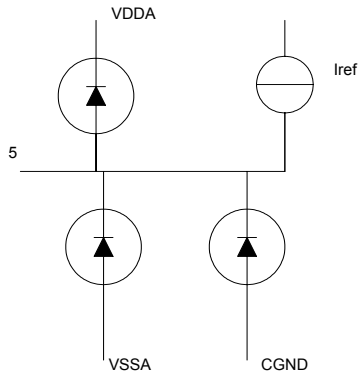
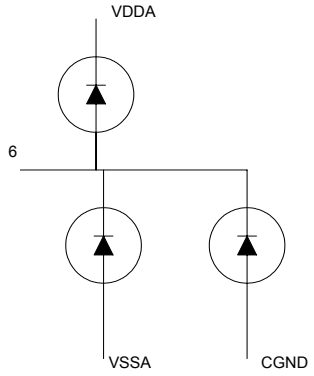
When the POWER UP is high the half supply voltage output charges the Single-Ended capacitor. The start-up will be pop free since the device starts switching when the SE capacitors are completely charged.

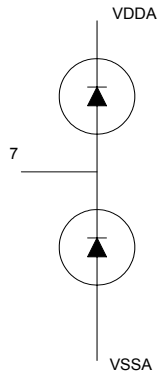
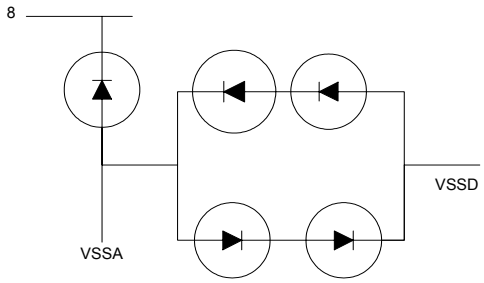
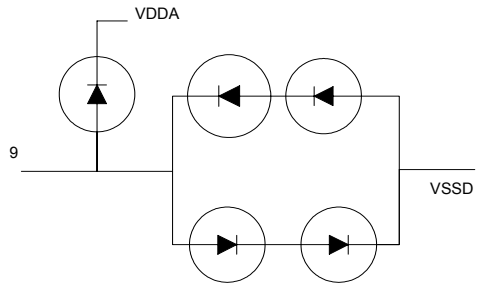
The time required for charging the SE capacitor is depending on its value.

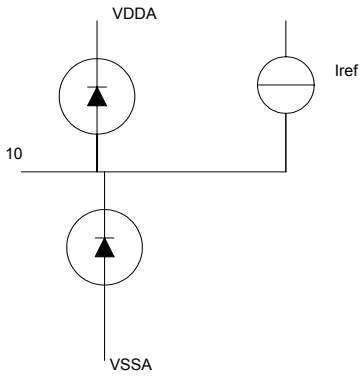
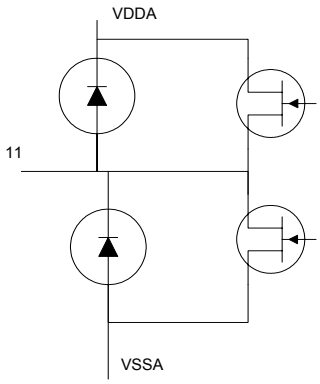
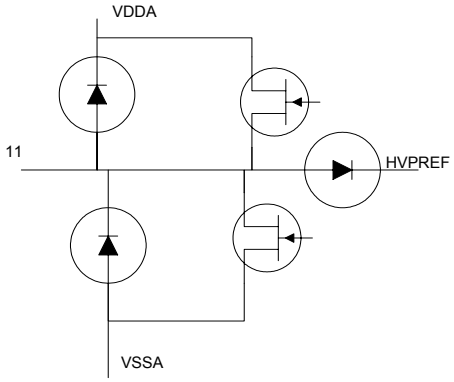
The half supply voltage output is disabled when the TDA8932 is used in combination with a symmetrical supply.

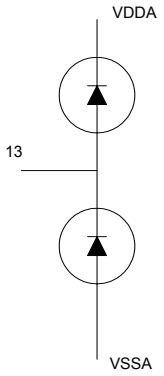
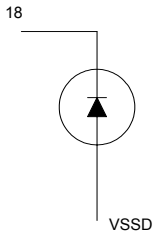
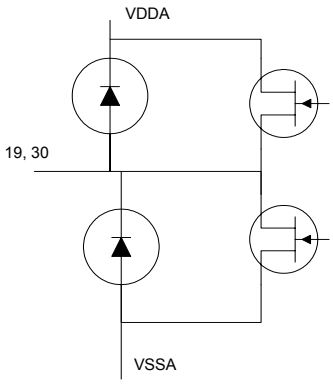
9 INTERNAL CIRCUITRY

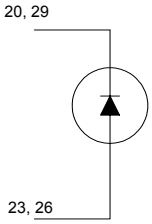
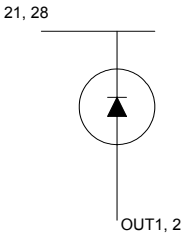
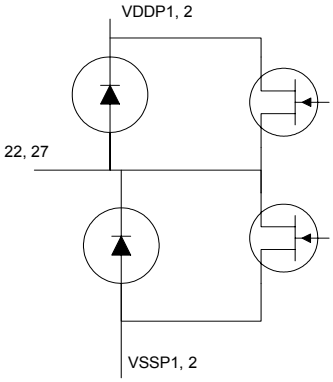
Pin	Symbol	Equivalent circuit
1, 16 17, 32	VSSD/HW	
2, 15 3, 14 12	IN1P, IN2P IN1N, IN2N INREF	

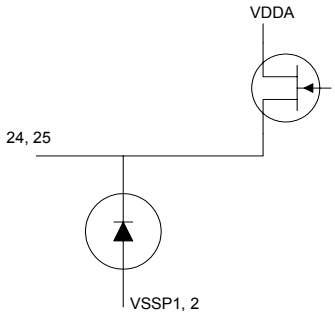
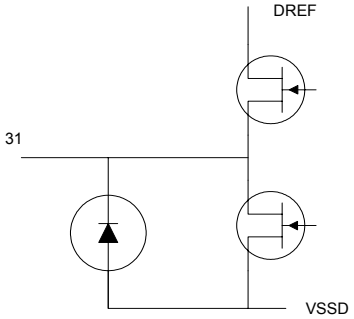
Pin	Symbol	Equivalent circuit
4	DIAG	
5	ENGAGE	
6	POWERUP	

Pin	Symbol	Equivalent circuit
7	CGND	
8	VDDA	
9	VSSA	

Pin	Symbol	Equivalent circuit
10	OSCREF	
11	HVPREF	
12	INREF	

Pin	Symbol	Equivalent circuit
13	TEST	
18	DREF	
19, 30	HVP1, 2	

Pin	Symbol	Equivalent circuit
20, 29 23, 26	VDDP2, 1 VSSP2, 1	
21, 28	BOOT	
22, 27	OUT1, 2	

Pin	Symbol	Equivalent circuit
24, 25	STAB1, 2	
31	OSCIO	

10 LIMITING VALUES

Table 6: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_p	Supply voltage	Asymmetrical operating mode	10	40	V
		Symmetrical operating mode	+/-5	+/-20	V
I_{orm}	repetitive peak current in output pin	note 1; maximum output current limiting	4		A
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature range		-55	150	°C
T_{amb}	Ambient temperature range		-40	85	°C

Notes
1. Current limiting concept.

11 THERMAL CHARACTERISTICS

Table 7: Thermal characteristics

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
$R_{th(j-a)\ SO32}$	Thermal resistance junction to ambient	In free air [1]	35	K/W
$R_{th(j-l)\ SO32}$	Thermal resistance junction to leadfinger	In free air [1]	16	K/W
$R_{th(j-c)\ SO32}$	Thermal resistance junction to case	In free air [2]	3	K/W

[1] Measured in the application board
[2] Strongly depends on where you measure on the case

12 QUALITY SPECIFICATION

In accordance with ‘SNW-FQ-611-D’. The number of the quality specification can be found in the “Quality Reference Handbook”. The handbook can be ordered using the code 9398 510 63011.

13 STATIC CHARACTERISTICS

Table 8: Static characteristics

Vp = 22V; f_{osc} =320 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_p	Single (a-symmetrical supply voltage	Operating mode note 1	10	22	36	V
	Symmetrical supply voltage	Operating mode note 1	+/- 5	+/-11	+/-18	V
I_{sleep}	Sleep supply current	Sleep mode	-	80	TBF	μA
$I_{q(tot)}$	Total quiescent supply current in operating mode	Operating mode No load, snubbers and filter connected	-	40	80	mA
Series resistance output switches						
$R_{ds,on25}$	Drain-source resistance power switch	Tj=25 °C	-	150	-	mΩ
$R_{ds,on125}$	Drain-source resistance power switch	Tj=125 °C	-	234	-	mΩ
Power up input: POWER UP w.r.t. CGND						
$V_{POWER\ UP}$	Input voltage	Reference to CGND note 5	0	-	6.5	V
$I_{POWER\ UP}$	Input current	$V_{POWER\ UP}$ = 3 V	-	1	20	μA
V_{low}	Input voltage low level	Reference to CGND	0	-	0.8	V
V_{high}	Input voltage high level mode	Reference to CGND note 5	2	-	6.5	V
Engage input: ENGAGE w.r.t. CGND						
V_{ENGAGE}	Input voltage	Reference to CGND note 5	0	-	6.5	V
I_{ENGAGE}	Input current	V_{ENGAGE} = 3 V	-	20	40	μA
V_{low}	Input voltage low level	Reference to CGND note 3	0	-	0.8	V
V_{high}	Input voltage high level mode	Reference to CGND Notes 3 and 5	3	-	6.5	V
Diagnostic output: DIAG w.r.t. CGND						
$V_{DIAG-LOW}$	Voltage on DIAG pin	Activated protection (see table 5). Reference to CGND.	-	-	0.8	V
$V_{DIAG-HIGH}$	Voltage on DIAG pin	Operating mode Reference to CGND.	2		5	V
Audio inputs; pins IN1M, IN1P, IN2M and IN2P						
V_i	DC input voltage	Note 2	-	2.9	-	V

Half supply voltage: HVP1, HVP2, HVPREF						
$V_{HVP1,2}$	Half supply voltage to charge SE-capacitor	Mute and operating mode	½V_p-0.5V	½ V_p	½V_p+0.5V	V
$I_{HVP1,2}$	Charge current for HVP capacitor	Mute mode HVP = ½ V_p – 1V		45		mA
V_{HVPREF}	Half supply reference voltage	Mute and operating	½V_p-0.5V	½ V_p	½V_p+0.5V	V
Amplifier outputs; pins OUT1 and OUT2						
$\|V_{oo(SE)}\|$	Output offset voltage with respect to HVPx	SE; mute;	-	-	15	mV
		SE; operating; note 4	-	-	150	mV
$\|V_{oo(BTL)}\|$	Output offset voltage	BTL; mute;	-	-	20	mV
		BTL; operating; note 4	-	-	210	mV
Stabilizer output; pin STAB1, STAB2						
$V_{o(stab)}$	Stabilizer output voltage	Mute and operating; with respect to V_{SSPX}	10	11	12	V
Voltage protections						
V_{UVP}	Under voltage protection		7.5	8.5	9.5	V
V_{OVP}	Over voltage protection		36	38.5	40	V
V_{UBP}	Un balance protection	Operating when HVPREF within V_{UBP} levels	8	11	14	V
Current protections						
I_{OCPlim}	Over current protection	Current limiting	4	-	-	A
Temperature protection						
T_{prot}	Temperature protection activation		155	-	160	°C
T_{TF}	Thermal foldback activation		140	-	150	°C
Oscillator reference						
V_{oscio_high}	Oscillator I/O level voltage high		4.0	-	5	V
V_{oscio_low}	Oscillator I/O level voltage low		0	-	0.8	V
S_{max}	Number of slaves driven by one master		12	-	-	-

Notes

1. The circuit is DC adjusted at Vp = 10V to 36V.
2. With respect to VSSA and with asymmetrical supply.
3. The transition between mute and operating mode is determined by the time-constant on the ENABLE pin.
4. DC output offset voltage is applied to the output during the transition between mute and operating mode in a gradual way. The dV_{oo}/dt caused by any DC output offset is determined by the time-constant on the ENGAGE pin.
5. The maximum voltage applied on POWER UP and ENGAGE pin must never exceed the supply voltage VDDx

14 SWITCHING CHARACTERISTICS

Table 9: Switching characteristics
Vp=22V; Tamb = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal oscillator						
f_{osc}	Typical internal oscillator frequency	R_{osc} = 39kΩ	-	320	-	kHz
$f_{osc(int)}$	Internal oscillator frequency range		300	-	500	kHz
Timing						
t_{rise}	Rise-time PWM output	Iout=0	-	10	-	ns
t_{fall}	Fall-time PWM output	Iout=0	-	10	-	ns
t_{min}	Minimum pulse width	Iout=0	-	80	-	ns

15 DYNAMIC SE AC CHARACTERISTICS

Table 10: Dynamic AC SE characteristics

Vp = 22V; R_L = 2 x 4Ω; f = 1kHz; f_{osc} = 320 kHz; R_{SL} < 0.05Ω (note 1); Tamb = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	Output power per channel	R_L = 4Ω; Vp = 22V; note 2 Continuous-time output power				
		THD = 0.5%, f = 1kHz	11	12	-	W
		THD = 0.5%, f = 100Hz	-	12	-	W
		THD =10%, f = 1kHz	14	15	-	W
		THD =10%, f = 100Hz	-	15	-	W
		R_L = 8Ω; Vp = 30V; note 2 Continuous-time output power				
		THD = 0.5%, f = 1kHz	11	12	-	W
		THD = 0.5%, f = 100Hz	-	12	-	W
		THD = 10%, f = 1kHz	14	15	-	W
		THD = 10%, f = 100Hz	-	15	-	W
		R_L = 4Ω; Vp = 29V; note 2 Maximum output power (short-time)				
		THD = 0.5%	19	20	-	W
		THD =10%	23	25	-	W
		R_L = 8Ω; Vp = 24V; note 2 Continuous-time output power				
		THD = 0.5%	7	8	-	W
		THD =10%	9	10	-	W
THD	Total harmonic distortion	Po = 1W: note 3				
		f_i = 1kHz	-	0.04	0.1	%
		f_i= 10kHz	-	0.04	0.1	%
Gv(cl)	Closed loop voltage gain	Vi=100mV; no load	29	30	31	dB
α_{cs}	Channel separation	f_i = 1kHz, Po=1W	56	70	-	dB
SVRR	Supply voltage ripple rejection	Operating; note 4				
		f_i=100Hz	-	50	-	dB
		f_i = 1kHz	-	45	-	dB
$\|Z_i\|$	input impedance	Differential	70	100		kΩ
V_{no}	Noise output voltage	Operating, R_s=0Ω, note 5	-	70	100	μV
		mute; note 6	-	50	70	μV
$\|DG_V\|$	Channel unbalance		-	1	-	dB
$V_{o(mute)}$	Output signal in mute	Mute; Vi=TBF	-	-	500	μV
CMRR	Common mode rejection ratio	$V_{i(CM)}$ = $1V_{RMS}$	-	75	-	dB

Notes

1. R_{SL} is the series resistance of inductor of low-pass LC filter in the application.
2. Output power is measured indirectly; based on R_{DSon} measurement.
3. Total harmonic distortion is measured in a bandwidth of 22 Hz to 20 kHz, AES17 brick wall. Maximum limit is guaranteed but not 100% tested.
4. V_{ripple} = $V_{ripple(max)}$ = 2V(p-p); R_s=0ohm.
5. B = 22Hz – 20kHz, AES17 brick wall
6. B = 22Hz – 20kHz, AES17 brick wall, independent on R_s

16 DYNAMIC BTL AC CHARACTERISTICS

Table 11: Dynamic AC BTL characteristics

Vp = 22V; R_L = 4Ω; f = 1kHz; f_{osc} = 320 kHz; R_{sL} < 0.05Ω (note 1); Tamb = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	Output power	R_L = 4Ω; Vp = 12V; note 2				
		Continuous-time output power				
		THD = 0.5%, f = 1kHz	11	12	-	W
		THD = 0.5%, f = 100Hz	-	12	-	W
		THD =10%, f = 1kHz	14	15	-	W
		THD =10%, f = 100Hz	-	15	-	W
		R_L = 8Ω; Vp = 22V; note 2				
		Continuous-time output power				
		THD = 0.5%, f = 1kHz	23	24	-	W
		THD = 0.5%, f = 100Hz	-	24	-	W
		THD =10%, f = 1kHz	28	30	-	W
		THD =10%, f = 100Hz	-	30	-	W
		R_L = 4Ω; Vp = 15V; note 2				
		Maximum output power (short-time)				
		THD = 0.5%	19	20	-	W
		THD =10%	23	25	-	W
		R_L = 8Ω; Vp = 30V; note 2				
		Maximum output power (short-time)				
		THD = 0.5%	38	40	-	W
		THD =10%	47	50	-	W
THD	Total harmonic distortion	Po = 1W: note 3				
		f_i = 1kHz	-	0.04	0.1	%
		f_i= 10kHz	-	0.04	0.1	%
Gv(cl)	Closed loop voltage gain		35	36	37	dB
SVRR	Supply voltage ripple rejection	Operating; note 4				
		f_i=100Hz	-	50	-	dB
		f_i = 1kHz	-	45	-	dB
		Sleep; f_i = 100Hz; note 4	-	80	-	dB
$\|Z_i\|$	Input impedance	Differential	35	50		kΩ
V_{no}	Noise output voltage	Operating, 18V, R_s=0 ohm, note 5	-	100	150	μV
		Mute; 18V, note 6	-	70	100	μV
$\|\Delta G_v\|$	Channel unbalance		-	1	-	dB
$V_{o(mute)}$	Output signal in mute	Mute; Vi=TBF	-	-	500	μV
CMRR	Common mode rejection ratio	$V_{i(CM)}$ = 1 V_{RMS}	-	75	-	dB

Notes

1. R_{SL} is the series resistance of inductor of low-pass LC filter in the application.
2. Output power is measured indirectly; based on R_{DSon} measurement.
3. Total harmonic distortion is measured in a bandwidth of 22 Hz to 20 kHz, AES17 brick wall. Maximum limit is guaranteed but may not be 100% tested.
4. V_{ripple} = $V_{ripple(max)}$ = 2V(p-p); R_s=0ohm.
5. B = 22Hz – 20kHz, AES17 brick wall
6. B = 22Hz – 20kHz, AES17 brick wall, independent on R_s

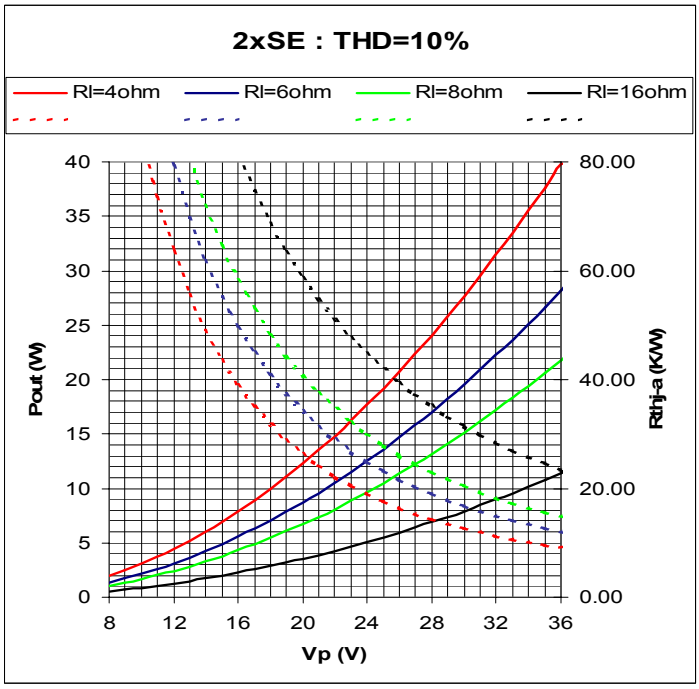


Figure 5: Output power stereo SE (@ THD=10%) and required Rth(j-a) versus supply voltage (Tj=125°C, dT=70°C)

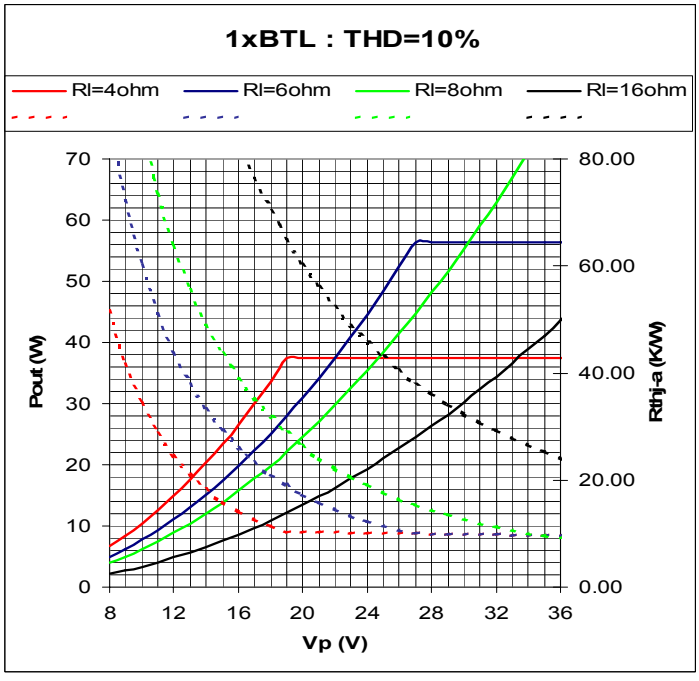


Figure 6: Output power mono BTL application (@ THD=10%) and required Rth(j-a) versus supply voltage (Tj=125°C, dT=70°C)

17 APPLICATION INFORMATION

17.1 Thermal behaviour (PCB considerations)

The heat sink in the application with the TDA8932 is made with the copper on the Printed Circuit Board (PCB). The TDA8932T uses the four corner leads (pins 1, 16, 17 and 32) for heat transfer from die to PCB. The limiting factor is the maximum junction temperature [Tj(max)]. In case of thermal foldback this maximum junction temperature is limited to 140 degrees for full gain. The formula below shows the relation between the maximum allowable power dissipation and the thermal resistance from junction to ambient.

$$R_{th(j-a)} = \frac{T_{j(max)} - T_a}{P_{diss}}$$

Pdiss is determined by the efficiency of the TDA8932.

In figures 5 and 6 the output power (for stereo SE and mono BTL application, both for THD=10%) is given as a function of supply voltage for different load impedances (4, 6, 8 and 16 ohm). The y-axis to the left in combination with solid lines applies to the output power levels. In the same figures the secondary y-axis on the right in combination with the dashed lines indicates the required Rth(j-a) value to apply these output powers continuously. All values are calculated taking into account a maximum temperature difference of 70 degrees between ambient and junction, while at the same time the maximum junction temperature is 125 degrees.

Example:
Vp=22V
Pout = 2 x 15W into 4 ohm (THD=10%)
Tj(max) = 125°C
Tamb = 55°C
The required Rth(j-a) = 22 K/W.

If music output power instead of continuous sine wave output power is considered the maximum achievable output power with the same Rth(j-a) can be much higher.

17.2 Thermal foldback

The TDA8932 has a built-in thermal foldback protection. In case the junction temperature of the TDA8932 exceeds the threshold level (e.g. 140°C) the gain of the amplifier is decreased to a level were the combination of dissipation and Rth(j-a) result in a junction temperature around the threshold level. This means that the device will not completely switch off, but remains operational at lower output power levels. Especially with music output signals this feature enables high peak output powers while still operating without any external heat sink other than the PCB area.

If the junction temperature still increases due to external causes a second temperature protection threshold level is built in which shuts down the amplifier completely.

17.3 Output Power estimation

The achievable output powers in several applications (SE and BTL) can be estimated using the following expressions:

$$SE: P_{o(0.5\%)} = \frac{\left(\frac{R_L}{R_L + Rs} x1/2V_P x\left(1 - t_{\min} x f_{osc}\right)\right)^2}{2xR_L}$$

$$BTL: P_{o(0.5\%)} = \frac{\left(\frac{R_L}{R_L + 2xRs} xV_P x\left(1 - t_{\min} x f_{osc}\right)\right)^2}{2xR_L}$$

Maximum current internally limited to 4A:

$$SE: I_{o(peak)} = \frac{1/2V_P x\left(1 - t_{\min} x f_{osc}\right)}{R_L + Rs}$$

$$BTL: I_{o(peak)} = \frac{V_P x\left(1 - t_{\min} x f_{osc}\right)}{R_L + 2xRs}$$

Variables:

R_L = load impedance
f_{osc} = oscillator frequency (typical 350 kHz)
t_{min} = minimum pulse width (typical 80 ns)
V_P = single sided supply voltage (or $0.5*(V_{DD} + |V_{SS}|)$)
$P_{O(0.5\%)}$ = output power at the onset of clipping
Rs = total series resistance consisting of bond wires, leads, Rdson_switch, series resistance of coil (typical 0.3Ω @ Tj=25°C)

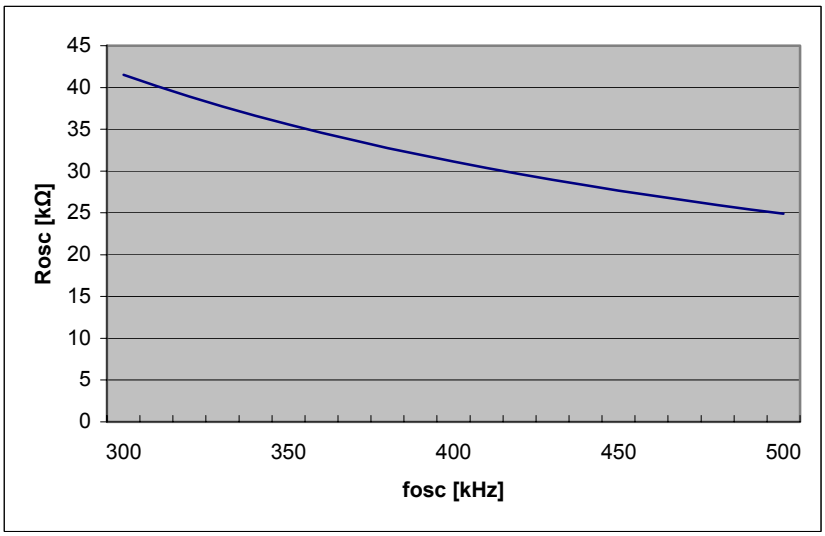
Note that $I_{o(peak)}$ should be below 4 A (section 9). $I_{o(peak)}$ is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and voltage drop over the coil.

17.4 External clock

If two or more class D amplifiers are used it is recommended that all devices run at the same switching frequency. This can be realized by connecting all OSCIO pins together and configure one of the TDA8932 in the application as CLOCK MASTER, while the other TDA8932 devices are configured in SLAVE MODE.

The OSCIO pin is a tri-state input output buffer.

In MASTER MODE the OSCIO pin is configured as oscillator OUTPUT. In SLAVE MODE the OSCIO pin is configured as oscillator INPUT.
MASTER MODE is enabled by applying a resistor between OSCREF pin and VSSD, while SLAVE MODE is entered by directly connecting the OSCREF pin to VSSD (so without any resistor). This is illustrated in figure 7.
The value of the resistor also sets the frequency of the carrier and can be estimated by following expression: $f_{osc} = \frac{12.45x10^9}{R_{OSC}}$



The table below summarizes how to configure the TDA8932 in Master or Slave configuration.

Table 12: Master/Slave configuration

Configuration	OSCREF	OSCIO
Master	Rosc > 25kΩ	OUTPUT
Slave	Rosc=0Ω; Shorted to VSSD	INPUT

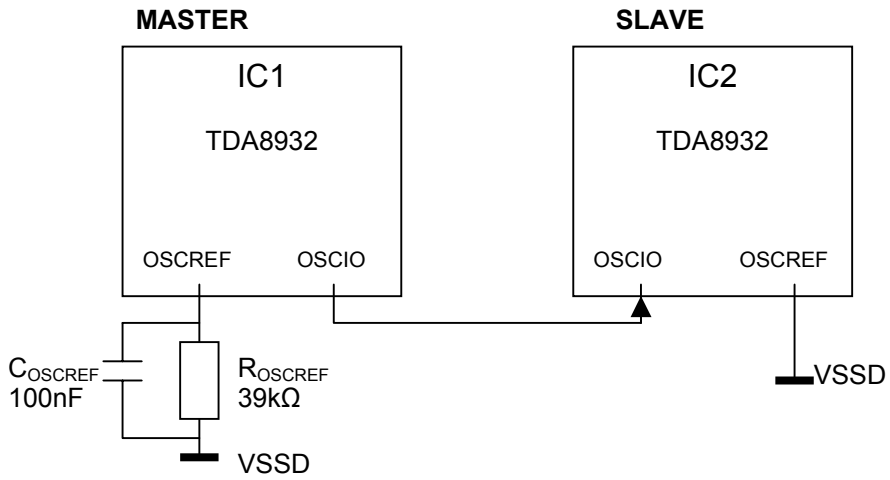


Figure 7: Master slave concept in two chip application

17.5 Pumping effects

When the amplifier is used in a SE configuration, a so-called 'pumping effect' can occur. During one switching interval, energy is taken from one supply (e.g. VDD), while a part of that energy is delivered back to the other supply line (e.g. Vss) and visa versa. When the power supply cannot sink energy, the voltage across the output capacitors of that power supply will increase.
The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of decoupling capacitors on supply lines
- Source and sink currents of other channels.

The pumping effect should not cause a malfunction of either the audio amplifier and/or the power supply. For instance, this malfunction can be caused by triggering of the under voltage or over voltage protection of the amplifier. Best remedy for pumping effects is to use the TDA8932 in the mono full-bridge application or in case of stereo half-bridge application, adapt the power supply (e.g. increase supply decoupling capacitors).
In a stereo half bridge application pumping effects can be minimized by connecting audio inputs in anti-phase and change the polarity of one speaker. This is illustrated in figure 8.

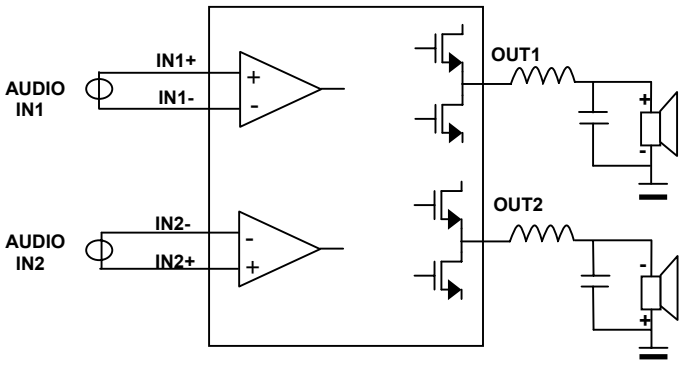


Figure 8: Input/speaker configuration for stereo SE application for reducing pumping effects.

17.6 Gain setting

The input signal in combination with the speaker impedance determines the required gain. The TDA8932 has a fixed gain of 30dB for SE applications. By adding a resistor of 12kΩ the gain is reduced by 6dB.

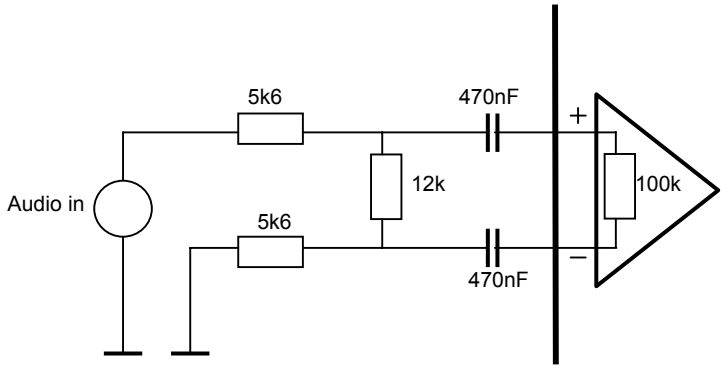


Figure 9: Input configuration for reducing gain.

17.7 Low pass filter considerations

For a flat frequency response (second order Butterworth filter) it is necessary to change the LC-filter components (Lx and Cx) according the speaker impedance. Table 13 shows the required components values in case of a 4Ω, 6Ω or 8Ω speaker impedance.

Table 13: Filter components value

Speaker impedance [Ω]	Lx value [μH]	Cx value [nF]
4	22	680
6	33	470
8	47	330

17.8 Curves measured in reference design

tbd

17.9 Typical application schematics

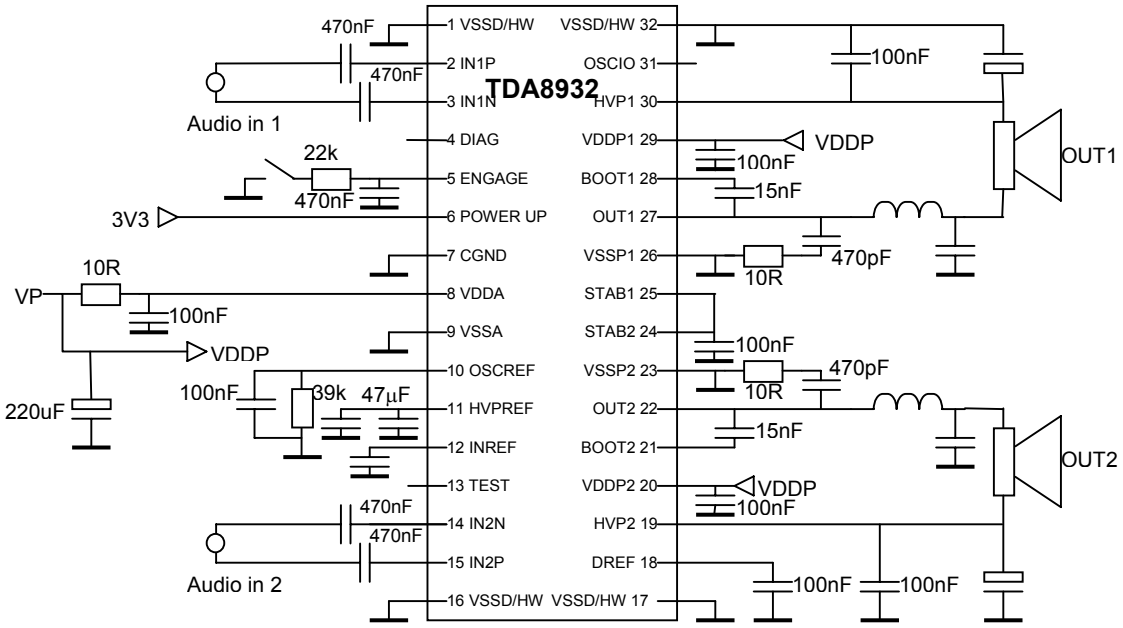


Figure 10: Typical application diagram for 2 x SE (asymmetrical supply)

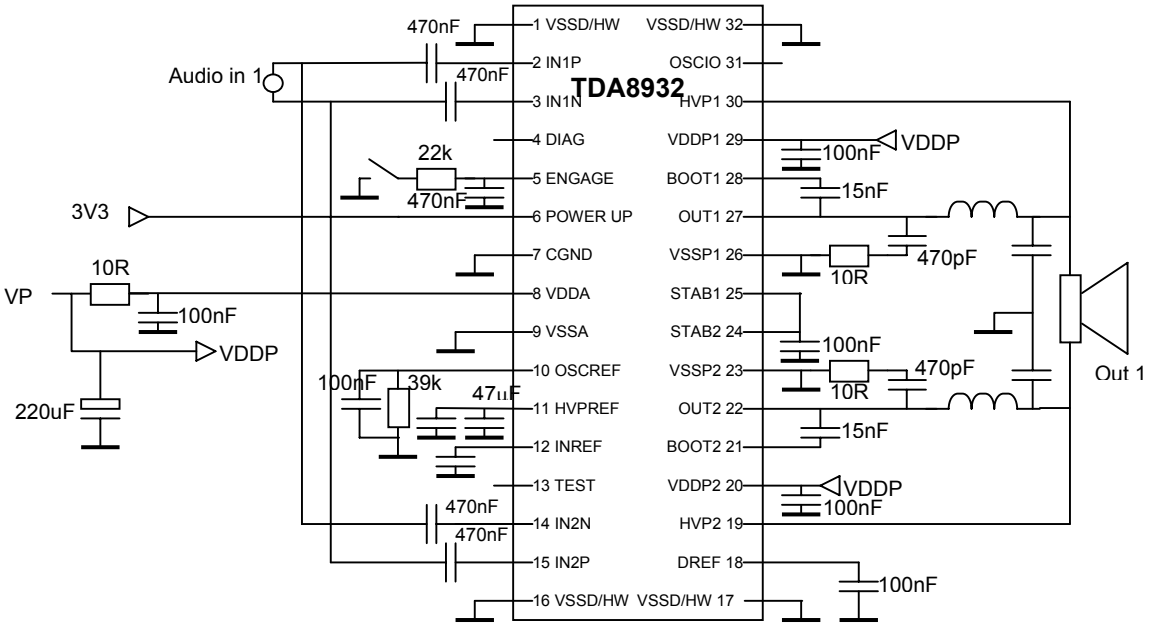


Figure 11: Typical application diagram for 1 x BTL (asymmetrical supply)

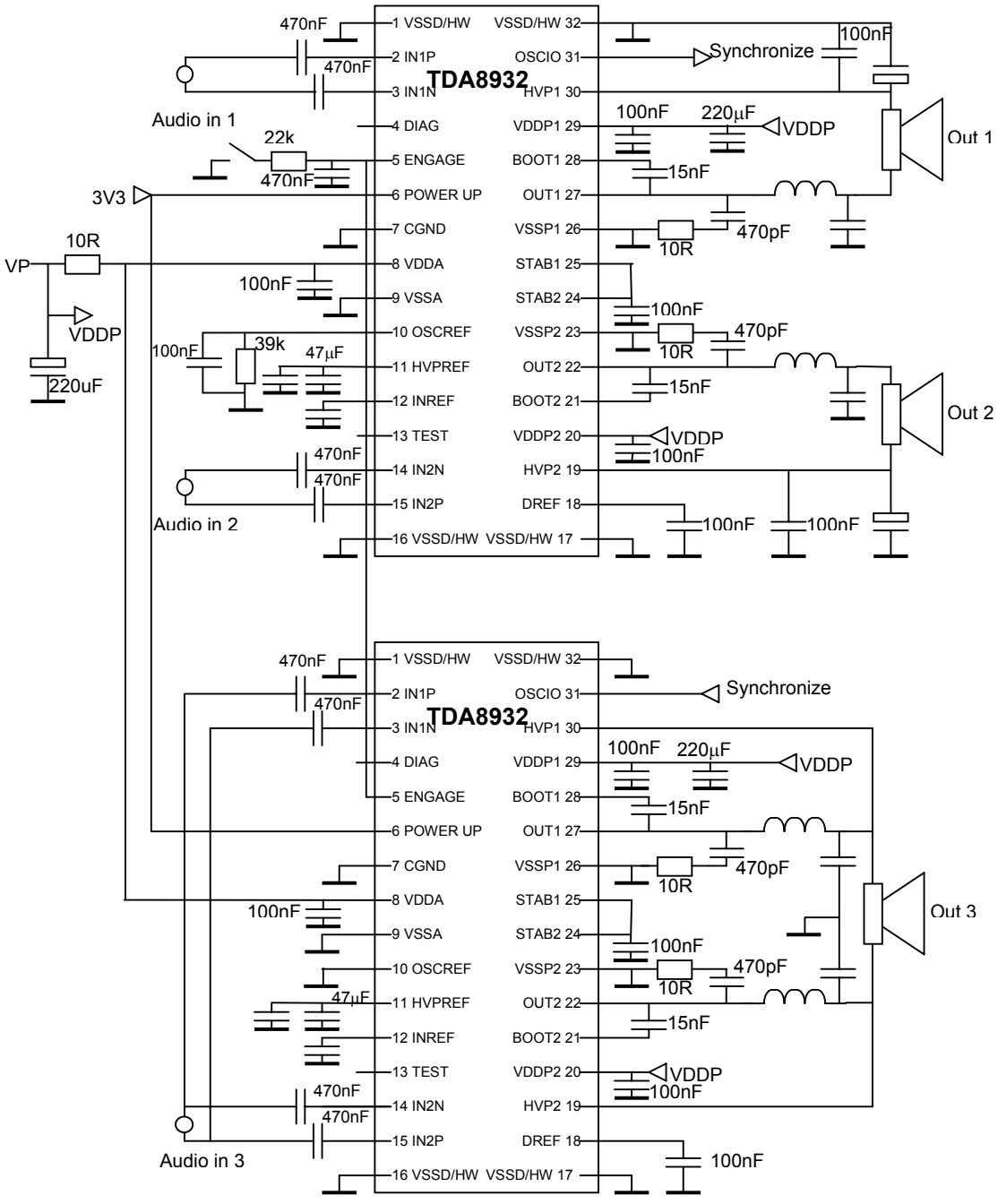
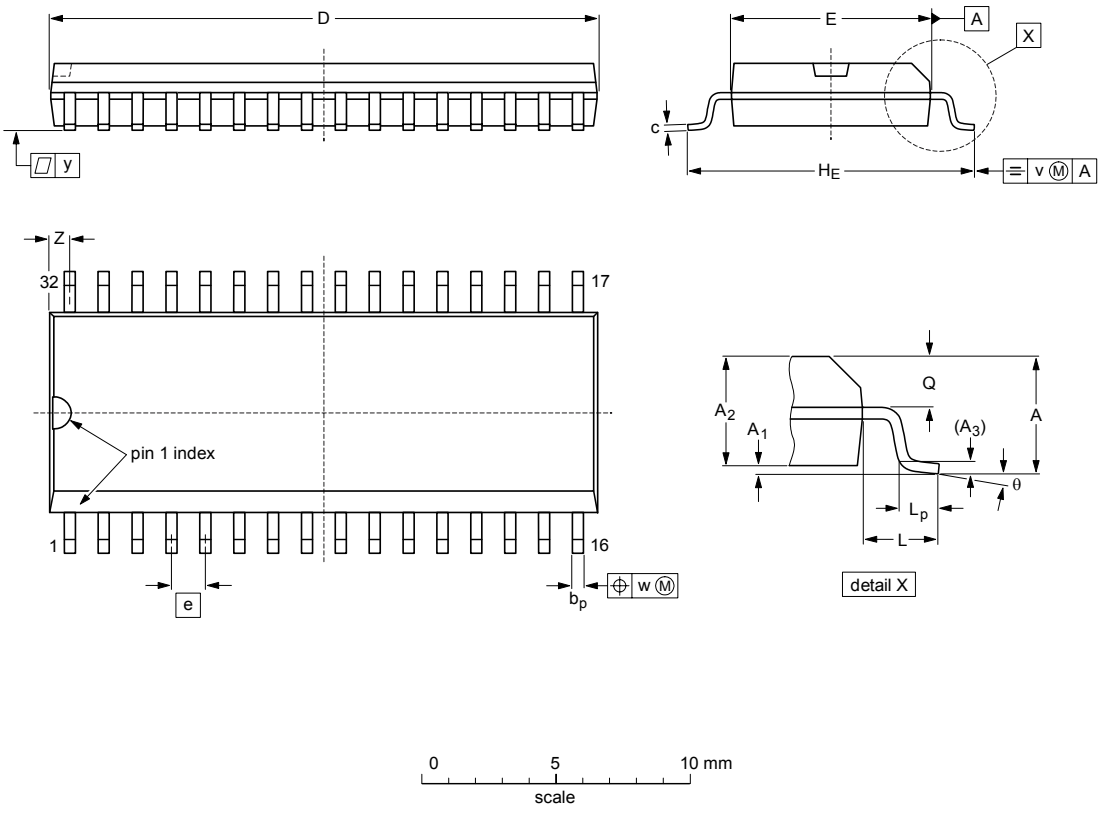


Figure 12: Typical application diagram for 2 x SE + 1 x BTL (asymmetrical supply)

18 PACKAGE OUTLINE

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT287-1		MO-119				~~00-08-17~~ 03-02-19

19 SOLDERING