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MC54/74HC244A

Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver

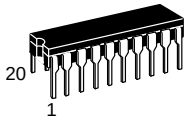
High–Performance Silicon–Gate CMOS

The MC54/74HC244A is identical in pinout to the LS244. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

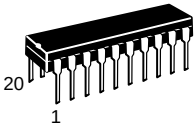
This octal noninverting buffer/line driver/line receiver is designed to be used with 3–state memory address drivers, clock drivers, and other bus–oriented systems. The device has noninverting outputs and two active–low output enables.

The HC244A is similar in function to the HC240A and HC241A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 136 FETs or 34 Equivalent Gates



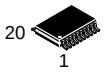
J SUFFIX
CERAMIC PACKAGE
CASE 732–03



N SUFFIX
PLASTIC PACKAGE
CASE 738–03

DW SUFFIX
SOIC PACKAGE
CASE 751D–04

SD SUFFIX
SSOP PACKAGE
CASE 940C–03



DT SUFFIX
TSSOP PACKAGE
CASE 948E–02

ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXADW	SOIC
MC74HCXXXASD	SSOP
MC74HCXXXADT	TSSOP

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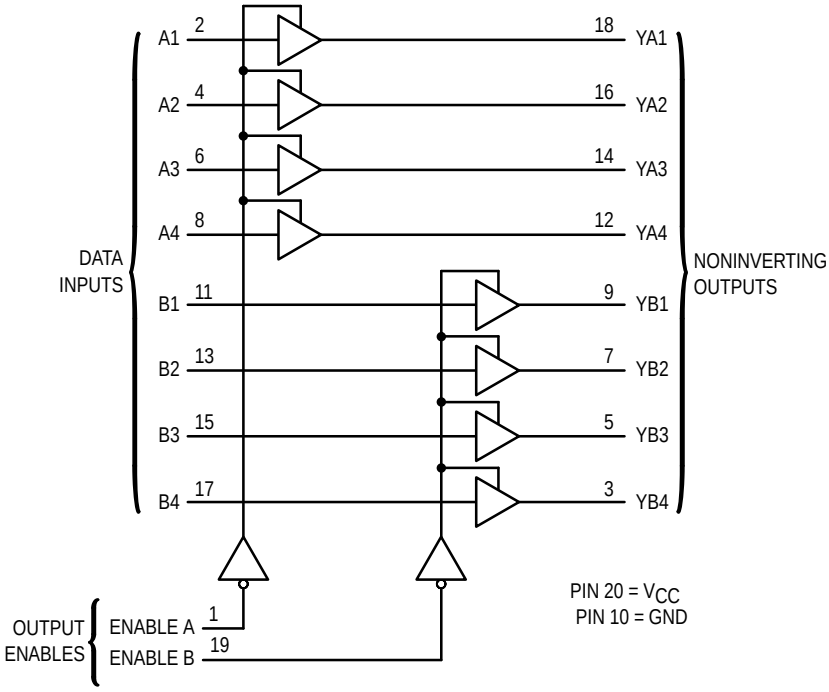
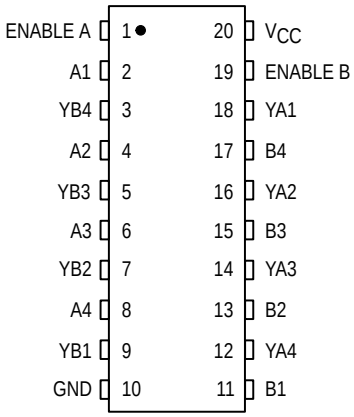
LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = high impedance

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† SSOP or TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	° C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package) (Ceramic DIP)	 260 300	° C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/° C from 65° to 125° C
Ceramic DIP: – 10 mW/° C from 100° to 125° C
SOIC Package: – 7 mW/° C from 65° to 125° C
SSOP or TSSOP Package: – 6.1 mW/° C from 65° to 125° C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	° C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25° C	≤ 85° C	≤ 125° C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 6.0 mA $\|I_{out}\|$ ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IL}$ $\lvert I_{out}\rvert \le 20\ \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in} = V_{IL}$ $\lvert I_{out}\rvert \le 2.4$ mA	3.0	0.26	0.33	0.4	
		$\lvert I_{out}\rvert \le 6.0$ mA	4.5	0.26	0.33	0.4	
		$\lvert I_{out}\rvert \le 7.8$ mA	6.0	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{OZ}	Maximum Three–State Leakage Current	Output in High–Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	4.0	40	160	µA

NOTE: Information on typical parametric values and high frequency or heavy load considerations can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	2.0	96	115	135	ns
		3.0	50	60	70	
		4.5	18	23	27	
		6.0	15	20	23	
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	60	70	80	
		4.5	22	28	33	
		6.0	19	24	28	
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	60	70	80	
		4.5	22	28	33	
		6.0	19	24	28	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		3.0	23	27	32	
		4.5	12	15	18	
		6.0	10	13	15	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	34	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

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SWITCHING WAVEFORMS

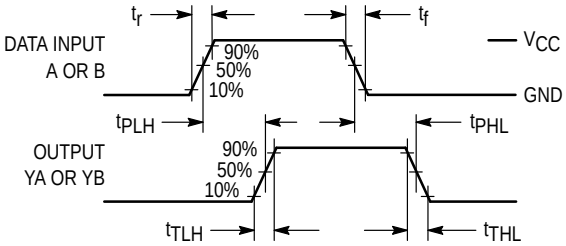


Figure 1.

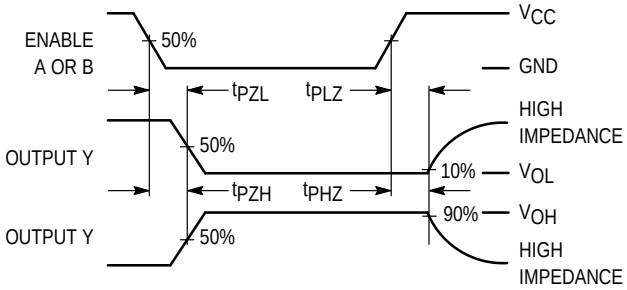
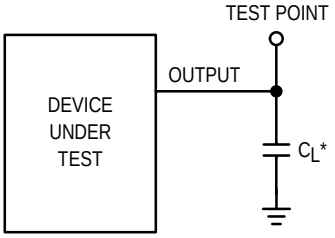


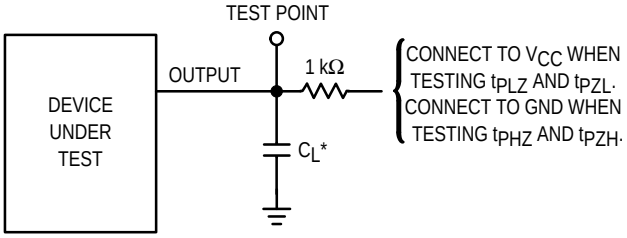
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

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PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, B1, B2, B3, B4
(Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROLS

Enable A, Enable B (Pins 1, 19)

Output enables (active–low). When a low level is applied to these pins, the outputs are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high impedance state.

OUTPUTS

YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4
(Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output–enable pins, these outputs are either noninverting outputs or high–impedance outputs.

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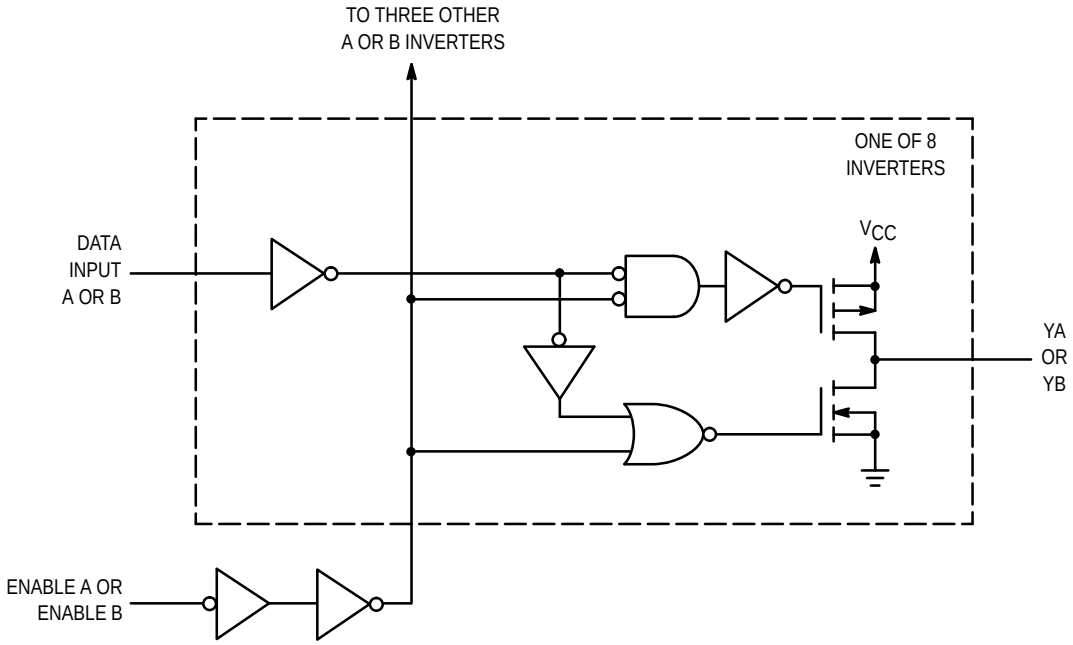
LOGIC DETAIL



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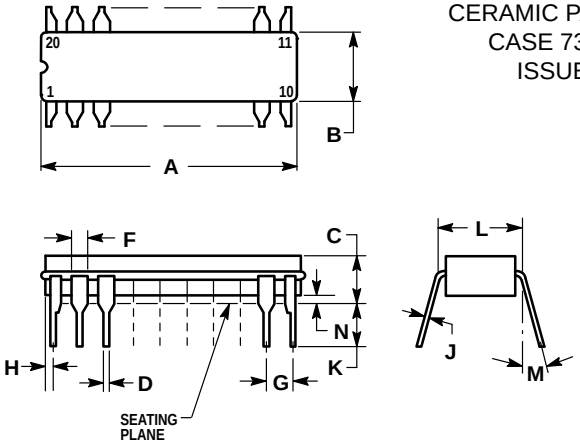
OUTLINE DIMENSIONS

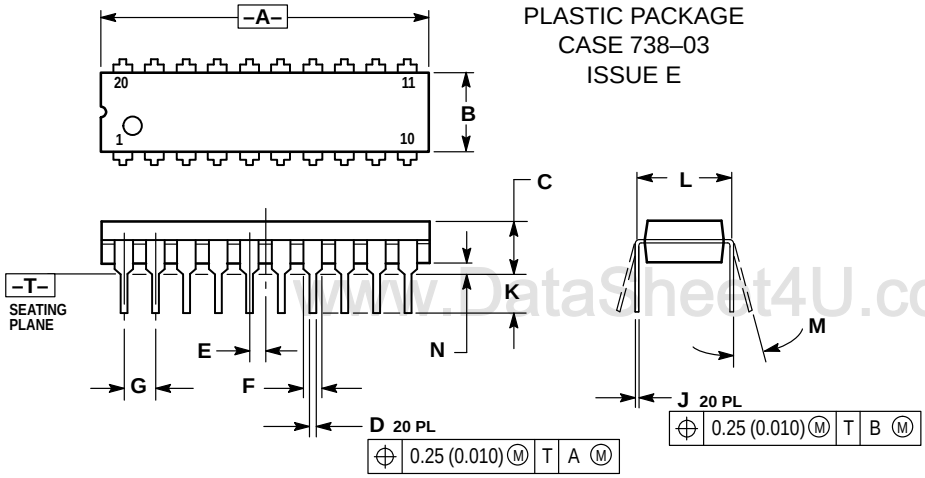
J SUFFIX
CERAMIC PACKAGE
CASE 732–03
ISSUE E



NOTES:
1. LEADS WITHIN 0.25 (0.010) DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

N SUFFIX
PLASTIC PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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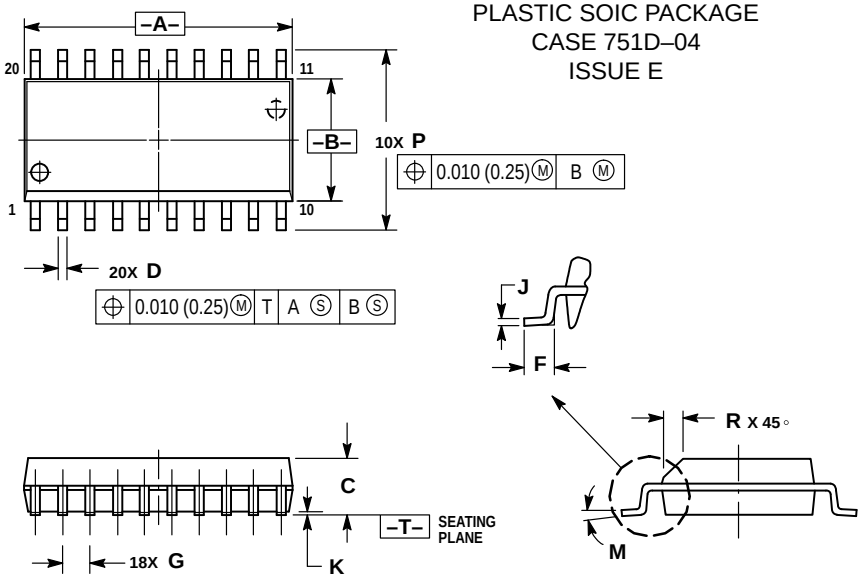
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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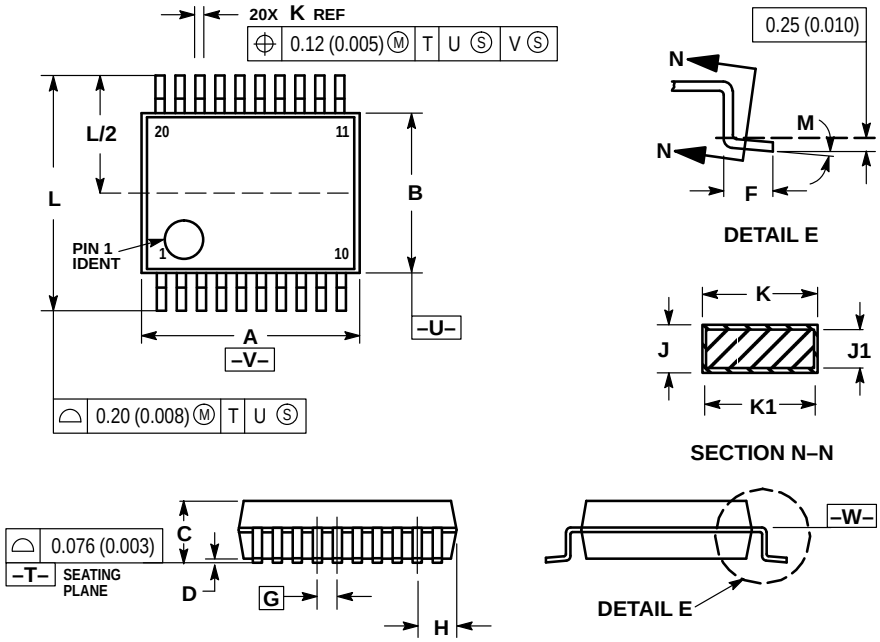
OUTLINE DIMENSIONS

SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940C–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

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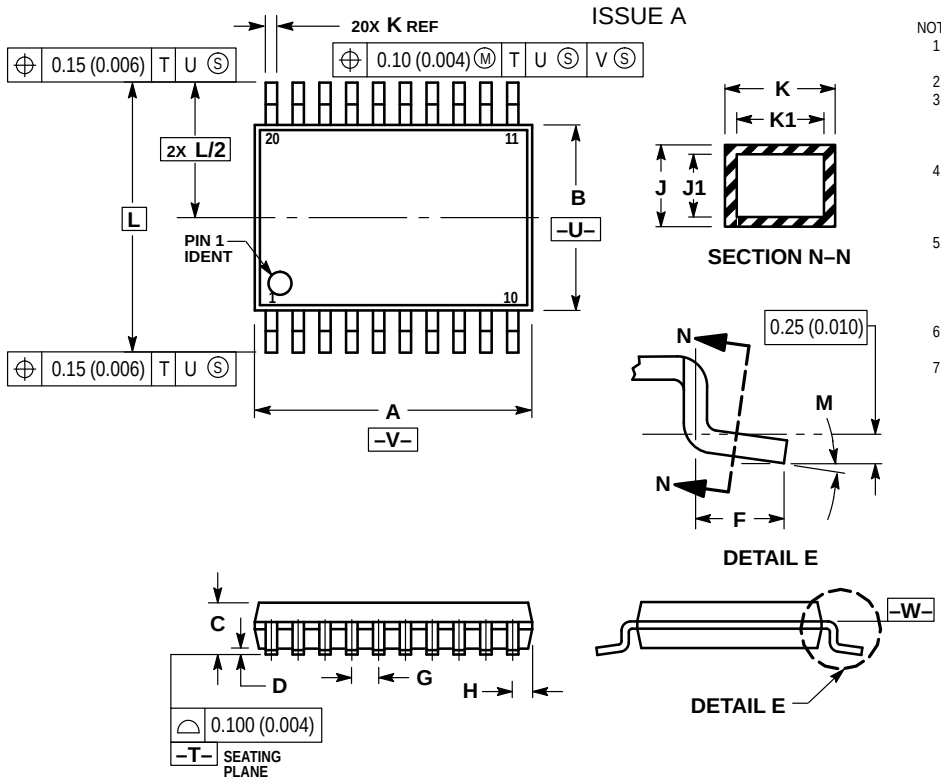
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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