RTD2023L

Flat Panel Display Controller

Version 0.13
Last updated: 2005/3/30

Revision History

0.13	3/30/2005			Initial release

1. Features

General
- Support DDCCI
- Zoom scaling up and down
- No external memory required.
- Require only one crystal to generate all timing.
- Programmable 3.3V/5V detection reset output.
- 3 channels 8 bits PWM output, and wide range selectable PWM frequency.

Analog RGB Input Interface
- Integrated 8-bit triple-channel 165MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync On Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL

Auto Detection /Auto Calibration
- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Scaling
- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor
- True 10 bits color processing engine
- sRGB compliance
- Advanced Dithering logic for 18-bit panel color depth enhancement
- Content adaptive edge enhancement.
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Programmable 10-bit gamma support

Output Interface
- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Dual/Single LVDS output interface
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Host Interface
- Support MCU serial bus interface.
- Support MCU dual edge data latch.

Embedded OSD
- Embedded 12K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 16 color palette with 24bit true color selection
- Maximum 8 window with alpha-blending/ gradient/dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Every window can place anywhere on the screen
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18~4x18 proportional font

Power & Technology
- 1.8V and 3.3V power supplier
- 0.18um CMOS process, 48-pin LQFP package
- Embedded 3.3V to 1.8V voltage regulator (P type) BJT control

2. Pin-Out Diagram

Analog Input with LVDS (when CR8D[7] = 0)

Analog Input with LVDS (when CR8D[7] = 1)

RTD2023L & RTD2323/RTD2523B pin-to-pin Illustration

3. Pin Description

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

■ **INPUT PORT**

Name	I/O	Pin No	Description	Tolerance	Note
AVS	I	4	ADC vertical sync input Adjustable Schmidt trigger Power from PIN 48	5V	
AHS	I	5	ADC horizontal sync input Power from PIN 48	5V	
B-	AI	6	Negative BLUE analog input	3.3V	
B+	AI	7	Positive BLUE analog input	3.3V	
G-	AI	8	Negative GREEN analog input	3.3V	
G+	AI	9	Positive GREEN analog input	3.3V	
SOG	AI	10	Sync on Green	3.3V	
R-	AI	11	Negative RED analog input	3.3V	
R+	AI	12	Positive RED analog input	3.3V	
ADC_GND	AG	13	ADC Ground		
ADC_VDD	AP	14	ADC Power (1.8V)		

■ **PLL**

Name	I/O	Pin No	Description	Tolerance	Note
XO	AO	1	Crystal OSC output		
XI	AI	2	Reference clock input from external crystal or from single-ended CMOS/TTL OSC	3.3V	
PLL_GND	AG	3	Ground for display digital PLL		
PLL_VDD	AP	48	Power for digital PLL (3.3V)		

■ **Host interface**

Name	I/O	Pin No	Description	Tolerance	Note
SDIO[3]	I/O	43/15	Serial control I/F data in (Open drain)	5V	
SCSB	O	44/16	Serial control I/F chip select (Open drain)	5V	
SCLK	O	45/17	Serial control I/F clock (Open drain)	5V	

■ **Pad/Digital Power & Ground**

Name	I/O	Pin No	Description	Tolerance	Note
Pad 1.8V Power	P	19/42	PVCC (1.8V)		
Pad 1.8V Ground	G	20/41	PGND		

■ **DDC Channel & PWM**

Name	I/O	No	Description	Tolerance	Note
PWM0	O	15/45	Open drain	5V	
DDCSCL/PWM1	I/O	16/44	Open drain	5V	
DDCSDA/PWM2	I/O	17/43	Open drain	5V	

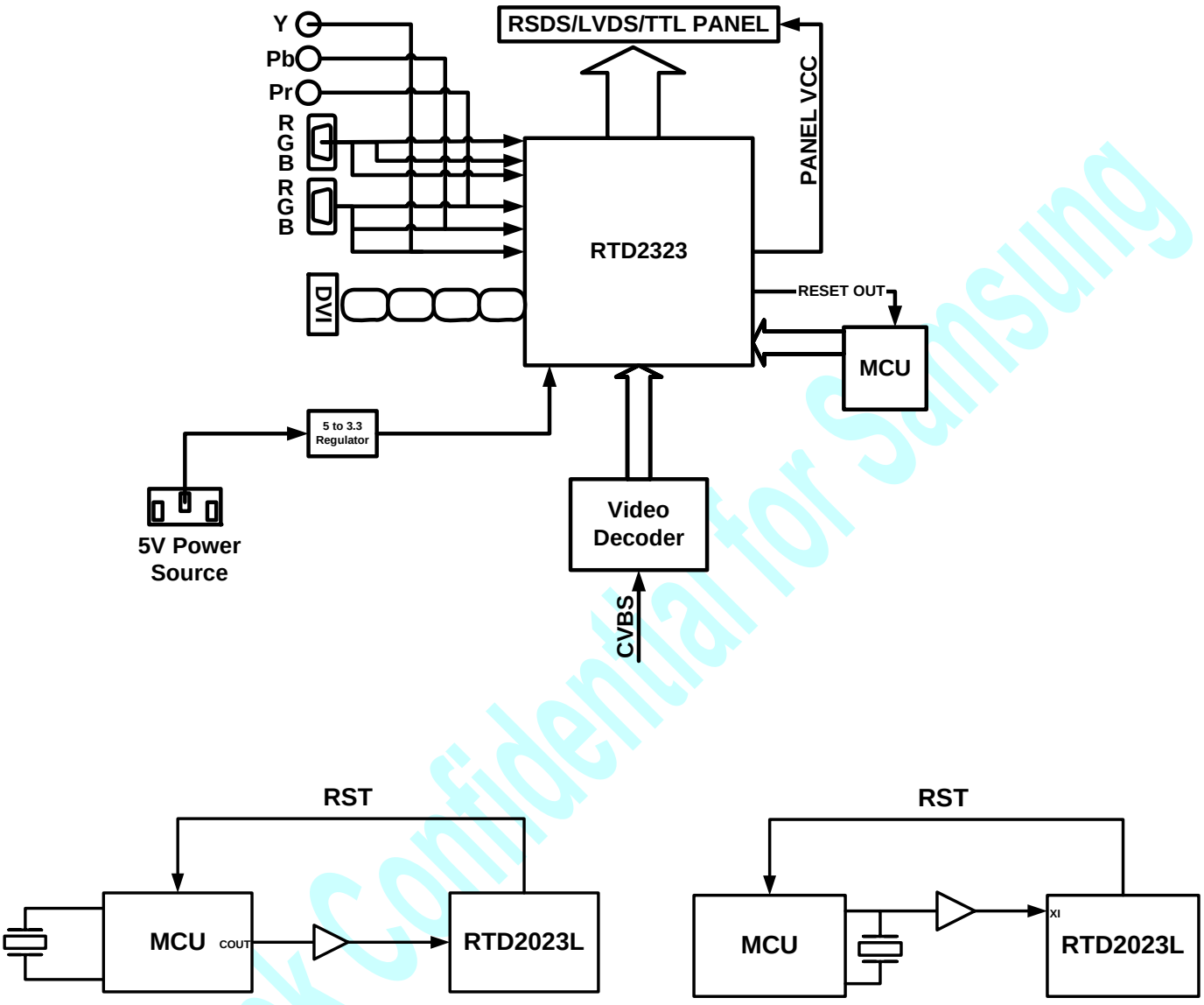
■ **MISC**

Name	I/O	No	Description	Tolerance	Note
BJT_B	O	18	Embedded regulator P type BJT control pin out	3.3V	
RESET_OUT	O	46	Reset out Open drain	5V	
33VRST_REF	I	47	Reference 3.3V for Reset Out		

■ LVDS Display Interface

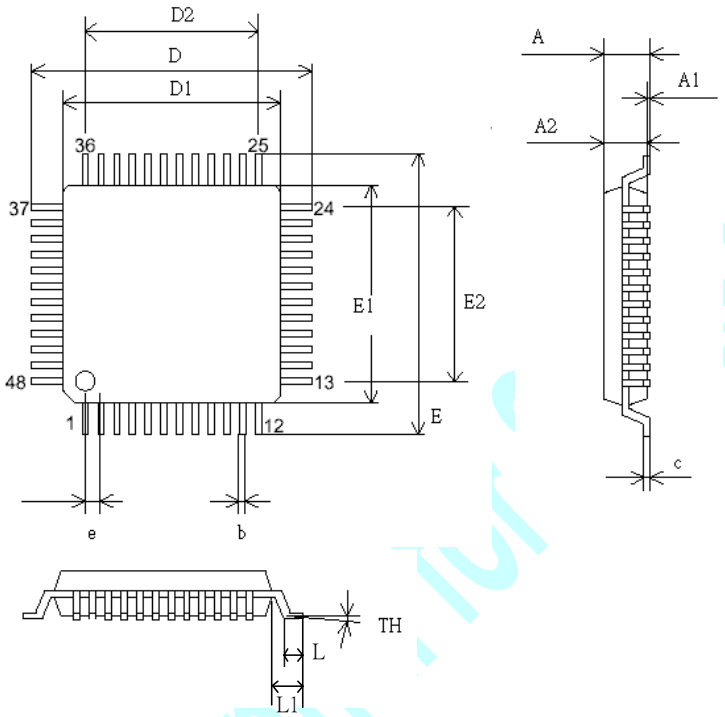
Name	I/O	No	Description	Tolerance	Note
TXE3+ / TXE0-	O	21	(CR8D[7] = 0) / (CR8D[7] = 1)	1.8V	
TXE3- / TXE0+	O	22		1.8V	
TXEC+ / TXE1-	O	23		1.8V	
TXEC- / TXE1+	O	24		1.8V	
TXE2+ / TXE2-	O	25		1.8V	
TXE2- / TXE2+	O	26		1.8V	
TXE1+ / TXEC-	O	27		1.8V	
TXE1- / TXEC+	O	28		1.8V	
TXE0+ / TXE3-	O	29		1.8V	
TXE0- / TXE3+	O	30		1.8V	
TXO3+ / TXO0-	O	31		1.8V	
TXO3- / TXO0+	O	32		1.8V	
TXOC+ / TXO1-	O	33		1.8V	
TXOC- / TXO1+	O	34		1.8V	
TXO2+ / TXO2-	O	35		1.8V	
TXO2- / TXO2+	O	36		1.8V	
TXO1+ / TXOC-	O	37		1.8V	
TXO1- / TXOC+	O	38		1.8V	
TXO0+ / TXO3-	O	39		1.8V	
TXO0- / TXO3+	O	40		1.8V	

4.Architecture



5. Mechanical Specification

48 Pin LQFP



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.0196 BSC		
TH	0o	3.5o	7o	0o	3.5o	7o
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		