10 MHz, 20 V/µs, G = 1, 2, 4, 8 *i*CMOS® Programmable Gain Instrumentation Amplifier

Preliminary Technical Data

AD8251

FEATURES

- Small package: 10-lead MSOP
- Programmable gains: 1, 2, 4, 8
- Digital or pin-programmable gain setting
- Wide supply: ±5 V to ±15 V
- Excellent dc performance
  - High CMRR 96 dB (min), G = 8
  - Low gain drift: 10 ppm/°C (max)
  - Low offset drift: 1.8 µV/°C (max), G = 8
- Excellent ac performance
  - Fast settling time: 615 ns to 0.001% (max)
  - High slew rate: 20 V/µs (min)
  - Low distortion: −110 dB THD at 1 kHz
  - High CMRR over frequency: 80 dB to 50 kHz (min)
  - Low noise: 18 nV/√Hz, G = 8 (max)
  - Low power: 4 mA

APPLICATIONS

- Data acquisition
- Biomedical analysis
- Test and measurement

FUNCTIONAL BLOCK DIAGRAM

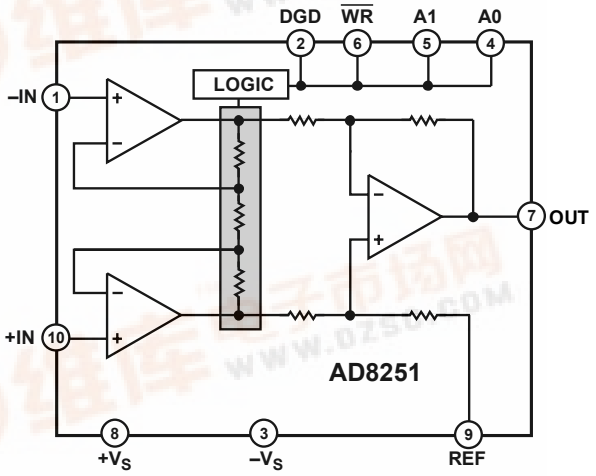

Figure 1.

GENERAL DESCRIPTION

The AD8251 is an instrumentation amplifier with digitally programmable gains that has GΩ input impedance, low output noise, and low distortion making it suitable for interfacing with sensors and driving high sample rate analog-to-digital converters (ADCs). It has high bandwidth of 10 MHz, low THD of −110 dB and fast settling time of 615 ns to 0.001%. Offset drift and gain drift are guaranteed to 1.8 µV/°C and 10 ppm/°C, respectively for G = 8. In addition to its wide input common voltage range, it boasts a high common-mode rejection of 80 dB at G = 1 from dc to 50 kHz. The combination of precision dc performance coupled with high speed capabilities make the AD8251 an excellent candidate for data acquisition. Furthermore, this monolithic solution simplifies design and manufacturing, and boosts performance of instrumentation by maintaining a tight match of internal resistors and amplifiers.

The AD8251 user interface consists of a parallel port that allows users to set the gain in one of two different ways (see Figure 1 for the functional block diagram). A 2-bit word sent via a bus can be latched using the $\overline{WR}$ input. An alternative is to use transparent gain mode where the state of logic levels at the gain port determines the gain.

Table 1. Instrumentation and Difference Amplifiers by Category

High Performance	Low Cost	High Voltage	Mil Grade	Low Power	Digital Gain
AD8220[1]	AD623[1]	AD628	AD620	AD627[1]	AD8231[1]
AD8221	AD8553[1]	AD629	AD621		AD8250
AD8222			AD524		AD8555[1]
AD8224[1]			AD526		AD8556[1]
			AD624		AD8557[1]

[1] Rail-to-rail output.

The AD8251 is available in a 10-lead MSOP package and is specified over the −40°C to +85°C temperature range, making it an excellent solution for applications where size and packing density are important considerations.

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SPECIFICATIONS

$+V_S$ = +15 V, $-V_S$ = −15 V, V_{REF} = 0 V @ T_A = 25°C, G = 1, R_L = 2 kΩ, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR to 60 Hz with 1 kΩ Source Imbalance	+IN = −IN = −10 V to +10 V				
G = 1		80	94		dB
G = 2		86	104		dB
G = 4		92	105		dB
G = 8		96	105		dB
CMRR to 50 kHz	+IN = −IN = −10 V to +10 V				
G = 1		80			dB
G = 2		86			dB
G = 4		89			dB
G = 8		90			dB
NOISE					
Voltage Noise, 1 kHz, RTI					
G = 1				40	nV/√Hz
G = 2				27	nV/√Hz
G = 4				22	nV/√Hz
G = 8				18	nV/√Hz
0.1 Hz to 10 Hz, RTI					
G = 1				2.5	µV p-p
G = 2				2.5	µV p-p
G = 4					µV p-p
G = 8					µV p-p
Current Noise, 1 kHz			5		pA/√Hz
Current Noise, 0.1 Hz to 10 Hz			60		pA p-p
VOLTAGE OFFSET					
Offset RTI V_{OS}	G = 1, 2, 4, 8			±200 + 600/G	µV
Over Temperature	T = −40°C to +85°C			±260 + 900/G	µV
Average TC	T = −40°C to +85°C			±1.2 + 5/G	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±5 V to ±15 V			±6 + 20/G	µV/V
INPUT CURRENT					
Input Bias Current			5	30	nA
Over Temperature	T = −40°C to +85°C			40	nA
Average TC				400	pA/°C
Input Offset Current			5	30	nA
Over Temperature	T = −40°C to +85°C			30	nA
Average TC				160	pA/°C
DYNAMIC RESPONSE					
Small Signal −3 dB Bandwidth					
G = 1		10			MHz
G = 2		10			MHz
G = 4		10			MHz
G = 8		3			MHz
Settling Time 0.01%	ΔOUT = 10 V step				
G = 1				585	ns
G = 2				605	ns
G = 4				605	ns
G = 8				648	ns

Parameter	Conditions	Min	Typ	Max	Unit
Settling Time 0.001%	ΔOUT = 10 V step				
G = 1				615	ns
G = 2				635	ns
G = 4				635	ns
G = 8				685	ns
Slew Rate					
G = 1		20			V/µs
G = 2		25			V/µs
G = 4		25			V/µs
G = 8		25			V/µs
Total Harmonic Distortion	f = 1 kHz, R_L = 10 kΩ, G = 1		−110		dB
GAIN					
Gain Range	G = 1, 2, 4, 8	1		8	V/V
Gain Error	OUT = ±10 V				
G = 1				0.03	%
G = 2, 4, 8				0.04	%
Gain Nonlinearity	OUT = −10 V to +10 V				
G = 1	R_L = 10 kΩ, 2 kΩ, 600 Ω			6	ppm
G = 2	R_L = 10 kΩ, 2 kΩ, 600 Ω			8	ppm
G = 4	R_L = 10 kΩ, 2 kΩ, 600 Ω			8	ppm
G = 8	R_L = 10 kΩ, 2 kΩ, 600 Ω			10	ppm
Gain vs. Temperature	All gains			10	ppm/°C
INPUT					
Input Impedance					
Differential		1			GΩ‖pF
Common Mode		1			GΩ‖pF
Input Operating Voltage Range	V_S = ±5 V to ±15 V	$-V_S$ + 1.0		$+V_S$ − 1.1	V
Over Temperature	T = −40°C to +85°C	$-V_S$ + 1.1		$+V_S$ − 1.4	V
OUTPUT					
Output Swing		−13.5		+13.5	V
Over Temperature	T = −40°C to +85°C	−13.5		+13.5	V
Short-Circuit Current			37		mA
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	+IN, −IN, REF = 0			1	µA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0001		V/V
DIGITAL LOGIC					
Digital Ground Voltage, DGND	Referred to GND	$-V_S$ + 4.25	0	$+V_S$ − 2.7	V
Digital Input Voltage Low	Referred to GND	DGND		2.1	V
Digital Input Voltage High	Referred to GND	2.8		$+V_S$	V
Digital Input Current			1		µA
Gain Switching Time[1]				325	ns
t_{SU}	See Figure 2 timing diagram	20			ns
t_{HD}		10			ns
$t_{\overline{WR}\text{-LOW}}$		20			ns
$t_{\overline{WR}\text{-HIGH}}$		40			ns

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		±5		±15	V
Quiescent Current, $+I_S$			4.1	4.5	mA
Quescent Current, $-I_S$			3.7	4.5	mA
Over Temperature	T = −40°C to +85°C			4.5	mA
TEMPERATURE RANGE					
Specified Performance		−40		+85	°C

[1] Add time for the output to slew and settle to calculate the total time for a gain change.

TIMING DIAGRAM

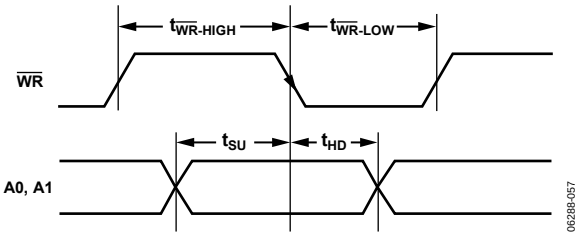


Figure 2. Timing Diagram for Latched Gain Mode (See the Timing for Latched Gain Mode Section)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±17 V
Power Dissipation	See Figure 3
Output Short-Circuit Current	Indefinite[1]
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Digital Logic Inputs	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range[2]	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	140°C
θ_{JA} (4-Layer JEDEC Standard Board)	112°C/W
Package Glass Transition Temperature	140°C

[1] Assumes the load is referenced to mid supply.
[2] Temperature for specified performance is −40°C to +85°C..

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8251 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 140°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8251. Exceeding a junction temperature of 140°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature is calculated as

$$T_J = T_A + \left(P_D \times \theta_{JA}\right)$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a 4-layer JEDEC standard board.

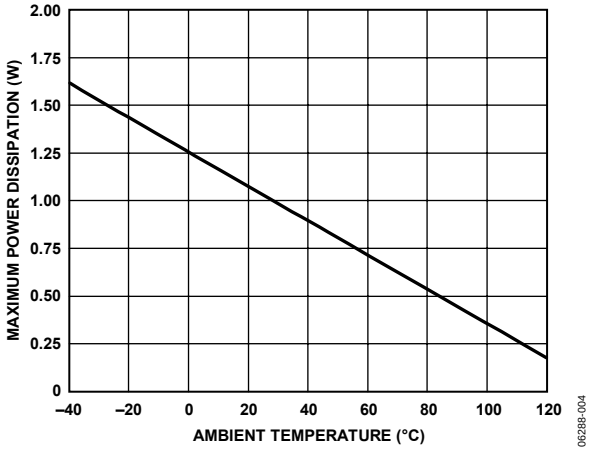


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

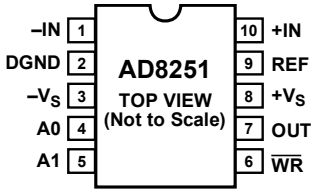


Figure 4. 10-Lead MSOP (RM-10), Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Name	Description
1	–IN	Inverting Input Terminal. True differential input.
2	DGND	Digital Ground.
3	$-V_S$	Negative Supply Terminal.
4	A0	Gain Setting Pin (LSB).
5	A1	Gain Setting Pin (MSB).
6	$\overline{WR}$	Write Enable.
7	OUT	Output Terminal.
8	$+V_S$	Positive Supply Terminal.
9	REF	Reference Voltage Terminal.
10	+IN	Noninverting Input Terminal. True differential input.

THEORY OF OPERATION

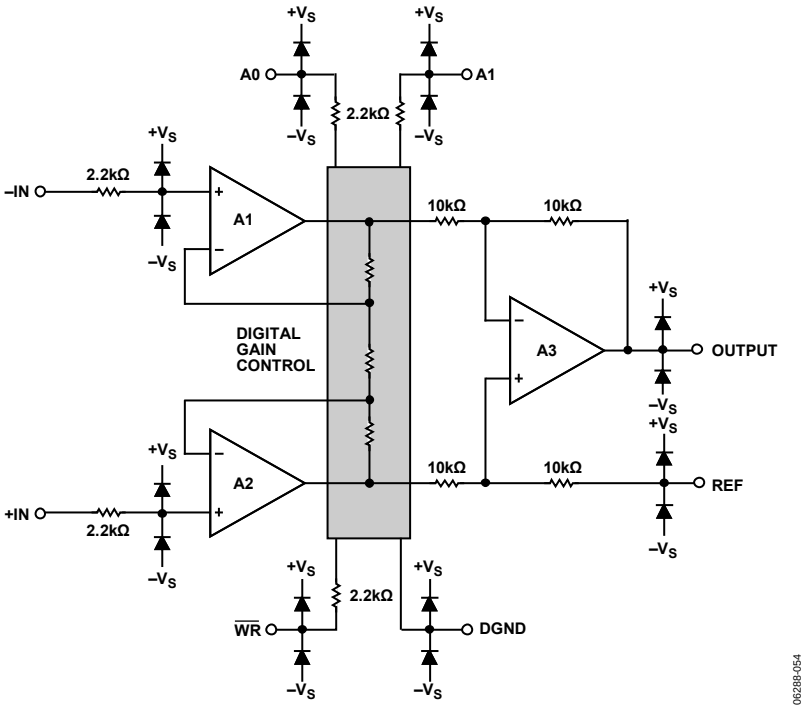


Figure 5. Simplified Schematic

The AD8251 is a monolithic instrumentation amplifier based on the classic, three-op amp topology as shown in Figure 5. It is fabricated on the Analog Devices, Inc. proprietary *i*CMOS process that provides precision, linear performance and a robust digital interface. A parallel interface allows users to digitally program gains of 1, 2, 4, and 8. Gain control is achieved by switching resistors in an internal, precision, resistor array (as shown in Figure 5). Although the AD8251 has a voltage feedback topology, gain bandwidth product increases for gains of 1, 2, and 4 because each gain has its own frequency compensation. This results in maximum bandwidth at higher gains.

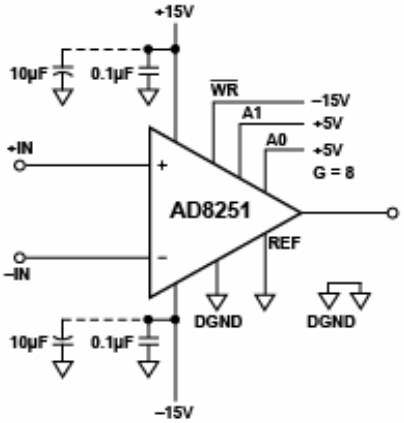
All internal amplifiers employ distortion cancellation circuitry and achieve high linearity and ultralow THD. Laser trimmed resistors allow for a maximum gain error of less than 0.03% for G = 1, and minimum CMRR of 96 dB for G = 8. A pinout optimized for high CMRR over frequency enables the AD8251 to offer a guaranteed minimum CMRR over frequency of 80 dB at 50 kHz (G = 1). The balanced input reduces the parasitics that, in the past, had adversely affected CMRR performance.

GAIN SELECTION

This section shows users how to configure the AD8251 for basic operation. Logic low and Logic high voltage limits are listed in the Specifications section. Typically, Logic low is 0 V and Logic high is 5 V; both voltages are measured with respect to DGND. Refer to the specifications table (see Table 2) for the permissible voltage range of DGND. The gain of the AD8251 can be set using two methods.

Transparent Gain Mode

The easiest way to set the gain is to program it directly via a Logic high or Logic low voltage applied to A0 and A1. Figure 6 shows an example of this gain setting method, referred to throughout the data sheet as transparent gain mode. Tie $\overline{WR}$ to the negative supply to engage transparent gain mode. In this mode, any change in voltage applied to A0 and A1 from Logic low to Logic high, or vice versa, immediately results in a gain change. Table 5 is the truth table for transparent gain mode and Figure 6 shows the AD8251 configured in transparent gain mode.



NOTE:
1. IN TRANSPARENT GAIN MODE, $\overline{WR}$ IS TIED TO $-V_S$. THE VOLTAGE LEVELS ON A0 AND A1 DETERMINE THE GAIN. IN THIS EXAMPLE, BOTH A0 AND A1 ARE SET TO LOGIC HIGH, RESULTING IN A GAIN OF 8.

Figure 6. Transparent Gain Mode, A0 and A1 = High, G = 8

Table 5. Truth Table Logic Levels for Transparent Gain Mode

$\overline{WR}$	A1	A0	Gain
$-V_S$	Low	Low	1
$-V_S$	Low	High	2
$-V_S$	High	Low	4
$-V_S$	High	High	8

LATCHED GAIN MODE

Some applications have multiple programmable devices such as multiplexers or other programmable gain instrumentation amplifiers on the same PCB. In such cases, devices can share a data bus. The gain of the AD8251 can be set using $\overline{WR}$ as a latch, allowing other devices to share A0 and A1. Figure 7 shows a schematic using this method, known as latched gain mode. The AD8251 is in this mode when $\overline{WR}$ is held at Logic high or Logic low, typically 5 V and 0 V, respectively. The voltages on A0 and A1 are read on the downward edge of the $\overline{WR}$ signal as it transitions from Logic high to Logic low. This latches in the logic levels on A0 and A1, resulting in a gain change. See the truth table listing in Table 6 for more on these gain changes.

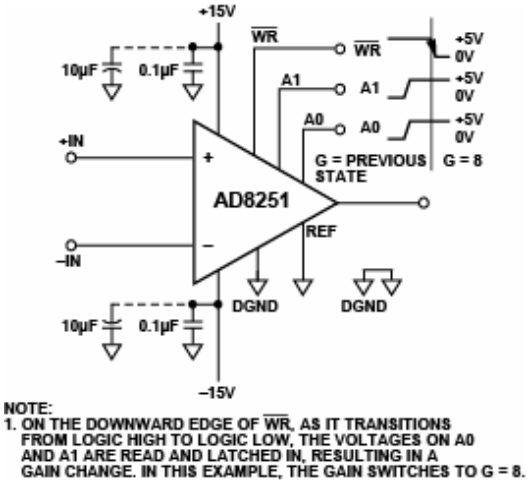


Figure 7. Latched Gain Mode, G = 8

Table 6. Truth Table Logic Levels for Latched Gain Mode

$\overline{WR}$	A1	A0	Gain
High to Low	Low	Low	Change to 1
High to Low	Low	High	Change to 2
High to Low	High	Low	Change to 4
High to Low	High	High	Change to 8
Low to Low	X[1]	X[1]	No Change
Low to High	X[1]	X[1]	No Change
High to High	X[1]	X[1]	No Change

[1] X = don't care.

Upon power up, the AD8251 defaults to a gain of 1 when in latched gain mode. In contrast, if the AD8251 is configured in transparent gain mode, it starts at the gain indicated by the voltage levels on A0 and A1 upon power-up.

Timing for Latched Gain Mode

In latched gain mode, logic levels at A0 and A1 have to be held for a minimum setup time, t_{SU}, before the downward edge of $\overline{WR}$ latches in the gain. Similarly, they must be held for a minimum hold time of t_{HD} after the downward edge of $\overline{WR}$ to ensure that the gain is latched in correctly. After t_{HD}, A0 and A1 may change logic levels but the gain does not change (until the next downward edge of $\overline{WR}$). The minimum duration that $\overline{WR}$ can be held high is $t_{\overline{WR}\text{-HIGH}}$, and $t_{\overline{WR}\text{-LOW}}$ is the minimum duration that $\overline{WR}$ can be held low. Digital timing specifications are listed in Table 2. The time required for a gain change is dominated by the settling time of the amplifier. A timing diagram is shown in Figure 8.

When sharing a data bus with other devices, logic levels applied to those devices can potentially feed through to the output of the AD8251. Feedthrough can be minimized by decreasing the edge rate of the logic signals. Furthermore, careful layout of the PCB also reduces coupling between the digital and analog portions of the board.

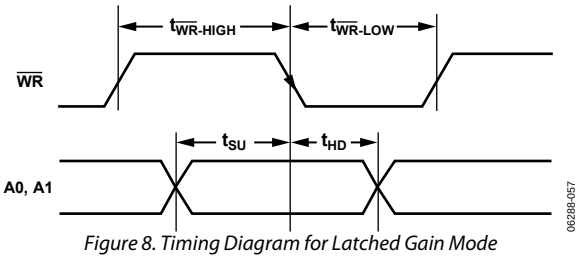
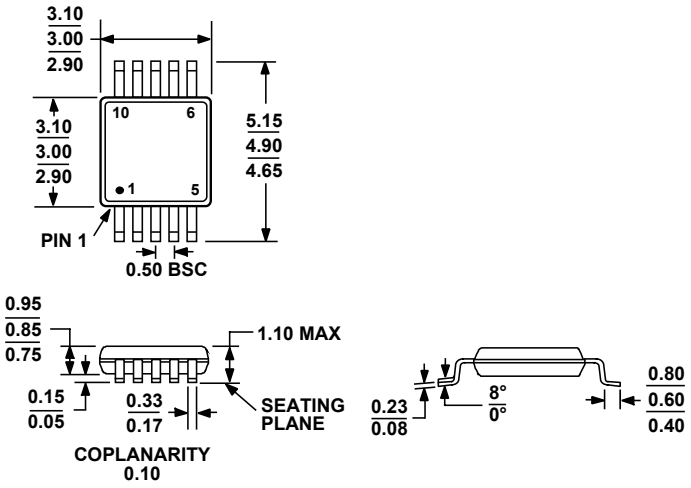


Figure 8. Timing Diagram for Latched Gain Mode

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 9. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8251ARMZ[1]	–40°C to +85°C	10-Lead MSOP	RM-10	H0T
AD8251ARMZ-RL[1]	–40°C to +85°C	10-Lead MSOP	RM-10	H0T
AD8251ARMZ-R7[1]	–40°C to +85°C	10-Lead MSOP	RM-10	H0T
AD8251-EVALZ[1]		Evaluation Board		

[1] Z = Pb-free part.

NOTES

NOTES

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