RichWave

RTC6711

Preliminary | **Data Sheet** | **Dec 2005**

Rev.	Date	From	Description
V.002 V.003	10/3/2005 10/31/2005	R2200 R2200	Original Modify the following items: 1. Add pin 1 PD_REG18 description; 1 for power down and 0 for power on 2. Modify switch mode to Easy channel selection mode 3. Add Absolute Maximum Ratings 4. Add S3=0 into Channel selection table 5. Modify Data slicer bit rate 4Mpbs in typical case
V.004	12/1/2005	R2200	1.Add SPI timing diagram 2.Add mini audio SNR 45dB in electrical specification 3.Add mini video SNR 45dB in electrical specification

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R2200

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RTC6711

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RTC6711 CMOS 2.4GHz FM/FSK Receiver

Product Description

The RTC6711 is a highly integrated FM/FSK receiver intended for application on 2.4GHz band analog FM or digital FSK demodulation. The chip includes a low noise amplifier, mixer, IF amplifier, FM demodulator, AGC, and FSK data slicer. With RSSI voltage output the instantaneous radio signal strength can be monitoring as input for the followed indicator process.

RX Carrier frequency can be set by SPI programming, or by selecting among 4 fixed channels using three dedicated pins. The device is available in a 48-pin QFN package.

Features

- 3.3V/2.5V Power Supply
- 2.4GHz ISM bands FM demodulator
- High sensitivity FM/FSK Receiver Operation
- Simple three digital pins setting 4 fixed channels to eliminate external micro-controller
- FM and FSK dual output formats
- Radio Strength Indicator (RSSI)
- CMOS technology
- On-chip VCO and PLL
- Receiver frequency setting by SPI programming
- 48-pin Leadless QFN package

Application

- AV Sender
- FSK transmitter
- Baby Monitor
- Wireless Camera
- Wireless Audio
- Wireless Earphone

Pin Descriptions

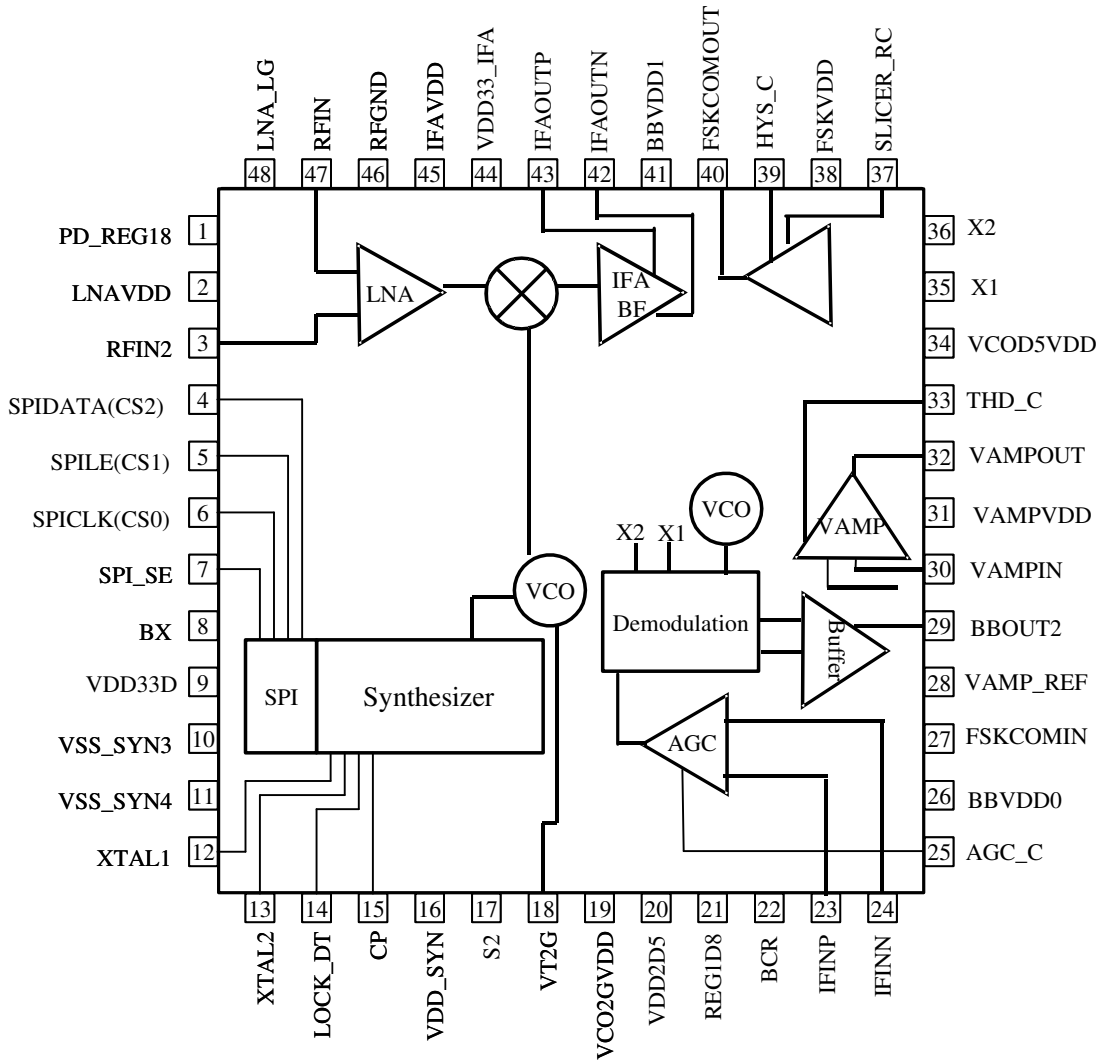
PIN	NAME	I/O	FUNCTION
1	PD_REG18	Digital In	Power Down 1.8V Regulator 1: Power Down; 0:Power on
2	LNAVDD	Supply In	LNA VDD
3	RFIN2	Analog In	NC
4	CS2	Digital In	Easy channel selection (Internal pull high)
	SPIDATA	Digital In	SPI bus data input
5	CS1	Digital In	Easy channel selection (Internal pull high)
	SPILE	Digital In	SPI bus latch enable input
6	CS0	Digital In	Easy channel selection (Internal pull high)
	SPICLK	Digital In	SPI bus clock input
7	SPI_SE	Digital In	Switch mode or SPI selection [1]
8	BX	Digital In	At easy channel selection mode : BX is used for alternative band selection [1] At SPI mode : BX is Don't care
9	VDD33D	Supply In	3.3V Digital Power
10	VSS_SYN3	Digital Ground	RF synthesizer digital ground pad
11	VSS_SYN4	Digital Ground	RF synthesizer digital ground pad
12	XTAL1	Analog In	Crystal Input
13	XTAL2	Analog In	Crystal Input
14	LOCK_DT	Digital Out	NC
15	CP	Analog Out	Charge Pump Output
16	VDDSYN	Supply In	Synthesizer VDD
17	S2	Digital In	Internal test only, don't care
18	VT2G	Analog In	RFVCO Vtune
19	VCO2GVDD	Supply In	2G VCO VDD
20	VDD2D5	Supply In	Regulator/Bias Center VDD
21	REG1D8	Analog Out	Regulator 1.8V for Digital
22	BCR	Analog I/O	Reference current by connecting 10k resistor
23	IFINP	Analog In	IFA_AF inputs
24	IFINN	Analog In	IFA_AF inputs
25	AGC_C	Analog I/O	AGC Rectifier output
26	BBVDD0	Supply In	Baseband 2.5V Supply
27	FSKCOMIN	Analog IN	FSK comparator Input
28	VAMP_REF	Analog I/O	Video amp reference
29	BBOUT2	Analog Out	FMDeMod Buffer negative output
30	VAMPIN	Analog In	Video amp input
31	VAMPVDD	Supply In	Video amp 3.3V VDD
32	VAMPOUT	Analog Out	Video amp output
33	THD_C	Digital In	Video amp linearity control 1 (Default): for high linearity mode
34	VCOD5VDD	Supply In	IFVCO VDD
35	X1	Digital In	IFVCO switched cap Control 1
36	X2	Digital In	IFVCO switched cap Control 2
37	SLICER_RC	Analog I/O	FSKCOM Slicer time constant Adjust
38	FSKVDD	Supply In	FSK comparator 3.3V VDD
39	HYS_C	Digital In	FSKCOM Slicer hysteresis control
40	FSKCOMOUT	Analog Out	FSK comparator Output
41	BBVDD1	Supply In	Baseband 2.5V Supply
42	IFAOUTN	Analog Out	IFA_BF outputs

Pin Descriptions (continued)

PIN	NAME	I/O	FUNCTION
43	IFAOUTP	Analog Out	IFA_BF outputs
44	VDD33_IFA	Supply In	IFA_BF ESD 3.3V VDD
45	IFAVDD	Supply In	IFA_BF and Mixer 2.5V VDD
46	RFGND	Analog In	LNA input be tied to RF ground
47	RFIN	Analog In	2.4 GHz LNA input for RF input signal
48	LNA_LG	Digital In	LNA high/low gain control

Note 1. Digital pins BX and SPI_SE (7,8) are without internal pull-high circuits, therefore those pins can not be left floating for logical high operation.

Block Diagram



Electrical Specification

(1) Absolute Maximum Ratings

SYMBOL	PARAMETER	Ratings	UNIT
Tstr	Storage Temperature Range	-65 to +150	°C
Totr	Operating Temperature Range	-40 to +85	°C
Vdd	Supply Voltage	-0.5 to +5	V
Vlog	Logic control signal	-0.5 to +5	V
VRX	RX input	-2 to +2	V

The maximum rating must not be exceeded at any time. Do not operate the device under conditions outside the above

(2) DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Tj	Temperature Range		-40	25	85	°C
VDD2D5	Analog Supply Voltage		2.25	2.5	2.75	V
VDD33	3.3V Supply Voltage		3.1	3.3	3.5	V
I_RF	Power consumption for IC	TT 25C, 2.5V/3.3V		94		mA
I_module	Power consumption under test circuit	TT 25C, 2.5V/3.3V		140		mA
I_pd	Power down current leakage	TT 25C, 2.5V		1	10	uA
Fref	Oscillator operating frequency			8		MHz
V_IH	High Level Input Voltage for Digital Interface	V_IO=3V	0.7xV_IO		V_IO+0.3	V
V_IL	Low Level Input Voltage for Digital Interface		-0.3		0.3xV_IO	V

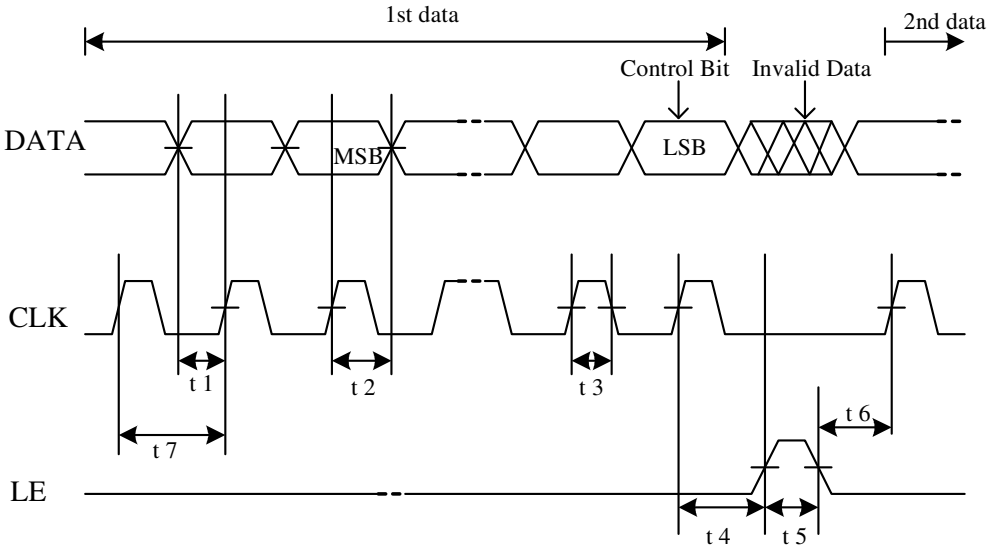
(3) Receiver Specifications

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
RF_Freq	RF Input frequency		2370		2510	MHz
IF_Freq	IF output frequency			479.5		MHz
S11	RF Input return loss under test circuit	External matching@50Ω		-10		dB
Si	Input Sensitivity measurement under test circuit	SNR 45dB Fmod=15KHz LPF BW:20KHz		-87		dBm
Phase noise	1934.5MHz	100KHz offset 1MHz offset		-110 -120		dBc/Hz
Z22_IFout	IF 479.5MHz output Impedance	SE		70		Ω
Z22_IFin	IF 479.5MHz Input Impedance	SE		280		Ω

(3) Receiver Specifications (continued)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Video						
Output signal level	Vpp after video amplifier	75ohm load		1		Vpp
Useable S/N	20dB higher than sensitivity	Fmod=15KHz LPF BW:20KHz		60		dB
VRSSI	RSSI Output Voltage (AGC_C pin)	Monotonically -85dBm to 5dBm	1.68		1.9	V
Audio						
Output signal level	Vpp after Audio Amplifier	Fmod: 1KHz tone Frequency deviation: ±25Khz Load: > 1Kohm		1		Vpp
THD	Total harmonic distortion Output 1Vpp (1KHz tone)	Fmod: 1KHz tone Frequency deviation: ±25Khz Load: > 1Kohm		0.6	0.9	%
S/N	Audio SNR (as reference design,) With pre-emphasis/ de-emphasis	Fmod: 1KHz tone Frequency deviation: ±25Khz Load: > 1Kohm	45	47		dB
FSK application						
Data Slicer Bit rate	As reference design			4		Mbps

(4) SPI Digital Timing Diagram



Parameter	Min.	Typ.	Max.	Unit
t1	20	-	-	ns
t2	20	-	-	ns
t3	30	-	-	ns
t4	30	-	-	ns
t5	100	-	-	ns
t6	20	-	-	ns
t7	100	-	-	ns

Note:
1.) On the rising edge of the clock, one bit of data is transferred into the shirt register.
2.) LE should be *L* when the data is transferred into the shirt register.

Channel Selection

There are two principle modes for channel selection

SPI_SE (Pin 7)	High	Low
Mode	SPI Mode	Easy Channel Selection Mode

(1) Easy channel selection mode

Pin 7 (SPI_SE) set low (0V), and the chip operates in Easy Channel Selection Mode. Operation frequency is selected by the pins 4(CS2), 5(CS1) and 6(CS0). The selected channel frequencies are listed in Table below.

BX=0

Pin8 (BX) is pulled low for normal ISM band, and operation frequency table show as following Table.

BX	SPI_SE	S2	Pin6/Pin5/Pin4 CS0/CS1/CS2			
			011	101	110	111
0	0	0	2414MHz	2432MHz	2450MHz	2468MHz

BX=1

Reserved for alternative band selection

(2) SPI mode

When pin 7 (SPI_SE) is set at high (3.3V), the chip works as in the SPI mode and the pins 5(SPIDATA), 5(SPILE) and 6(SPICLK)are used for 'SPI' inputs for 3-wire programming interface. The BX is "don't care".

SPI Register Definition

Address 00: Synthesizer Register A

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYN_RF_R_REG [14:0]															SYN_RF_A_REG [6:0]							Address	
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0

SYN_RF_R_REG [14:0]: R counter divider ratio control for RF Synthesizer.
SYN_RF_A_REG [6:0]: A counter divider ratio control for RF Synthesizer.

For integer N Synthesizer, the RF LO frequency is calculated by $(N*32+A)*f_{ref}/R$, where f_{ref} is the frequency of external reference oscillator (8 MHz). For default operation (f = 2414MHz, flo=1934.5MHz),
Default: R=16; N=120; A=29
1934.5MHz= (120*32+29)*8MHz/16

Address 01: Synthesizer Register B

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYN_RF_N_REG [12:0]													CP_RF [2:0]			SC_ctrl	Not Used			Not Used	Not Used	Address	
Default	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	X	X	X	X	X	0	1

SYN_RF_N_REG [12:0] : N counter divider ratio control for RF Synthesizer.
CP_RF [2:0] RF charge pump current control (from 50uA to 6mA, default=100uA)
SC_ctrl: external/internal SC_select control pin (LOW=internal). If set "1" in RTC67 series then charge pump will enter the testing mode ----Only for internal testing

Address 10: Synthesizer Register C

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LNAMIX_ctrl [2:0]			Not Used									Mout [1:0]		PRE_ctrl [2:0]			IFA_ctrl [2:0]			Not used		Address	
Default	1	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0

LNAMIX_ctrl [2:0]: For Rx Mixer LO_BUFFER bias current fine-tuning.
Ibias(000,001,010,011,100,101,110,111)=(0,30uA,60uA,90uA,120uA,150uA ,180uA,210uA)
Mout [1:0]: Multi-function output select
(00,01,11,10)=(gnd, lock in detect ,RF divider output, reference clk output)
PRE_ctrl [2:0]: Prescaler current control ([001]~[111])=(20 ~ 140uA).
IFA_ctrl [2:0]: For Rx IFA bias fine-tuning ([000] ~ [111])=240uA+15uA*(0~7)

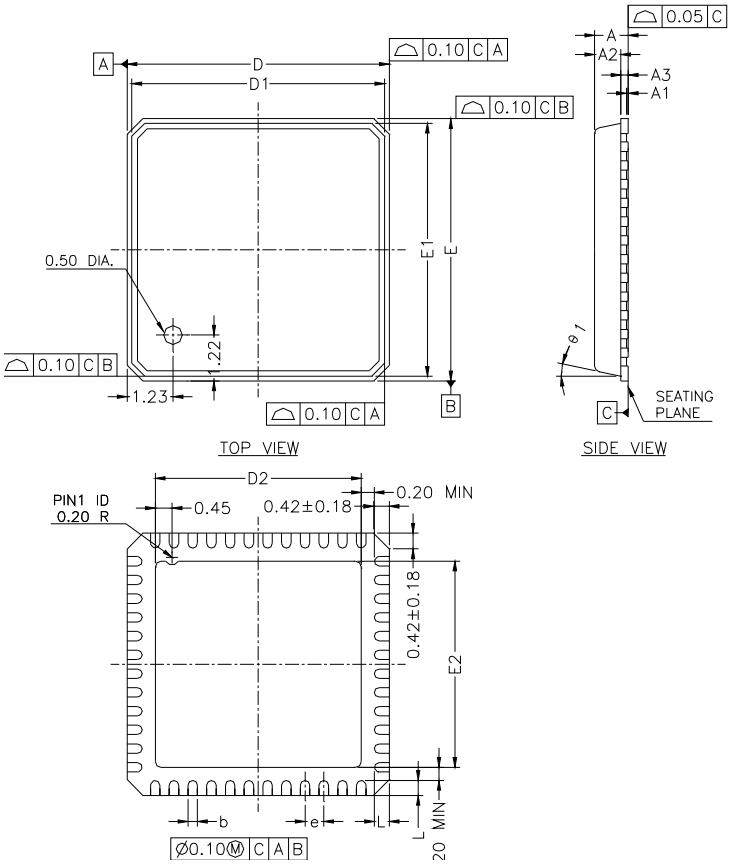
Address 11: Synthesizer Register D

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Not Used											VCOSC [1:0]		Not used	Not used				Not used		AC10_DMVCOPOUT [1:0]		Address	
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1

VCOSC[1:0] : The RF VCO switch capacitance
AC10_DMVCOPOUT [1:0] : The demodulation VCO output swing adjustment
AC10_DMVCOPOUT [1:0] Total Rb (ohm)

PACKAGE

QFN 7X7 48 pins



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.32	0.008	0.010	0.013
D	7.00 bsc			0.276 bsc		
D1	6.75 bsc			0.266 bsc		
D2	5.30	5.50	5.70	0.209	0.217	0.244
E	7.00 bsc			0.276 bsc		
E1	6.75 bsc			0.266 bsc		
E2	5.30	5.50	5.70	0.209	0.217	0.244
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		