ANALOG DEVICES

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APPLICATION NOTE

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Adding HART® Capability to the AD421, Loop-Powered 4 mA–20 mA DAC Using the 20C15* HART Modem

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INTRODUCTION

The AD421 is a complete, loop-powered, digital to 4 mA–20 mA converter designed to meet the needs of smart transmitter manufacturers in the industrial control industry. It provides a high precision, fully integrated, low cost solution in a compact 16-lead package and is ideal for extending the resolution of smart 4 mA–20 mA transmitters at very low cost. The HART (Highway Addressable Remote Transducer) protocol is widely accepted in the industry as the standard for digitally enhanced 4 mA–20 mA communication with smart field instruments. This protocol makes use of the Bell 202 Frequency Shift Keying (FSK) standard to superimpose digital signals at a low level on the 4 mA–20 mA analog signal. This allows two-way communication to take place and makes it possible for additional information beyond just the normal process variable to be communicated to/from a smart field instrument. The SYM20C15 from Symbios Logic is designed to allow the user implement a HART-compliant physical layer. This device implements the necessary modulation, demodulation, carrier detection, waveshaping and bandpass filtering to implement the protocol on-chip. The HART protocol communicates without interrupting the 4 mA–20 mA signal and allows a host application (master) to get two or more digital updates per second from a field device. As the digital FSK signal is phase continuous, there is no interference with the 4 mA–20 mA signal. Two different frequencies, 1200 Hz and 2200 Hz respectively, are used to represent binary 1 and 0 as shown in Figure 1.

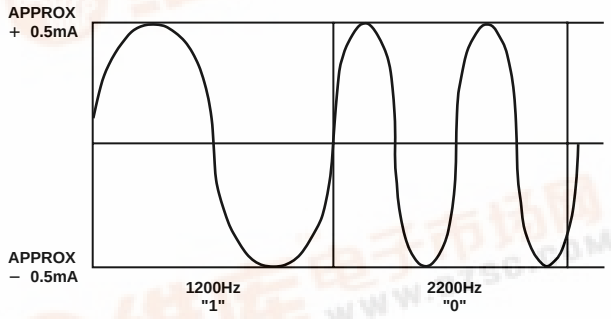

Figure 1. Digital Transmission Using the HART Protocol

These tones are superimposed on the dc signal at a low level with the average value of the sine wave signal being zero. Therefore, no dc component is added to the existing 4 mA–20 mA signal regardless of the digital data being sent over the line. Consequently, existing analog instruments continue to work in systems that apply HART; as the low-pass filtering present removes the digital signal. A single-pole 10 Hz low-pass filter effectively reduces the communication signal to a ripple of about ±0.01% of the full scale signal. Figure 2 shows a block diagram of a field instrument that uses the HART protocol.

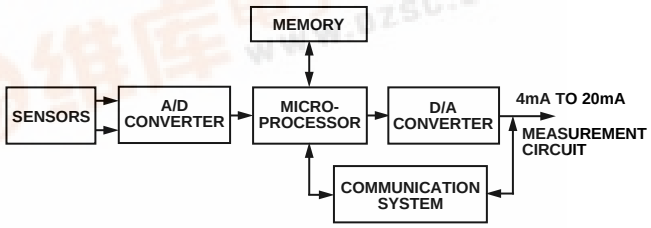

Figure 2. Smart and Intelligent Field Instrument

This application note deals primarily with the interface between the AD421 loop-powered 4 mA–20 mA DAC and the 20C15 HART modem and the necessary steps required to implement a HART-compliant instrument.

os Logic, Telephone No. (408) 433-8000.
of the HART Communication Foundation

AD421 Current Control Circuitry

The AD421 contains a 16-bit sigma-delta DAC to convert the digital information loaded to the input latch into a current. The sigma-delta architecture is particularly useful for the relatively low bandwidth requirements of the industrial control environment because of its inherent monotonicity at high resolution. The AD421 guarantees monotonicity to the 16-bit level.

The sigma-delta DAC on the part consists of a second order modulator followed by a continuous time filter. The single bit stream from the modulator controls a switched current source. This current source is then filtered by three resistor capacitor filter sections. The resistors for each of the filter sections are on-chip while the capacitors should be connected to the C1, C2 and C3 pins. To meet the specified HART physical layer low pass characteristic of a double pole with cutoff frequency of 25 Hz, capacitor C1 should be 0.01 μF, C2 = 0.5 μF and C3 = 0.16 μF. The HART signal is coupled into the loop through capacitor C_C at node C3. Capacitors C_C and C3 ensure a flat response at the HART frequencies of 1200 Hz and 2200 Hz. Figure 3 shows a block diagram of the current control circuitry within the AD421.

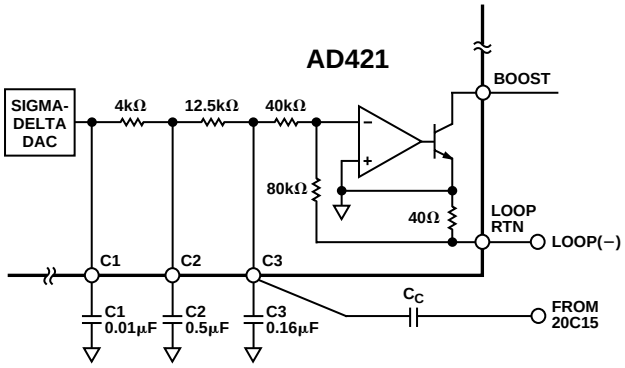

Figure 3. AD421 Current Control Circuitry

The DAC output current drives the second section, an operational amplifier and NPN transistor which acts as a current amplifier to set the current flowing from the LOOP RTN pin. The base drive to the NPN transistor servos the voltage across the 40 Ω sense resistor to equal the voltage across the 80 kΩ resistor connected between the DAC output and loop return.

Selecting Coupling Capacitor C_C

The HART output signal on the loop is 1 mA p-p and is generated in the AD421 by applying a suitable voltage signal to the C3 pin as mentioned earlier. HART applications accommodate both digital and analog communications, therefore it is very important that the digital HART signal injected onto the loop not interfere with the mean value of the analog loop current. The HART signal is ac-coupled to avoid introducing errors. Capacitors C_C and C3 attenuate the HART voltage signal from the 20C15 to ensure that a HART signal of 1 mA p-p gets onto the loop during HART transmissions. The signal appearing at the C3 pin is applied across a 40 kΩ resistor and twice this signal is forced across the 40 Ω loop current sense resistor. Therefore, a 20 mV signal is required at the C3 pin to ensure a 1 mA current on the loop. The following attenuation factor is required on the HART input signal V_H from the 20C15.

$$\textit{Attenuation Factor: } 20\ mV/V_H = C_C/(C_C + C3).$$
$$\therefore\ C_C = (20E{-}3 \times C3)/(V_H{-}20E{-}3).$$
$$\textit{Filter Time Constant} = (C_C + C3) \times (40E + 3).$$

As an example, if the HART input signal applied to C_C is 500 mV p-p, and the filter time constant is to correspond to 25 Hz, the HART signal band requirement, then C_C should be approximately 6.2 nF.

AD421-20C15 Interface

Figure 4 shows an evaluation circuit for the AD421-20C15 interface, which shows the required components to implement the transmit interface. The external transistor Q1 (DN25D depletion mode MOSFET), in association with the internal op amp and voltage reference on the AD421, form a voltage regulator that regulates the supply voltage for the AD421 from the loop voltage. LK1, LK2 and LK3 allow this regulated voltage to be programmed to either 5 V, 3.3 V or 3 V. The external pass transistor (Q2) is added to reduce the power loading on the depletion mode MOSFET Q1.

The MOSFET supplies the quiescent current for the AD421. The BOOST pin on the AD421 sinks the necessary current through the pass transistor Q2 from the loop so that the current flowing into BOOST, plus the quiescent current flowing into COM, equals the programmed loop current.

U3 shows the 20C15 HART modem and its associated circuitry required to implement the HART interface. The coupling capacitor C15 couples the HART signal onto the analog 4 mA–20 mA loop at the C3 pin of the AD421.

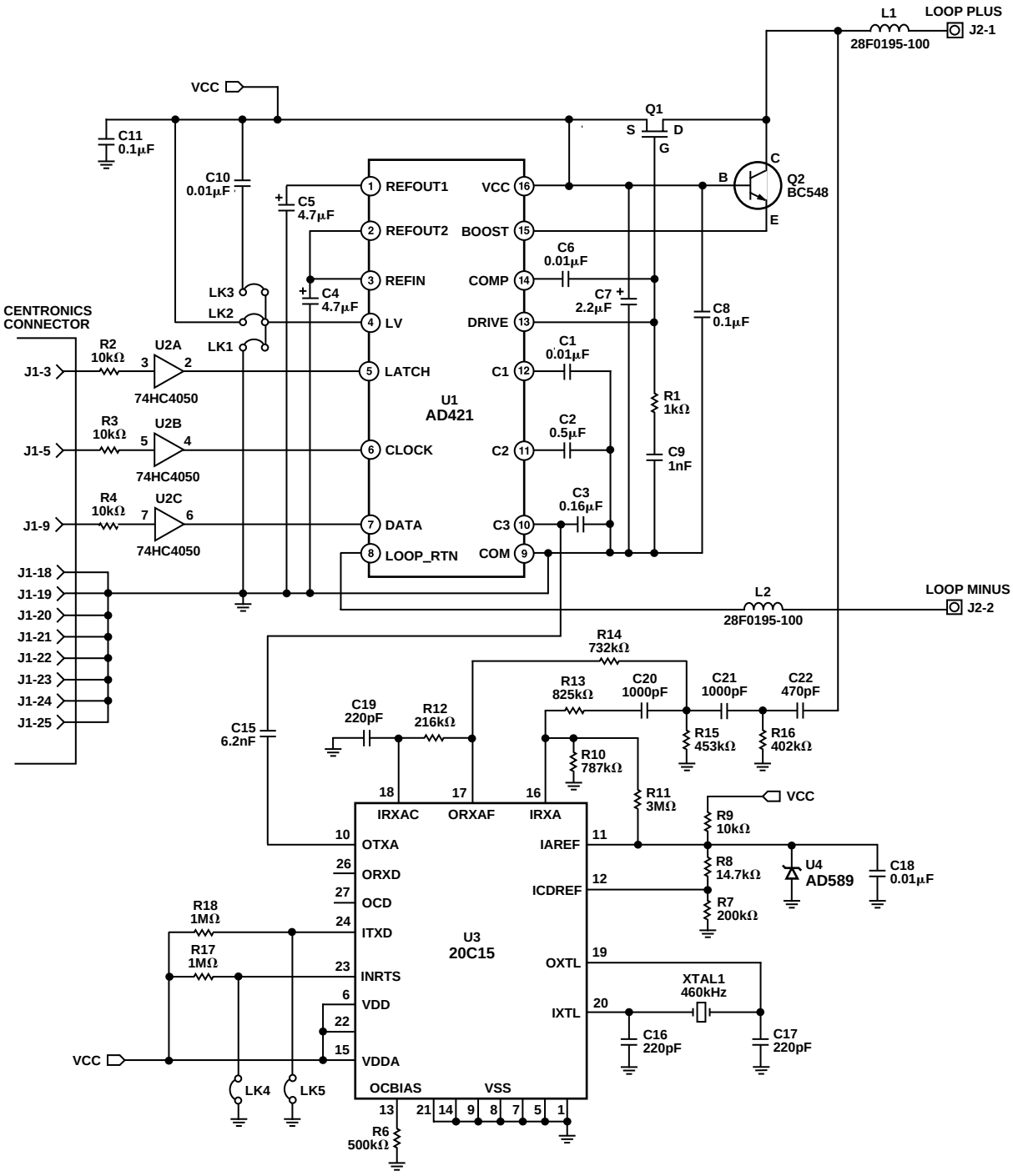

Figure 4. AD421-20C15 Interface Circuit Diagram

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