INTERNATIONAL CMOS TECHNOLOGY INC

ICT ANNOUNCES FULL PRODUCTION OF ENHANCED CMOS SERIAL EEPROM

For Immediate Release

September 10, 1990

San Jose, California, September 10th, 1990 - International CMOS Technology, Incorporated announced today the immediate availability of the 93C46A, a 1K-bit CMOS Serial EEPROM. ICT announced the 93C46, the first 5 volt only CMOS Serial EEPROM in 1984.

The 93C46A is targeted for low cost, low power microcomputer based systems such as telephones, cameras, VCRs, pagers, meters, modems, electronic appliances, alarms, locks, and automobile systems.

The 93C46A is the industry's fastest with a maximum operating frequency of 2MHz. This allows data to be written to and read from the device via a four line serial interface. This interface can easily be controlled from I/O port pins from most 4-bit or 8-bit microcontrollers. The 93C46A offers 1024 bits of non-volatile read/write memory and is organized into 64 registers of 16 bits per register.

More

Additional benefits of the 93C46A include:

* Ultra low power consumption. During active operation this device requires a maximum of 3mA of current. In CMOS stand-by, current consumption is reduced to less than 50uA.
* Software write protection and a ready-busy status signal indication.
* Hardware write protection capability.
* Auto erase write instruction, which eliminates the need for an ERASE command before every WRITE instruction.
* Space saving 8 pin DIP or surface mount packaging.

In 1990 there will be an estimated 145 million serial EEPROMS sold, by 1994 this number will reach 310-315 million units. "With this type of increasing demand, we are pleased to offer the 93C46A to our customers. The additional features are simply a case of listening to customers needs and delivering what they want," stated Robin Jigour, director of marketing. Pricing for the 93C46A is $0.70 in 1,000 piece quantities.

International CMOS Technology, Inc. (ICT) designs, manufactures and markets user programmable integrated circuits. ICT's products include a variety of memory and logic devices, and the development tools for designing with user programmable products. ICT is publicly owned and traded Over The Counter (pink sheets).

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* Source: Instat

INTERNATIONAL CMOS TECHNOLOGY, INC.

August 1990

93C46A
1,024-Bit Serial (5V only) CMOS Electrically Erasable Programmable Read Only Memory (EEPROM)

Features

- **Advanced CMOS EEPROM Technology**
- **Read/Write Non-volatile Memory**
  - Single 5V supply operation
  - 1,024 bits: 64 x 16 organization
  - Versatile, easy to use serial data interface
- **Low Power Consumption**
  - 3mA max Active
  - 1mA max Standby, TTL interface
  - 50µA max Standby, CMOS interface
- **Special Features**
  - Automatic-erase write instruction
  - Ready/Busy status signal
  - Software and hardware controlled write protection
- **Ideal For Low-Density Data Storage**
  - Low cost, space saving, 8-pin package
  - Commercial, industrial, & military versions
  - Interfaces with popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 8096, 6805, 6801, TMS1000, Z8)
- **Application Versatility**
  - Alarms, Electronic Locks, Appliances, Terminals, Smart Cards, Robotics, Meters, Telephones, Tuners, etc.
- **Reliability**
  - 10,000 erase/write cycles
  - Over 40 year data retention[1]

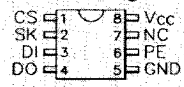
General Description

The ICT 93C46A is a 1,024-bit, 5V-only, serial read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. Its 1,024 bits of memory are organized into 64 registers each. Each register is individually addressable for serial read or write operations. A versatile serial interface consisting of chip select, clock, data-in and data-out, can easily be controlled by popular microcomputers (ie., COP4XX, 8048, 8049, 8051, 6805, 6801, TMS1000,Z8) or standard microprocessors.

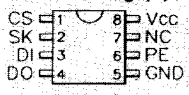
Low power consumption, low cost, and space efficiency make the ICT 93C46A an ideal candidate for high volume, low density data storage applications. Special features of the 93C46A include: automatic write time-out, ready/busy status signal, software controlled write protection, and ultra-low standby power mode when deselected (CS low). Additionally, the 93C46A offers functional compatibility with existing NMOS and CMOS serial EEPROMs. The 93C46A is designed for applications requiring 10,000 erase/write cycles per register and 40 years of data retention.

Connection Diagrams

DIP Package



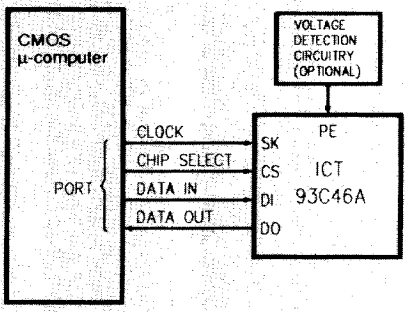
SO8 Package(K)



SO8 Package(S)

Pin Names

CS	= Chip Select
SK	= Serial Data Clock
DI	= Serial Data Input
DO	= Serial Data Output
PE	= Program Enable
GND	= Ground
Vcc	= Power Supply



Interfacing the 93C46A

Function Description

Device Operation[2]

The ICT 93C46A is a serial 1,024-bit non-volatile memory device organized as 64 registers by 16 bits. Each register is independently addressable for read, write, or erase operations. Five, 9-bit instructions control the operation of the device. The 93C46A operates on a single 5 Volt supply, and will generate, on chip, the high voltage required for any programming operation.

The 93C46A provides two methods of protecting data from being accidentally disturbed. The erase/write-disable (EWDS) instruction will disable all programming functions until an erase/write-enable (EWEN) instruction is executed. A hardware control is also available in the form of the PE (program enable) control pin. To perform any programming instruction, PE must be held high while loading the instruction into the 93C46A. The PE control can be used to ensure that no data is accidentally disturbed by erratic switching of the microcontroller's outputs during power-up or power-down. Voltage detection circuitry can be implemented to disable PE when the supply voltage drops below a user-specified voltage level. Note that the PE control pin is tied to an internal pull-up so that the pin may be left unconnected if the PE control feature is not to be used.

Instructions, address, and write data are clocked into the DI pin on the rising edge of the clock (SK). The instructions include: read; write; erase/write enable, erase/write disable; erase all; and write all. The format of each 9-bit instructions-starting with the most significant bit-is as follows: start bit (logical "1"); a two-bit op code; and an eight-bit address. The DO pin is normally in a high-impedance state, except when reading data from the device, or when checking the BUSY/READY status after a programming operation. The BUSY/READY status can be determined after a programming operation by selecting the device (CS high) and polling the DO pin. DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready for the next operation. DO will return to the high-impedance state when the next instruction is initiated.

Read (READ)

The read (READ) instruction outputs serial data on the DO pin. After a read instruction is received, the instruction and the address are decoded. Then data is transferred from the selected memory register to a 16-bit shift register and DO comes out of the high-impedance state. After sending a dummy bit (logical "0"), the 16-bit data string is shifted out of the device. The DO transitions occur on the rising edge of the clock and the data is stable after the specified delay t_{PO} or t_{PD1}.

Write Enable and Disable[3] (WEN and WDS)

The 93C46A powers up in the programming-disable state. Any programming after power-up, or following a write disable (WDS) instruction, must first be preceded by a write enable (WEN) instruction. The PE pin **MUST** be held high while loading the programming enable instruction. Once enabled, programming remains enabled until a write disable (WDS) instruction is executed or power is removed from the device. The write disable instruction disables all programming functions of the 93C46A and can be used to prevent accidentally disturbing data in the device. Data can be read from the 93C46A regardless of the programming enable/disable status.

Write (WRITE)[3]

The 93C46A initiates an autoerase cycle when executing a write (WRITE) instruction, eliminating the need of an erase (ERASE) command. The write instruction (opcode plus address) is followed by 16 bits of data to be written into the specified address. After the last bit of data (D_0) has been clocked into the DI pin, the CS (chip select) must be brought low before the next rising edge of the SK clock and held low for the minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the write instruction. However, after loading the write instruction the PE pin becomes a "don't care". It is not necessary to clock the SK pin after initiating the self-timed write mode. The READY/BUSY status of the device can be determined by selecting the device and polling the DO pin.

Write All (WRAL)[3]

The write-all (WRAL) instruction simultaneously programs all registers with the data pattern specified in the instruction. After receiving the write-all instruction and 16 bits of data, CS (chip select) must be held low for a minimum period specified by t_{CS}. The falling edge of CS initiates the self-timed write cycle. The PE pin **MUST** be held high while loading the write-all instruction. It is not necessary to clock the SK pin after initiating the self-timed write-all mode. The BUSY/READY status of the device can be determined by selecting the device and polling the DO pin.

Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damag

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.6 to +7.5	V
V_{IO}	Voltage Applied to Any Pin	Relative to GND	− 0.6 to V_{CC} + 0.6	V
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Commercial 93C46A		Industrial 93C46A (I)		Military 93C46A(M)		Unit
		Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
T_A	Ambient Temperature[1]	0	+ 70	− 40	+ 85	− 55	+ 125	°C

DC and AC Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	93C46A		93C46A I		93C46A M		Unit
			Min	Max	Min	Max	Min	Max	
I_{CC}	Power Supply Current, Active, TTL/CMOS Interface	V_{CC} = 5.5V, CS=SK=V_{IH} DO = Open, f = 2.0MHz		3		5		7	mA
I_{CCSB1}	Supply Current, Standby, TTL Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		1		1		2	mA
I_{CCSB2}	Supply Current, Standby, CMOS Interface	V_{CC} = 5.5V, CS = V_{IL} DO = Open		50		100		200	µA
V_{IH}	Input HIGH Level		2.0	V_{CC}+1	2.0	V_{CC}+1	2.0	V_{CC}+1	V
V_{IL}	Input LOW Level		− 0.1	0.8	− 0.1	0.8	− 0.1	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = − 0.4mA (note 2)	2.2		2.2		2.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA (note 2)		0.4		0.4		0.4	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V		±10		±10		±10	µA
I_{LO}	Output Leakage Current	V_O=5.5V, CS=0, V_{CC} ≤ 5.5V		±10		±10		±10	µA
t_{SKP}	SK Period		500		500		1000		ns
t_{SKW}	SK Pulse Width	High or Low	200		200		400		ns
t_{CSS}	CS High to SK High Delay		100		100		200		ns
t_{CSH}	SK Low to CS Low Delay		0		0		0		ns
t_{DIS}	Data Setup Time (Write)		200		200		400		ns
t_{DIH}	Data Hold Time (Write)		200		200		400		ns
t_{PD1} / t_{PD0}	Serial Clock to Output Delay	C_L = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V, V_{IL} = 0.45V, VIH = 2.4V		250		250		500	ns
$t_{E/W}$	Self-timed Program Cycle[4]			10		10		20	ms
t_{CS}	Min CS Low Time		250		250		250		ns
t_{SV}	CS to Status Valid	CL = 100pF		500		500		1000	ns
t_{OH}, t_{IH}	Falling Edge of CS to DO High Impedence			100		100		200	ns

Notes

Note 1. ICT's E^2 devices are designed to endure 10,000 Erase/Write cycles and to retain data for at least forty years while operating at 55°C. ICT's standard test flow verifies at least ten years of data retention for Commercial and Industrial temperature devices and at least two years data retention for Military temperature devices. Data retention verification is performed on 100% of the units being shipped. Cycling endurance is verified by lot-sample testing.

Note 2. If the power is removed or the CS pin is brought low during an instruction cycle, the device's instruction registers will be reset. Note that a power-down will totally reset the device. This means that the write-enable instruction (WEN) will need to be executed prior to any programming.

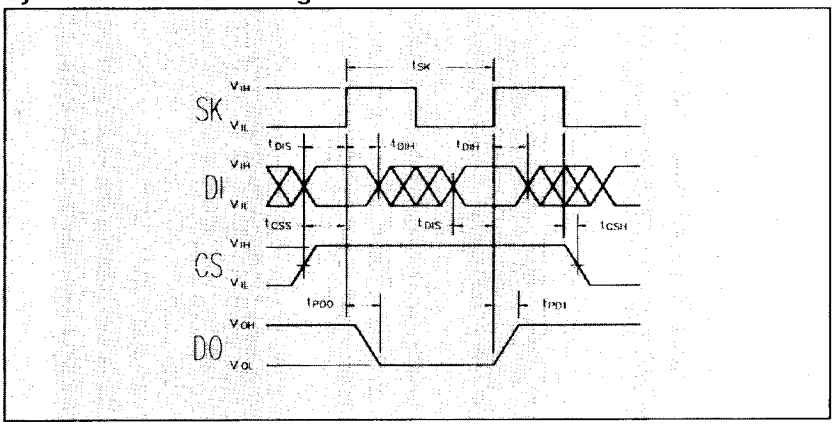
Note 3. If the PE pin is brought to low during the loading of the instruction, this instruction (WEN, WDS, WRITE, and WRAL) may not be executed reliably.

Note 4. Although the 93C46A self-timed program cycle allows software delay loops to be used to achieve the necessary Erase/Write delay, using the Ready/Busy feature is recommended instead. Using the Ready/Busy feature allows faster response time since t_{EW} will typically be less than the maximum specification.

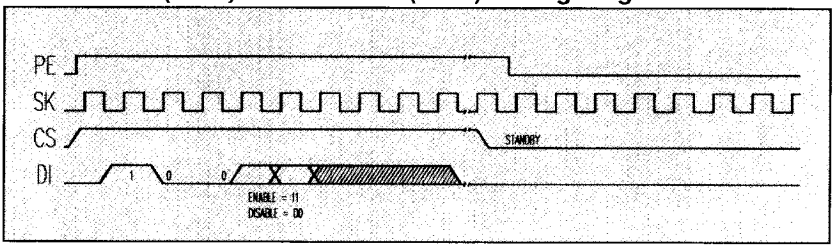
Instruction set for the 93C46A

Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	10	$A_5A_4A_3A_2A_1A_0$		Read address
WRITE	1	01	$A_5A_4A_3A_2A_1A_0$	D_{15} - D_0	Write to address
WEN	1	00	1 1 X X X X		Write enable
WDS	1	00	0 0 X X X X		Write disable
WRAL	1	00	0 1 X X X X	D_{15} - D_0	Write all addresses

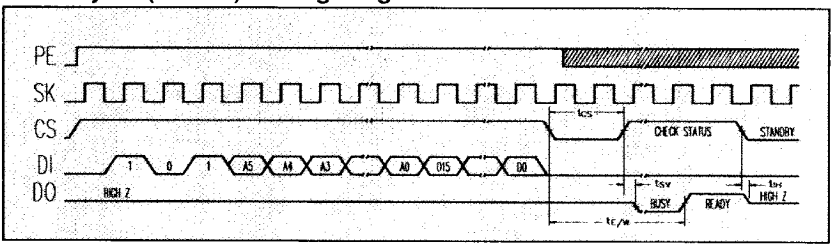
Synchronous Data Timing Waveforms



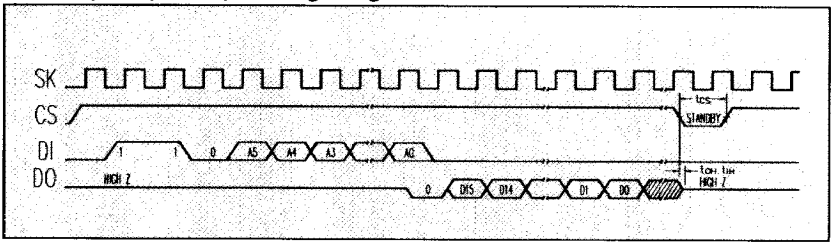
Write Enable (WEN)/Write Disable (WDS) Timing Diagram



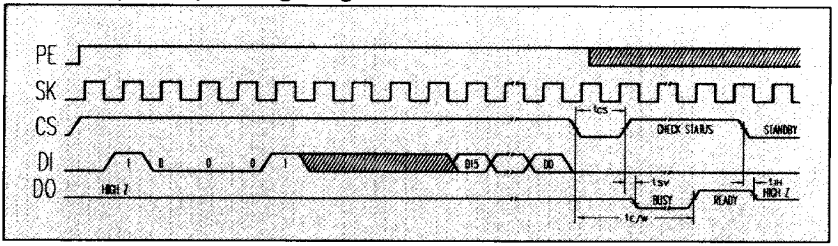
Write Cycle (WRITE) Timing Diagram



Read Cycle (READ) Timing Diagram



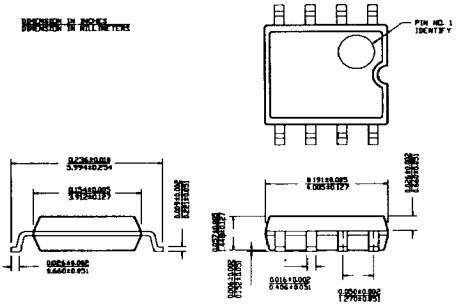
Write All (WRAL) Timing Diagram



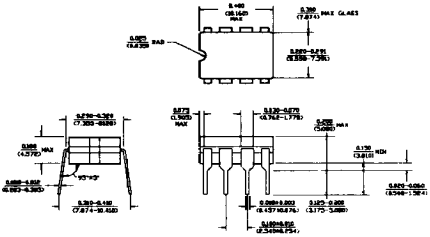
Physical Dimensions

All dimensions are in inches (millimeters)

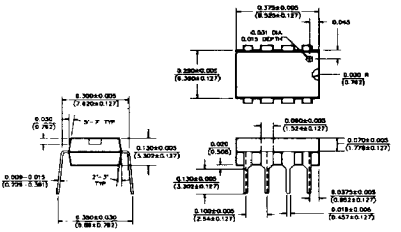
SOIC



Ceramic Dip



Molded DIP



Preliminary Designation

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INTERNATIONAL CMOS TECHNOLOGY, INC.
2125 Lundy Avenue
San Jose, California 95131
Telephone (408) 434-0678
TWX (901) 997-1531
FAX (408) 434-0688