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82551ER Fast Ethernet PCI Controller

Stepping Information

July 2005

Revision 1.3

Notice: The 82551ER Fast Ethernet Controller may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this document.

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Revision History

Date	Version	Description
Mar. 2003	1.0	Initial release.
July 2004	1.1	Added information for the 82551ER Component Marking Identification section.
August 2004	1.2	Removed Errata 3, "MDI/MDI-X Feature Not Supported". This feature is now supported. Removed Documentation Changes section.
July 2005	1.3	Deleted Erratum #3.

Preface

This document is an update to the specifications contained in the 82551ER Fast Ethernet PCI Controller Datasheet, and contains issues affecting all design using the 82551ER device.

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Document Changes.

All changes, errata, and clarifications described in this document will be incorporated into the next release of the 82551ER datasheet.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the 82551ER's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Product Code

The product ordering code for the 82551ER is: GD82551ER.

Identification Information

82551ER Component Marking Identification

The component marking identification and top marking diagram will be included in a future revision of this document.

Device	Stepping	Top Marking	Q-specification	MM Number	Notes
82551ER	A0	82551ER			
82551ER	A1	82551ER		844686	Tape and Reel
82551ER	A1	82551ER		844687	Tray

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82551ER steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes used in summary table:

X:	Specification Change, Erratum, or Specification Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This Item is either new or modified from the previous version of the document.

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No.	A-0	A-1	Plans	SPECIFICATION CHANGES	Page
1	x	x	SDM1.2	Unsupported End of List (EL) Bit in High Priority Queue	4
No.	**A-0**	**A-1**	**Plans**	**ERRATA**	**Page**
1	x	x	NoFix	Incorrect CIS Read Accesses After Power Up	5
2	x	x	NoFix	Link Loss Deep Power Down Noise Sensitivity	5
3	x	x	Fixed	Deleted	6
No.	**A-0**	**A-1**	**Plans**	**SPECIFICATION CLARIFICATIONS**	**Page**
1	x	x		PCI Buffer Leakage when the Voltage Input/Output (VIO) Pin Not Powered	7

NOTE: The table uses the following abbreviations for listed documents.
DS: Data Sheet
SDM: Software Developer's Manual
EDS: External Data Specification
AP: Application Note

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Specification Changes

1. Unsupported End of List (EL) Bit in High Priority Queue

Explanation: If High Priority Queue (HPQ) is used, the End of List (EL) bit in the command word of an HPQ or Low Priority Queue (LPQ) is not supported as an identification for the end of the Command Block List (CBL). Software drivers should only use the Start (S) bit in the header to identify the end of a CBL in a HPQ.

Implication: This change affects only software drivers that add support for multiple priority queues. It does not affect existing drivers.

Status: The appropriate definition changes will be made to all relative documents.

Errata

1.   Incorrect CIS Read Accesses After Power Up

Problem: When the 82551ER is configured for CardBus operation, it assumes that any Card Information Structure (CIS) read access from software waits one millisecond after the Reset signal is de-asserted. This allows EEPROM accesses to complete before CIS transactions are initiated. An EEPROM read before 1 ms may cause incorrect CIS transactions.

Implication: An EEPROM read performed prior to 1 ms after the Reset signal is de-asserted can cause incorrect CIS transactions.

Workaround: CIS access from PCI should be restricted to start only 1 ms after the Reset signal is de-asserted.

Status: There are no plans to fix this erratum at this time.

2.   Link Loss Deep Power Down Noise Sensitivity

Clarification: The 82551ER supports Deep Power Down on link loss. This feature enables the 82551ER to shut down when cable or activity from its link partner is present. If this feature is enabled, the powered down 82551ER physical layer (PHY) unit can be turned on by excessive noise. The 82551ER threshold values were chosen to work with existing devices on the market, with the goal of enabling the PHY unit over disabling the PHY in ambiguous situations.

Implication: The 82551ER may not be able to remain in the deep power down mode in noisy environments. This is not a serious concern because of the 82551ER's general low power consumption and its ability to shut down all but the PHY in this situation.

Workaround: Several changes can be made to the line interface to limit noise. These changes are only required on the receive differential pair of the device. This includes adding a capacitance between the receive pair (RDP and RDN). Additional capacitance between the receive pair helps filter the differential noise but may have a negative impact on the receive performance and on receive return loss. A capacitor value above 15 pF may impact performance and should be disconnected after link is achieved.

Status: There are no plans to fix this erratum at this time.

3.   Deleted

Specification Clarifications

1.   PCI Buffer Leakage when the Voltage Input/Output (VIO) Pin Not Powered

Clarification: When the system is in a suspended state (Voltage Input/Output [VIO] pin equals 0 volts and power equals 3.3 volts), the 82551ER PCI I/O buffers can rise to about 700 mV causing a leakage current to flow into the VIO pin. A resistor value greater than 100 KΩ is recommended in some of the application notes relating to 82551ER based designs. In 82551ER designs, it is also recommended that the VIO pin is pulled to the 5 V supply in a 5 V PCI signaling environment and a 3.3 V supply in 3.3 V signaling environment. If an auxiliary power supply (standby power) is available, the VIO should be connected to it.

Implication: The 82551ER VIO pin should be active whenever the device is active. This provides the lowest power consumption in suspended states.

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