CY7C4255
CY7C4265

8K/16Kx18 Deep Sync FIFOs

Features

- **High-speed, low-power, first-in first-out (FIFO) memories**
- **8K x 18 (CY7C4255)**
- **16K x 18 (CY7C4265)**
- **0.5 micron CMOS for optimum speed/power**
- **High-speed 100-MHz operation (10 ns read/write cycle times)**
- **Low power — I_{CC}=45 mA**
- **Fully asynchronous and simultaneous read and write operation**
- **Empty, Full, Half Full, and programmable Almost Empty and Almost Full status flags**
- **TTL compatible**
- **Retransmit function**
- **Output Enable ($\overline{OE}$) pins**
- **Independent read and write enable pins**
- **Center power and ground pins for reduced noise**
- **Supports free-running 50% duty cycle clock inputs**
- **Width Expansion Capability**
- **Depth Expansion Capability**
- **64-pin PLCC and 64-pin TQFP**
- **Pin-compatible density upgrade to CY7C42X5 family**
- **Pin-compatible density upgrade to IDT72205/15/25/35/45**

Functional Description

The CY7C4255/65 are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide and are pin/functionally compatible to the CY7C42X5 Synchronous FIFO family. The CY7C4255/65 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

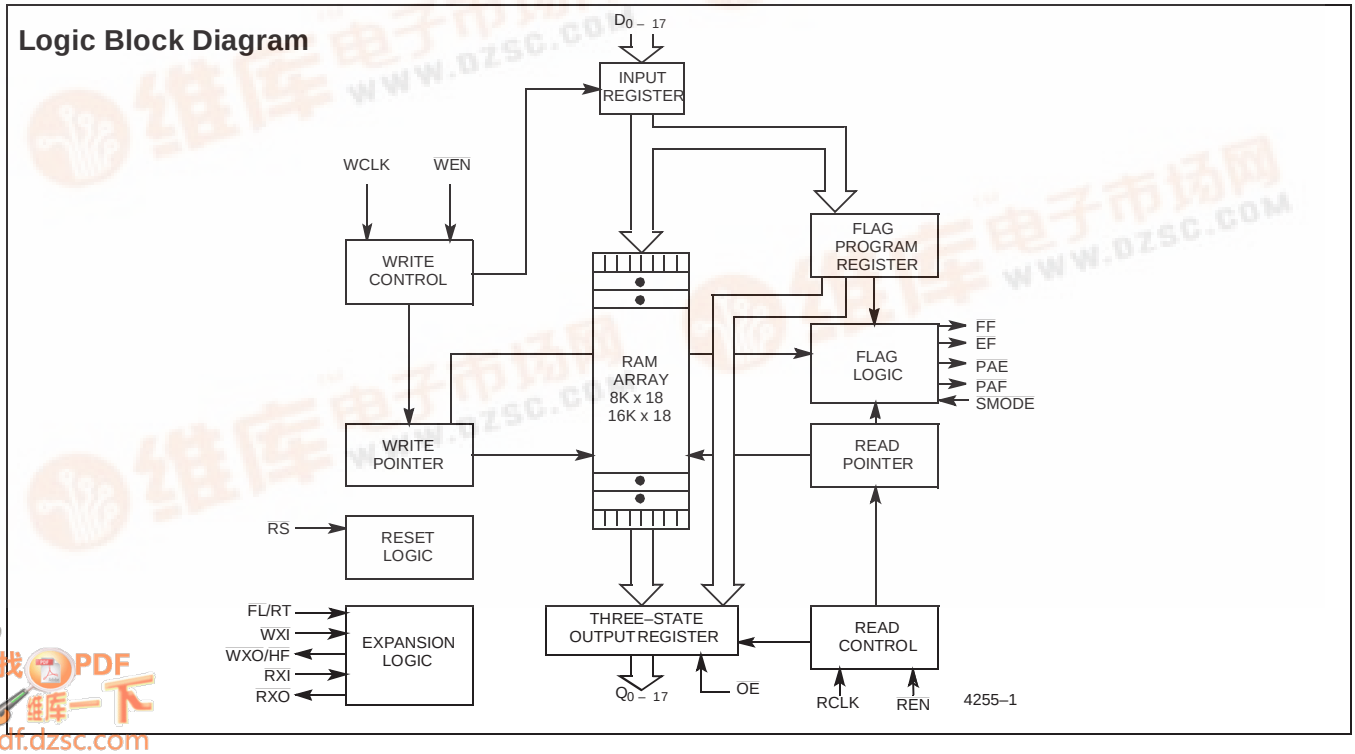
These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and a write enable pin ($\overline{WEN}$).

When $\overline{WEN}$ is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN}$ is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and a read enable pin ($\overline{REN}$). In addition, the CY7C4255/65 have an output enable pin ($\overline{OE}$). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices.

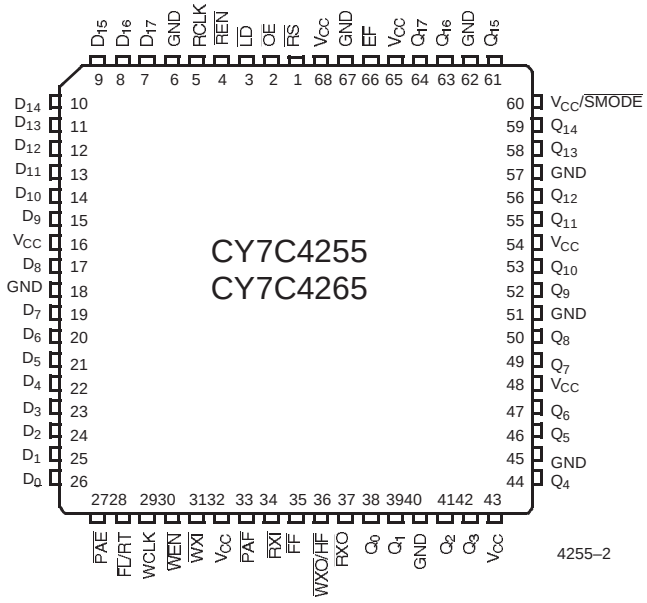
Depth expansion is possible using the cascade input ($\overline{WXI}$, $\overline{RXI}$), cascade output ($\overline{WXO}$, $\overline{RXO}$), and First Load ($\overline{FL}$) pins. The $\overline{WXO}$ and $\overline{RXO}$ pins are connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the next device, and the $\overline{WXO}$ and $\overline{RXO}$ pins of the last device should be connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS} and the $\overline{FL}$ pin of all the remaining devices should be tied to V_{CC}.

Logic Block Diagram

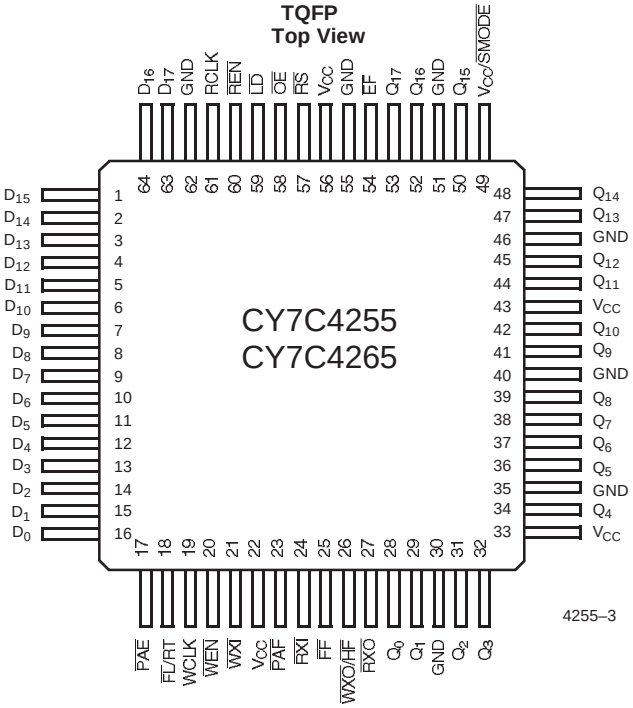


Pin Configurations

PLCC
Top View



TQFP
Top View



Functional Description (continued)

The CY7C4255/65 provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full (see *Table 2*). The Half Full flag shares the $\overline{WXO}$ pin. This flag is valid in the stand-alone and width-expansion configurations. In the depth expansion, this pin provides the expansion out ($\overline{WXO}$) information that is used to signal the next FIFO when it will be activated.

The Empty and Full flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags will remain valid from one clock cycle to the next. The Almost Empty/Almost Full flags become synchronous if the VCC/$\overline{SMODE}$ is tied to VSS. All configurations are fabricated using an advanced 0.5µ CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C4255/65–10	7C4255/65–15	7C4255/65–25	7C4255/65–35
Maximum Frequency (MHz)		100	66.7	40	28.6
Maximum Access Time (ns)		8	10	15	20
Minimum Cycle Time (ns)		10	15	25	35
Minimum Data or Enable Set-Up (ns)		3	4	6	7
Minimum Data or Enable Hold (ns)		0.5	1	1	2
Maximum Flag Delay (ns)		8	10	15	20
Active Power Supply Current (I_{CC1}) (mA)	Commercial	45	45	45	45
	Industrial	50	50	50	50

	CY7C4255	CY7C4265
Density	8K x 18	16K x 18
Package	64-pin PLCC,TQFP	64-pin PLCC,TQFP

Pin Definitions

Signal Name	Description	I/O	Function
D_{0-17}	Data Inputs	I	Data inputs for an 18-bit bus
Q_{0-17}	Data Outputs	O	Data outputs for an 18-bit bus
$\overline{WEN}$	Write Enable	I	Enables the WCLK input
$\overline{REN}$	Read Enable	I	Enables the RCLK input
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half Full Flag	O	Dual-Mode Pin: Single device or width expansion – Half Full status flag. Cascaded – Write Expansion Out signal, connected to $\overline{WXI}$ of next device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. $\overline{PAE}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to RCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to WCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, D_{0-17} (Q_{0-17}) are written (read) into (from) the programmable-flag-offset register.
$\overline{FL}$/RT	First Load/ Retransmit	I	Dual-Mode Pin: Cascaded – The first device in the daisy chain will have $\overline{FL}$ tied to V_{SS}; all other devices will have $\overline{FL}$ tied to V_{CC}. In standard mode or width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded – Tied to V_{SS}. Retransmit function is also available in stand-alone mode by strobing RT.
$\overline{WXI}$	Write Expansion Input	I	Cascaded – Connected to $\overline{WXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXI}$	Read Expansion Input	I	Cascaded – Connected to $\overline{RXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXO}$	Read Expansion Output	O	Cascaded – Connected to $\overline{RXI}$ of next device.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$V_{CC}/\overline{SMODE}$	Synchronous Almost Empty/ Almost Full Flags	I	Dual-Mode Pin Asynchronous Almost Empty/Almost Full flags – tied to V_{CC}. Synchronous Almost Empty/Almost Full flags – tied to V_{SS}. (Almost Empty synchronized to RCLK, Almost Full synchronized to WCLK.)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied –55°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .....–0.5V to +7.0V

DC Input Voltage .....–0.5V to V_{cc}+0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL–STD–883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C42X5–10		7C42X5–15		7C42X5–25		7C42X5– 35		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}[3]	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}[4]	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{CC1}[5]	Active Power Supply Current		Com'l		45		45		45		45	mA
			Ind		50		50		50		50	mA
I_{CC2}[6]	Average Standby Current		Com'l		10		10		10		10	mA
			Ind		15		15		15		15	mA

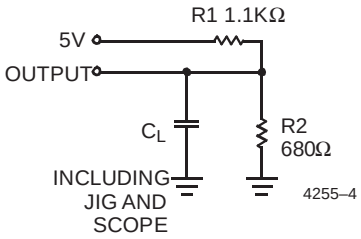
Capacitance[7,8]

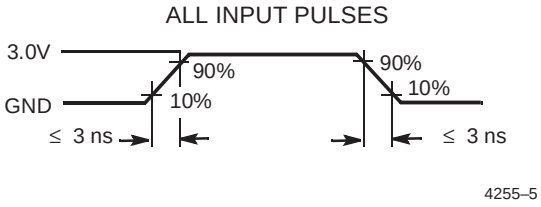
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

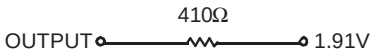
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
4. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
5. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at 20MHz, while data inputs switch at 10MHz. Outputs are unloaded. Icc1(typical) = (25mA+(freq-20MHz)*(1.0mA/MHz))
6. All inputs = V_{CC} – 0.2V, except RCLK and WCLK (which are switching at frequency = 20 MHz), and $\overline{FL}$/RT which is at V_{ss}. All outputs are unloaded.
7. Tested initially and after any design changes that may affect these parameters.
8. Tested initially and after any process changes that may affect these parameters.

AC Test Loads and Waveforms[9, 10]





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

Parameter	Description	7C42X5–10		7C42X5–15		7C42X5–25		7C42X5–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40		28.6	MHz
t_A	Data Access Time	2	8	2	10	2	15	2	20	ns
t_{CLK}	Clock Cycle Time	10		15		25		35		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		14		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		14		ns
t_{DS}	Data Set-Up Time	3		4		6		7		ns
t_{DH}	Data Hold Time	0.5		1		1		2		ns
t_{ENS}	Enable Set-Up Time	3		4		6		7		ns
t_{ENH}	Enable Hold Time	0.5		1		1		2		ns
t_{RS}	Reset Pulse Width[11]	10		15		25		35		ns
t_{RSR}	Reset Recovery Time	8		10		15		20		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25		35	ns
t_{PRT}	Retransmit Pulse Width	30		35		45		55		ns
t_{RTR}	Retransmit Recovery Time	60		65		75		85		ns
t_{OLZ}	Output Enable to Output in Low Z[12]	0		0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	3	12	3	15	ns
t_{OHZ}	Output Enable to Output in High Z[12]	3	7	3	8	3	12	3	15	ns
t_{WFF}	Write Clock to Full Flag		8		10		15		20	ns
t_{REF}	Read Clock to Empty Flag		8		10		15		20	ns
$t_{PAFasynch}$	Clock to Programmable Almost-Full Flag[13] (Asynchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns
$t_{PAFsynch}$	Clock to Programmable Almost-Full Flag (Synchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
$t_{PAEasynch}$	Clock to Programmable Almost-Empty Flag[13] (Asynchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{CC})		12		16		20		25	ns

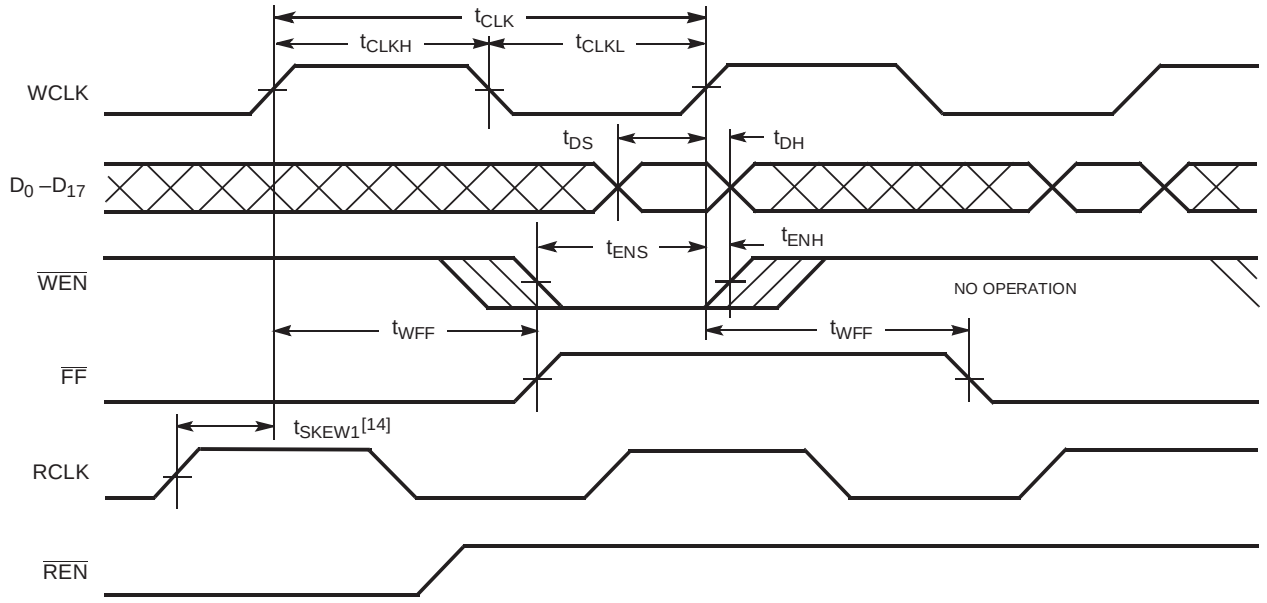
Notes:
9. C_L = 30 pF for all AC parameters except for t_{OHZ}.
10. C_L = 5 pF for t_{OHZ}.
11. Pulse widths less than minimum values are not allowed.
12. Values guaranteed by design, not currently tested.
13. $t_{PAFasynch}$, $t_{PAEasynch}$, after program register write will not be valid until 5 ns + $t_{PAF(E)}$.

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	7C42X5–10		7C42X5–15		7C42X5–25		7C42X5–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PAEsynch}$	Clock to Programmable Almost-Full Flag (Synchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})		8		10		15		20	ns
t_{HF}	Clock to Half-Full Flag		12		16		20		25	ns
t_{XO}	Clock to Expansion Out		6		10		15		20	ns
t_{XI}	Expansion in Pulse Width	4.5		6.5		10		14		ns
t_{XIS}	Expansion in Set-Up Time	4		5		10		15		ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5		6		10		12		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	5		6		10		12		ns
t_{SKEW3}	Skew Time between Read Clock and Write Clock for Programmable Almost Empty and Programmable Almost Full Flags (Synchronous Mode only)	10		15		18		20		ns

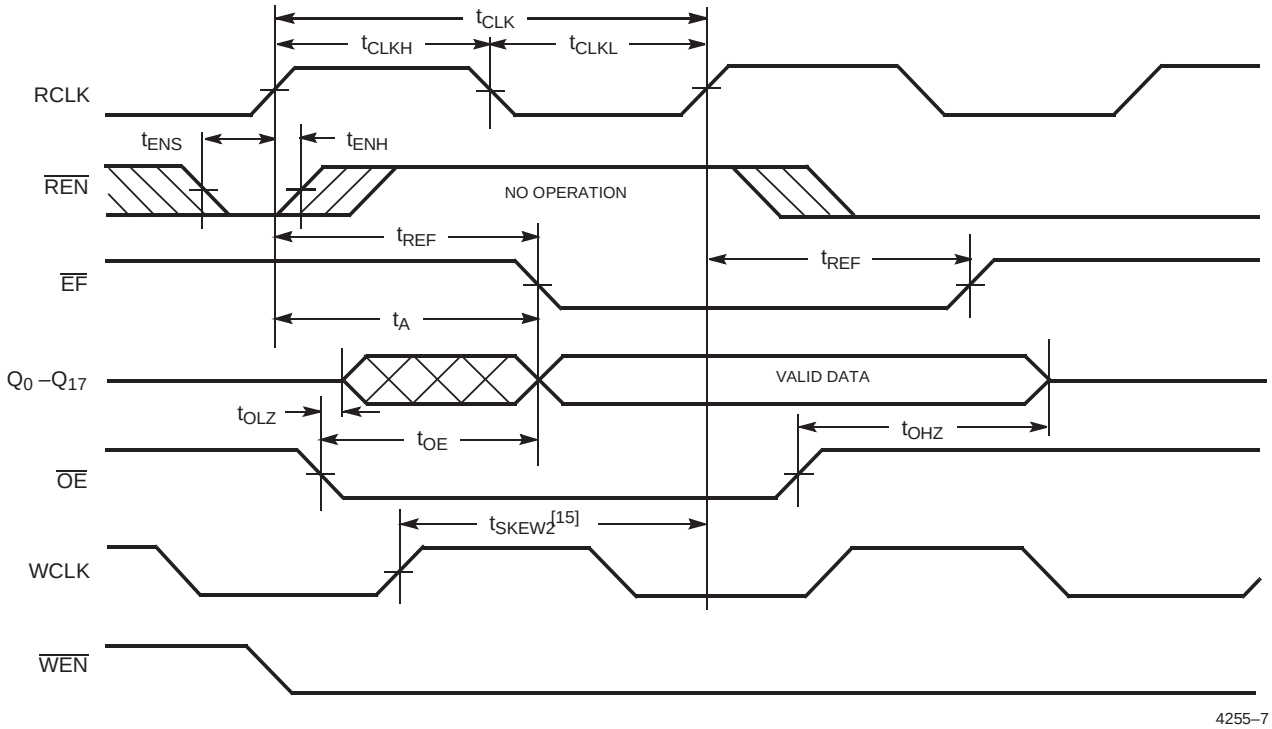
Switching Waveforms

Write Cycle Timing



4255–6

Read Cycle Timing



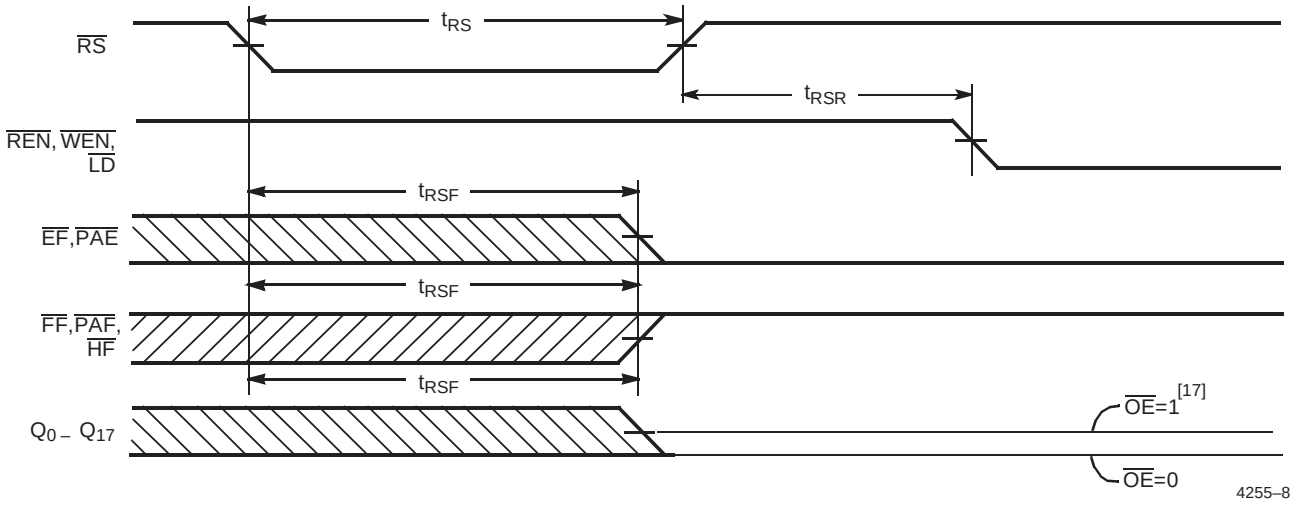
4255–7

Notes:

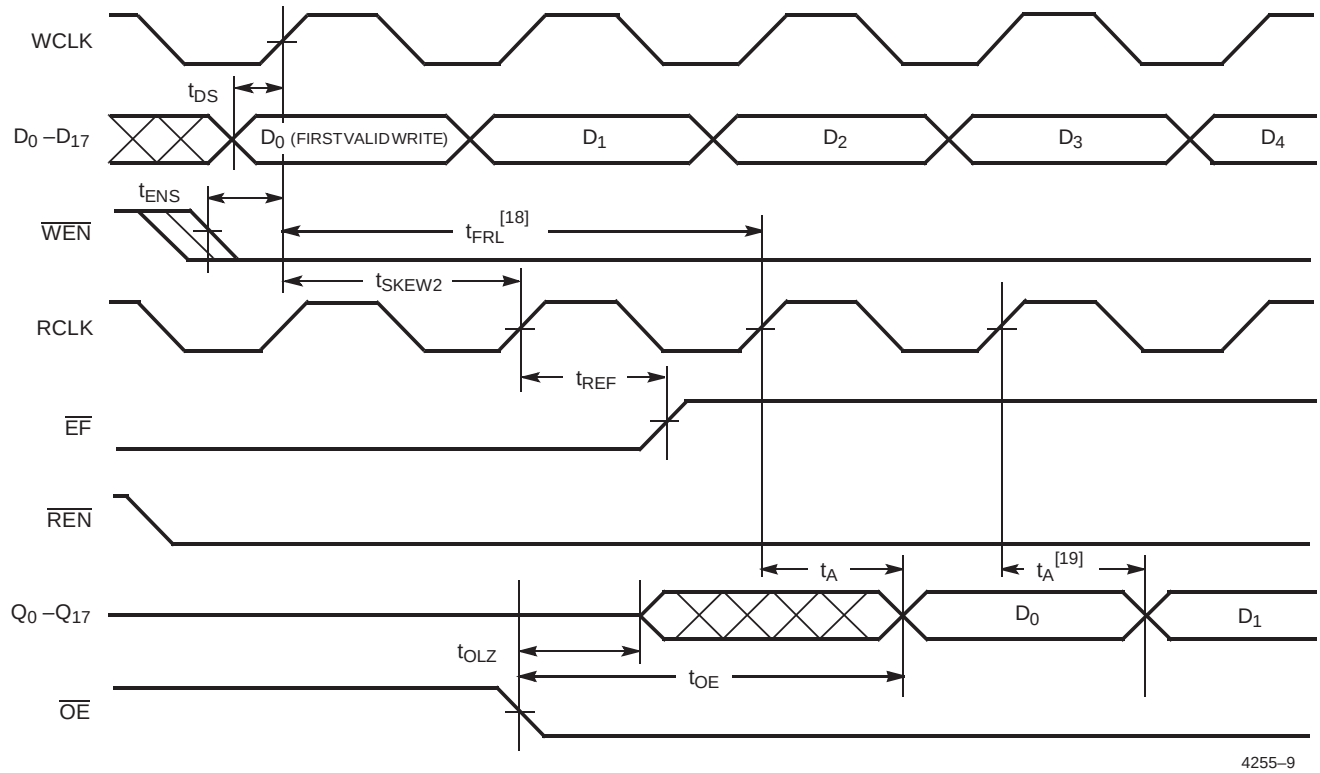
14. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
15. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Reset Timing [16]



First Data Word Latency after Reset with Simultaneous Read and Write

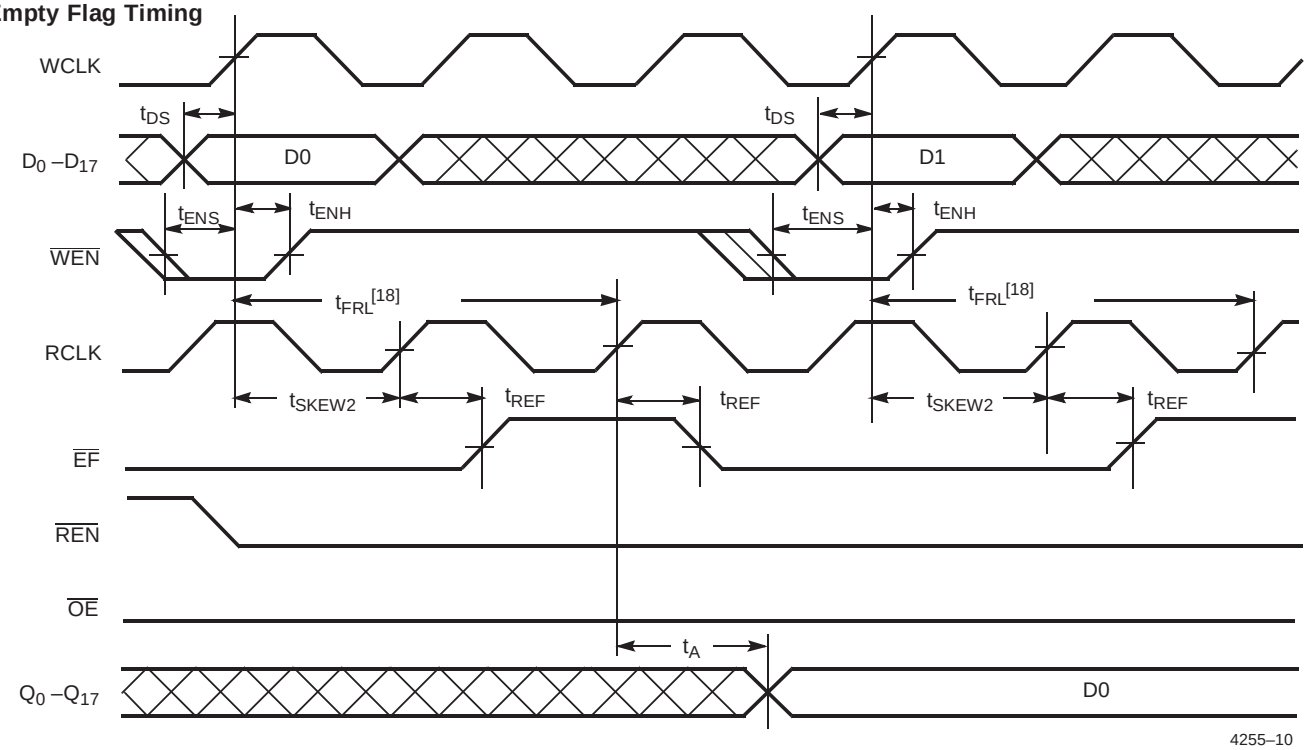


Notes:

16. The clocks (RCLK, WCLK) can be free-running during reset.
17. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
18. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When $t_{SKEW2} <$ minimum specification, t_{FRL} (maximum) = either $2*t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
19. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

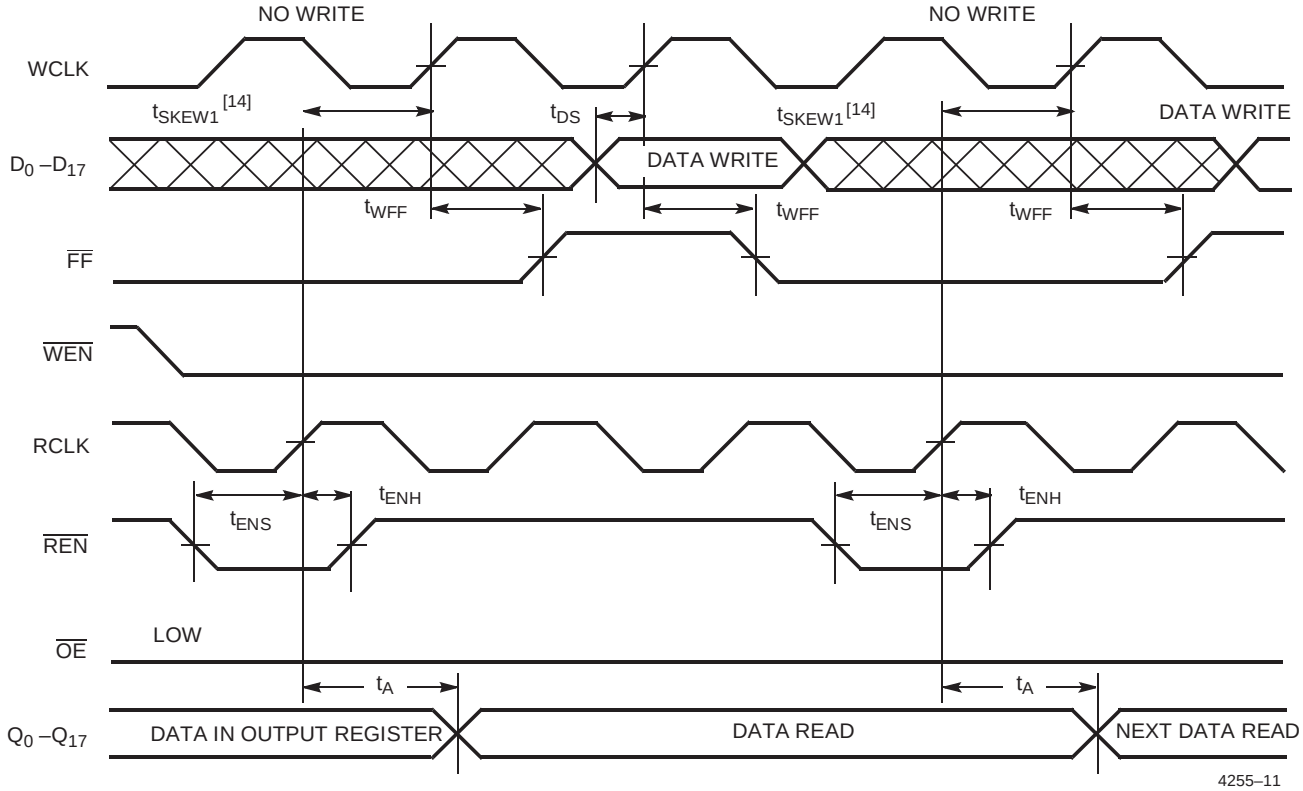
Switching Waveforms (continued)

Empty Flag Timing



4255–10

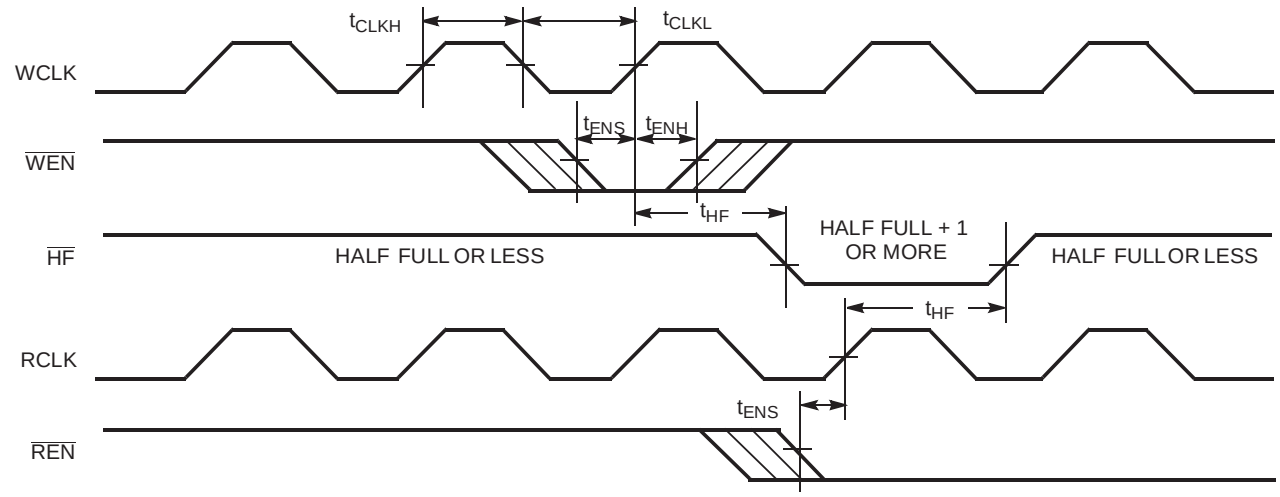
Full FlagTiming



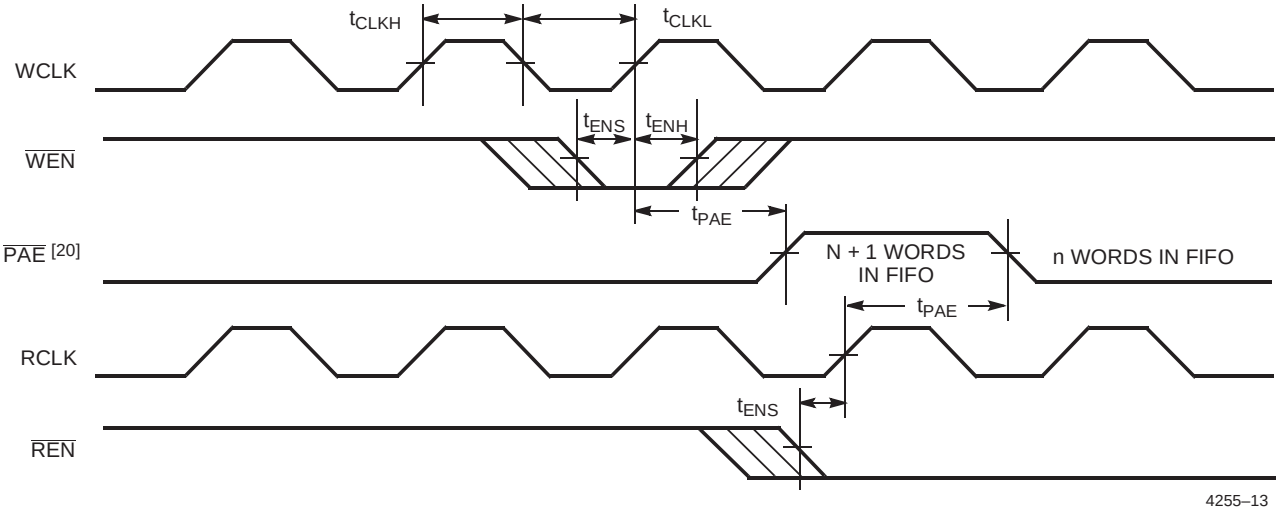
4255–11

Switching Waveforms (continued)

Half-Full Flag Timing



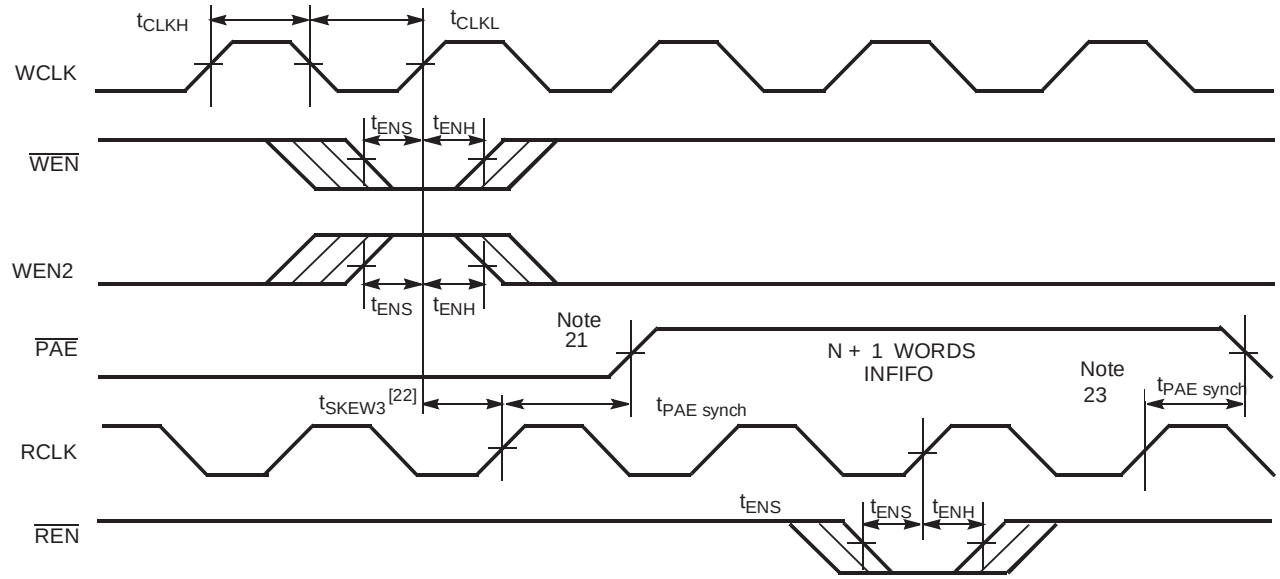
Programmable Almost Empty Flag Timing



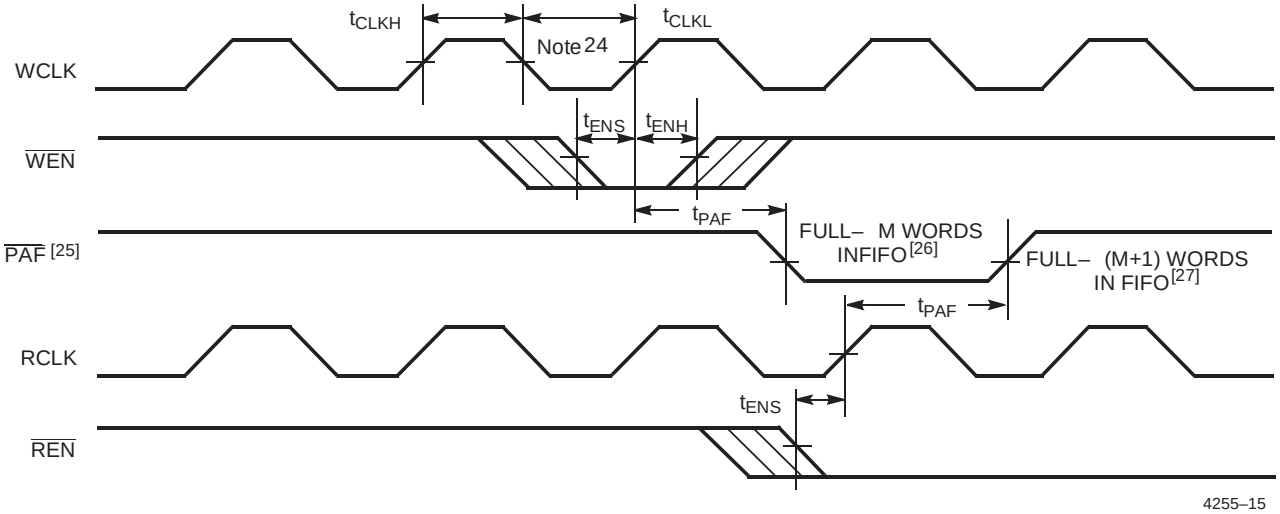
Note:
20. $\overline{PAE}$ is offset = n. Number of data words into FIFO already = n.

Switching Waveforms (continued)

Programmable Almost Empty Flag Timing (applies only in $\overline{SMODE}$ ($\overline{SMODE}$ is LOW))



Programmable Almost Full Flag Timing

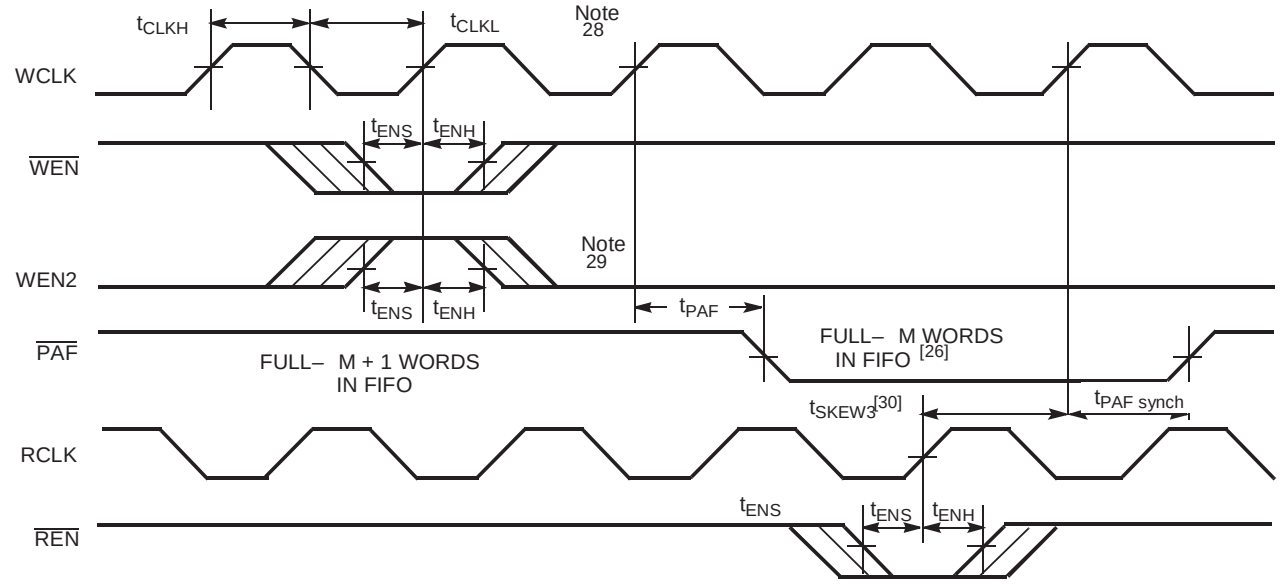


Notes:

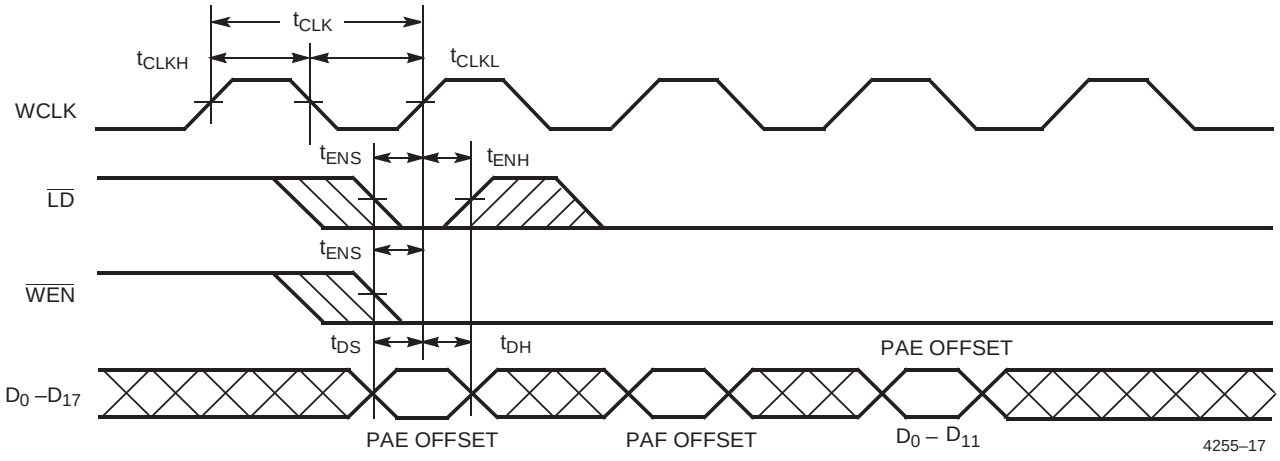
21. PAE offset – n.
22. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3}, then $\overline{PAE}$ may not change state until the next RCLK.
23. If a read is preformed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.
24. PAF offset = m. Number of data words written into FIFO already = 8192 – (m + 1) for the CY7C4255 and 16384 – (m + 1) for the CY7C4265.
25. PAF is offset = m.
26. 8192 – m words in CY7C4255 and 16384 - m words in CY7C4265.
27. 8192 – (m + 1) words in CY7C4255 and 16384 - (m + 1) CY7C4265.

Switching Waveforms (continued)

Programmable Almost Full Flag Timing (applies only in SMODE (SMODE is LOW))



Write Programmable Registers

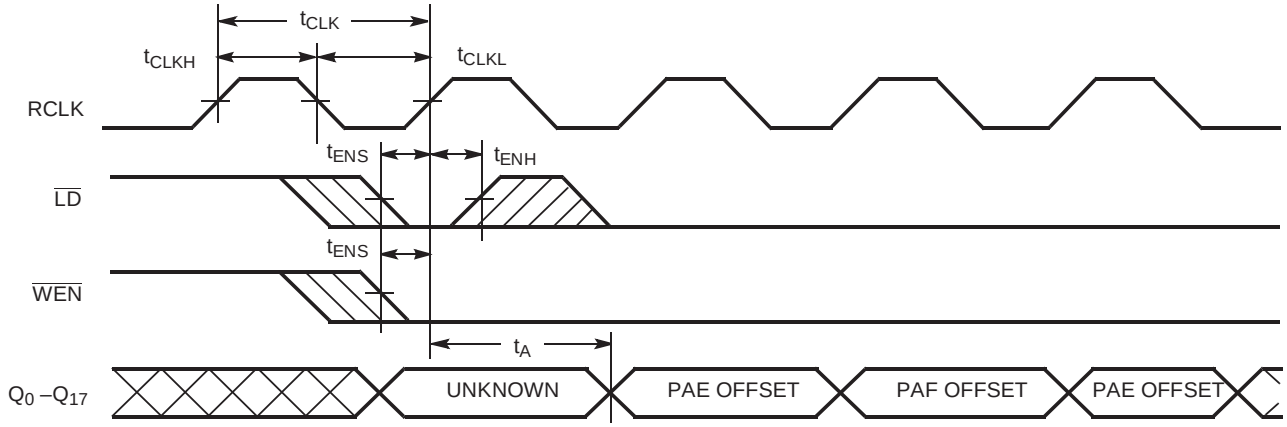


Notes:

28. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
29. PAF offset = m.
30. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for $\overline{PAF}$ to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.

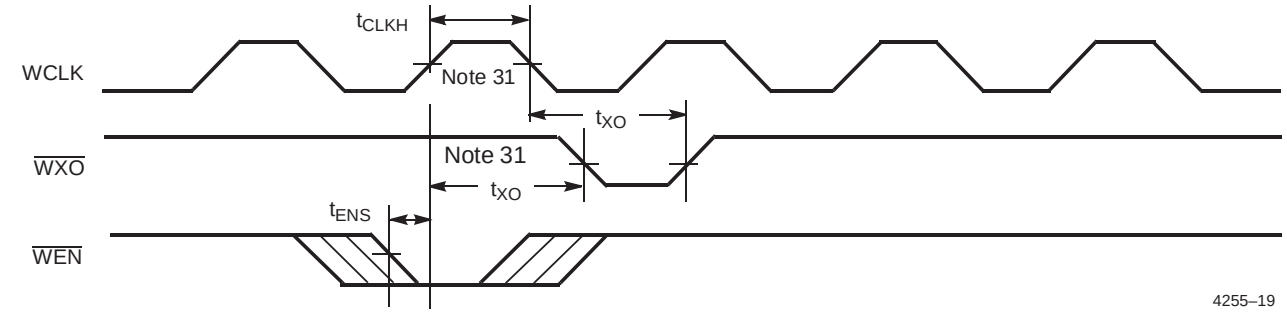
Switching Waveforms (continued)

Read Programmable Registers



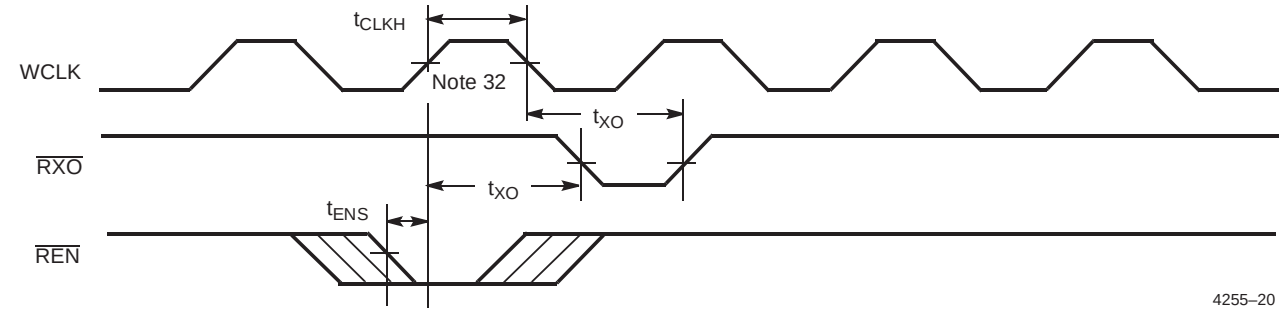
4255–18

Write Expansion Out Timing



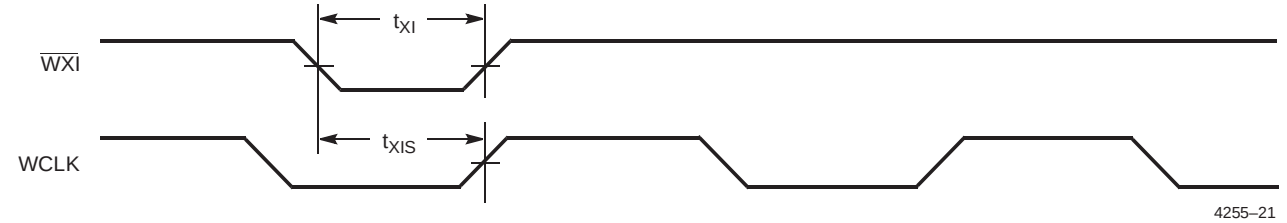
4255–19

Read Expansion Out Timing



4255–20

Write Expansion In Timing



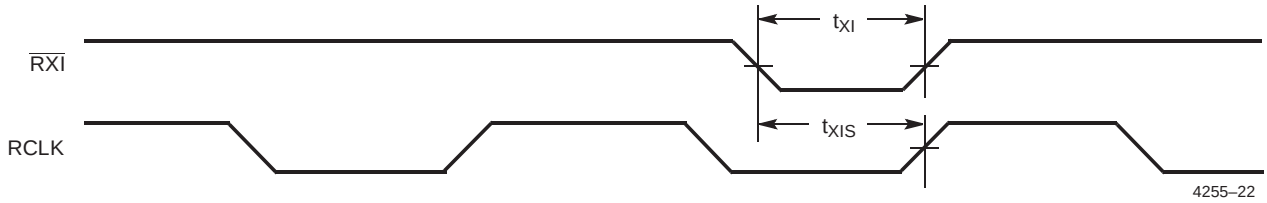
4255–21

Notes:

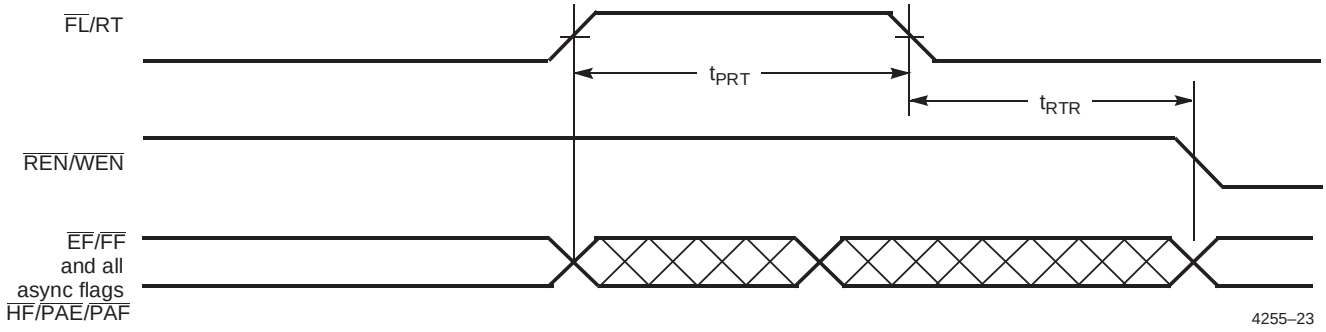
31. Write to Last Physical Location.
32. Read from Last Physical Location.

Switching Waveforms (continued)

Read Expansion In Timing



Retransmit Timing [33, 34, 35]



Notes:

33. Clocks are free running in this case.
34. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
35. For the synchronous $\overline{PAE}$ and $\overline{PAF}$ flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

Architecture

The CY7C4256/65 consists of an array of 8K/16K words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN}$, $\overline{WEN}$, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{HF}$, $\overline{PAF}$, $\overline{FF}$). The CY7C4255/65 also includes the control signals $\overline{WXI}$, $\overline{RXI}$, $\overline{WXO}$, $\overline{RXO}$ for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs go LOW after the falling edge of $\overline{RS}$ only if $\overline{OE}$ is asserted. In order for the FIFO to reset to its default state, a falling edge must occur on $\overline{RS}$ and the user must not read or write while $\overline{RS}$ is LOW.

FIFO Operation

When the $\overline{WEN}$ signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN}$ signal is active LOW, data in the FIFO memory will be presented on the Q_{0-17} outputs. New data will be presented on each rising edge of RCLK while $\overline{REN}$ is active LOW and $\overline{OE}$ is LOW. $\overline{REN}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN}$ must occur tENS before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the Q_{0-17} outputs when $\overline{OE}$ is deasserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and under flow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C4255/65 devices contain two 14-bit offset registers. Data present on D_{0-13} during a program write will determine the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see *Table 2*). When the Load $\overline{LD}$ pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D_{0-13} is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register (see *Table 1*). Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then, by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the $\overline{LD}$ pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

Table 1. Write Offset Register

$\overline{LD}$	$\overline{WEN}$	WCLK[36]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Flag Operation

The CY7C4255/65 devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. $\overline{PAE}$ and $\overline{PAF}$ are synchronous if V_{CC}/$\overline{SMODE}$ is tied to V_{SS}.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when device is Full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C4255/65 features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the $\overline{PAF}$ or $\overline{PAE}$ will be asserted, signifying that the FIFO is either Almost Full or Almost Empty. See *Table 2* for a description of programmable flags.

When the $\overline{SMODE}$ pin is tied LOW, the $\overline{PAF}$ flag signal transition is caused by the rising edge of the write clock and the $\overline{PAE}$ flag transition is caused by the rising edge of the read clock.

Note:

36. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the stand-alone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 2. Flag Truth Table

Number of Words in FIFO						
7C4255 – 8K x 18	**7C4265 – 16K x 18**	**FF**	**PAF**	**HF**	**PAE**	**EF**
0	0	H	H	H	L	L
1 to n[37]	1 to n[37]	H	H	H	L	H
(n+1) to 4096	(n+1) to 8192	H	H	H	H	H
4097 to (8192–(m+1))	8193 to (16384 –(m+1))	H	H	L	H	H
(8192–m)[38] to 8191	(16384–m)[38] to 16383	H	L	L	H	H
8192	16384	L	L	L	H	H

Notes:

37. n = Empty Offset (Default Values: CY7C4255/CY7C4265 n = 127).
38. m = Full Offset (Default Values: CY7C4255/CY7C4265 n = 127).

Width Expansion Configuration

The CY7C4255/65 can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode all control line inputs are common and all flags are available. Empty (Full) flags should be created by ANDing the Empty (Full) flags of every FIFO; the $\overline{PAE}$ and $\overline{PAF}$ flags can be detected from any one device. This technique will avoid reading data from, or writing data to the FIFO that is "staggered" by one clock cycle due to the variations in skew between RCLK and WCLK. *Figure 1* demonstrates a 36-word width by using two CY7C4255/65s.

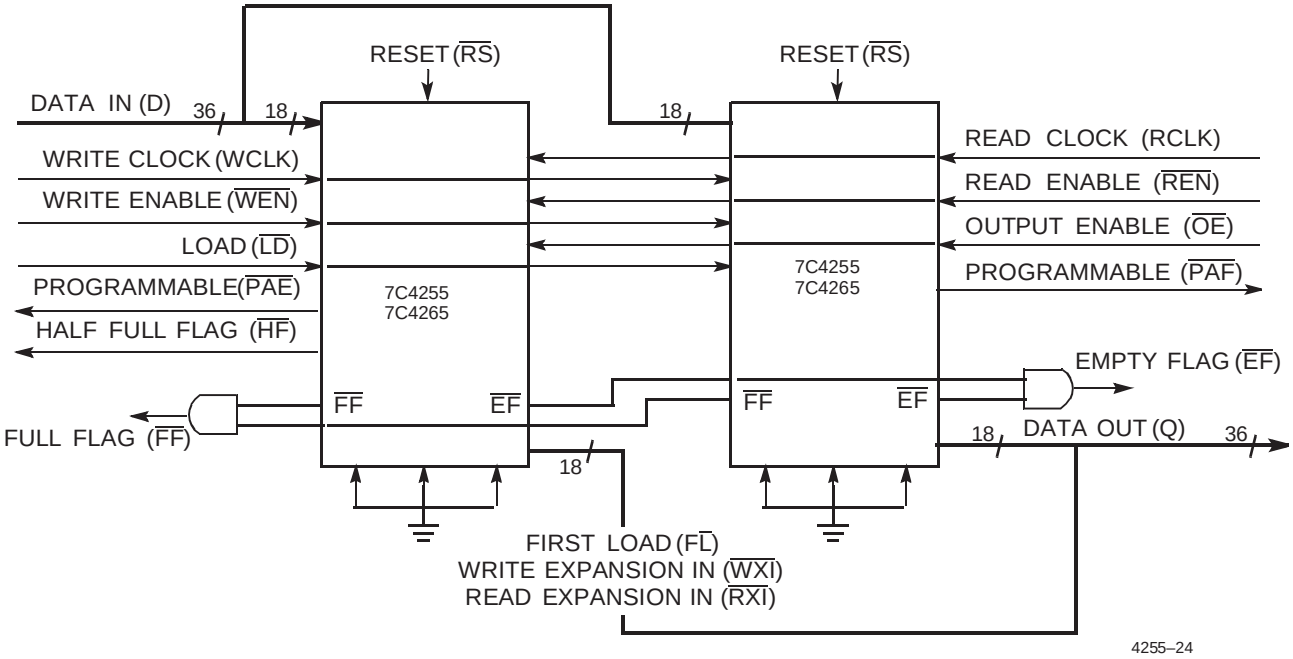


Figure 1. Block Diagram of 8K x18/16K x 18Synchronous FIFO Memory Used in a Width Expansion Configuration

Depth Expansion Configuration (with Programmable Flags)

The CY7C4255/65 can easily be adapted to applications requiring more than 8192/16384 words of buffering. *Figure 2* shows Depth Expansion using three CY7C42X5s. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together these respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

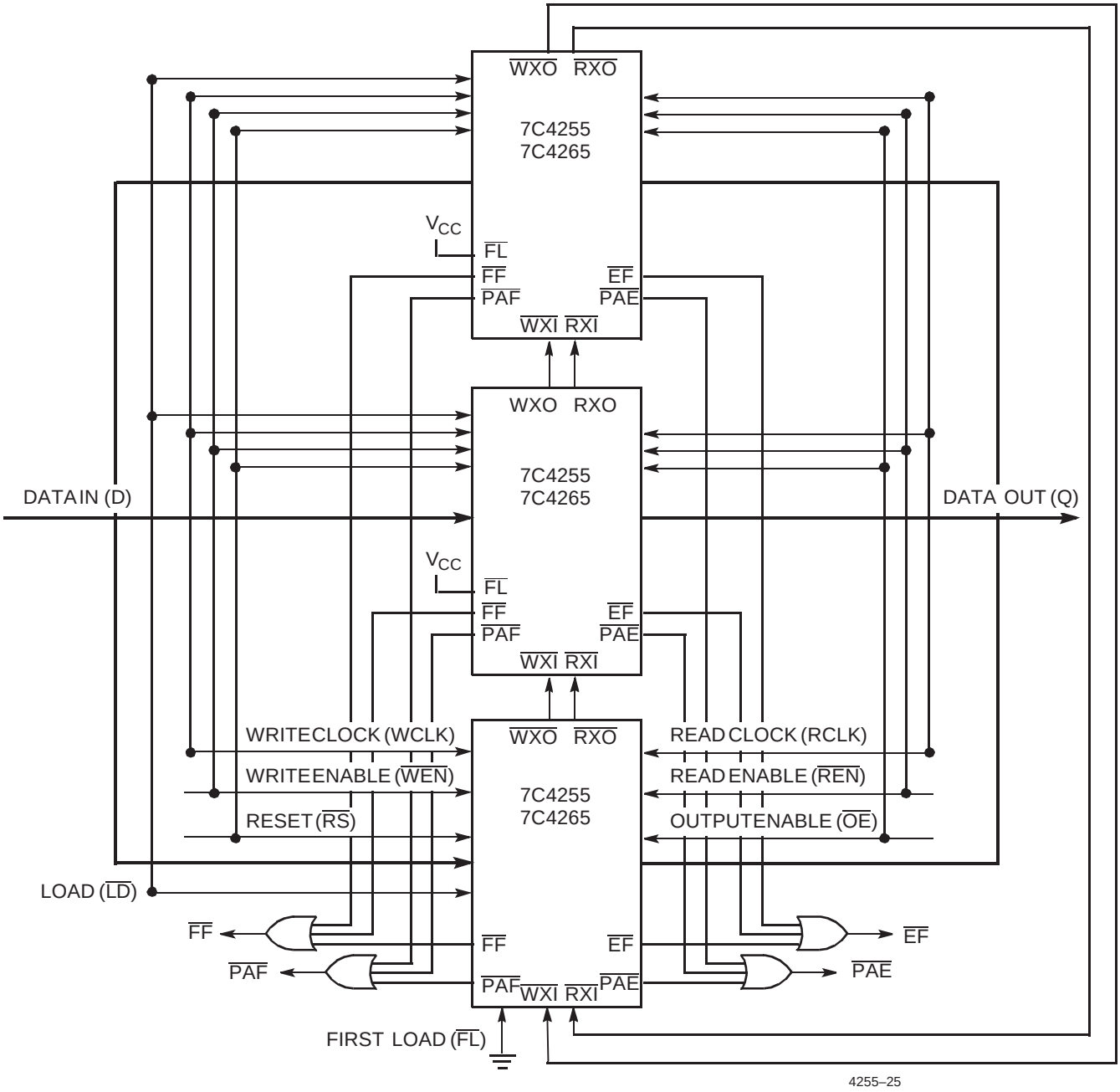
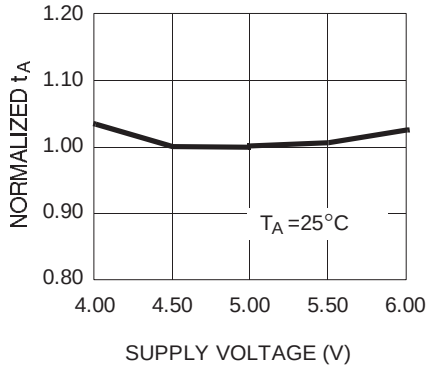


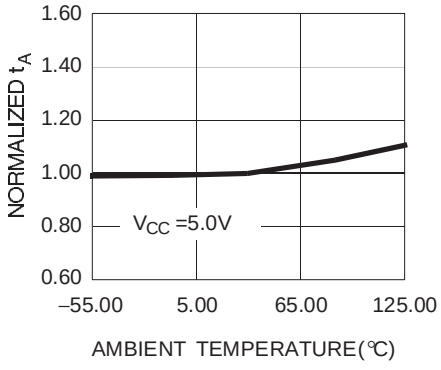
Figure 2. Block Diagram of 8Kx18/16Kx18 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration

Typical AC and DC Characteristics

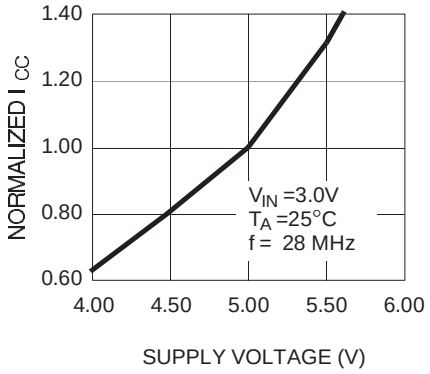
NORMALIZED t_A vs. SUPPLY VOLTAGE



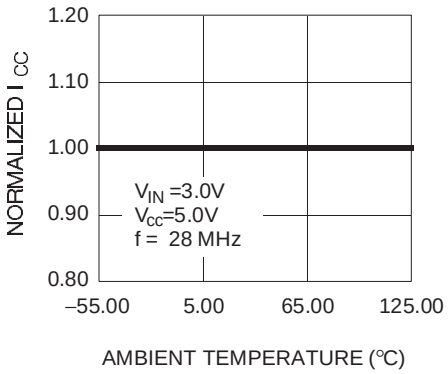
NORMALIZED t_A vs. AMBIENT TEMPERATURE



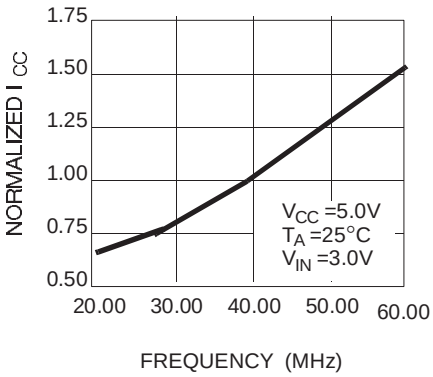
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. FREQUENCY



Ordering Information

8Kx18 Deep Sync FIFO

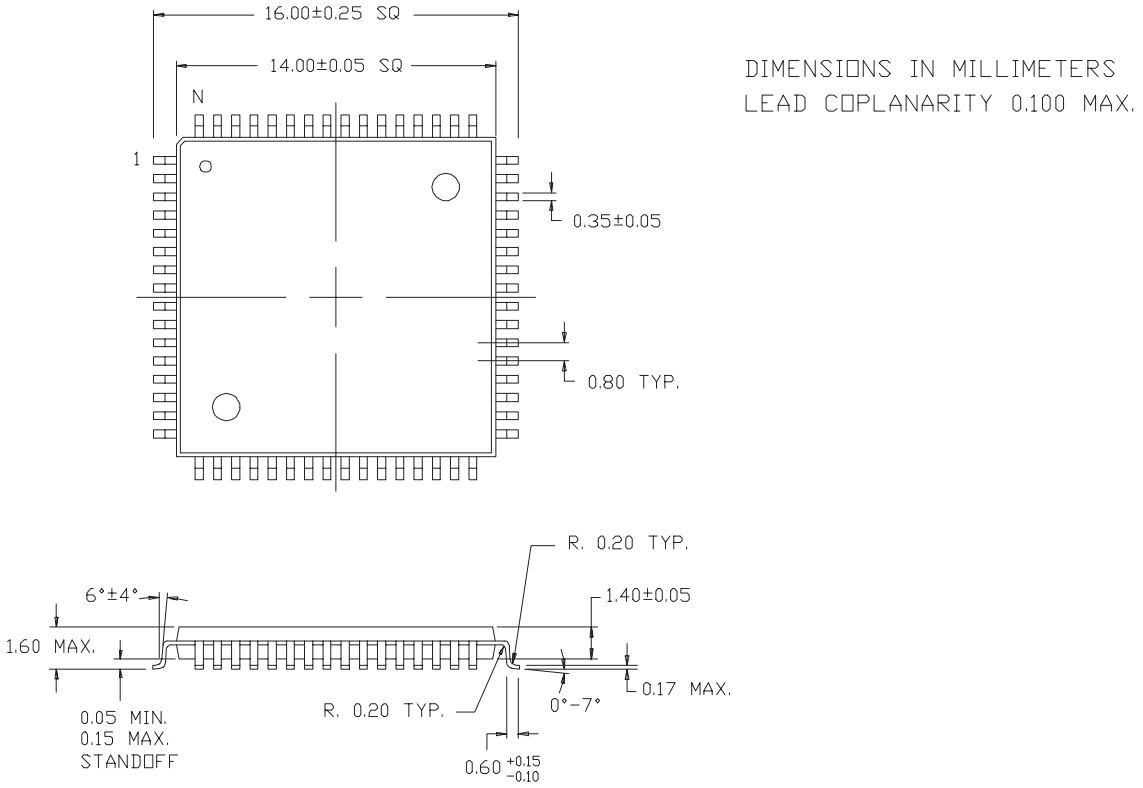
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4255–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4255–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4255–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4255–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4255–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4255–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4255–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

16Kx18 Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4265–10AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–10JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–10AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–10JI	J81	68-Lead Plastic Leaded Chip Carrier	
15	CY7C4265–15AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–15JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–15AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–15JI	J81	68-Lead Plastic Leaded Chip Carrier	
25	CY7C4265–25AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–25JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–25AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–25JI	J81	68-Lead Plastic Leaded Chip Carrier	
35	CY7C4265–35AC	A65	64-Lead Thin Quad Flatpack	Commercial
	CY7C4265–35JC	J81	68-Lead Plastic Leaded Chip Carrier	
	CY7C4265–35AI	A65	64-Lead Thin Quad Flatpack	Industrial
	CY7C4265–35JI	J81	68-Lead Plastic Leaded Chip Carrier	

Package Diagrams

64-Lead Thin Plastic Quad Flat Pack A65



68-Lead Plastic Leaded Chip Carrier J81