



PRELIMINARY

CY62256V

# 32K x 8 Static RAM

## Features

- **Low voltage range:**
  - 2.7V – 3.6V (62256V)
  - 2.3V – 2.7V (62256V25)
  - 1.6V – 2.0V (62256V18)
- **Low active power and standby power**
- **Easy memory expansion with CE and OE features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

## Functional Description

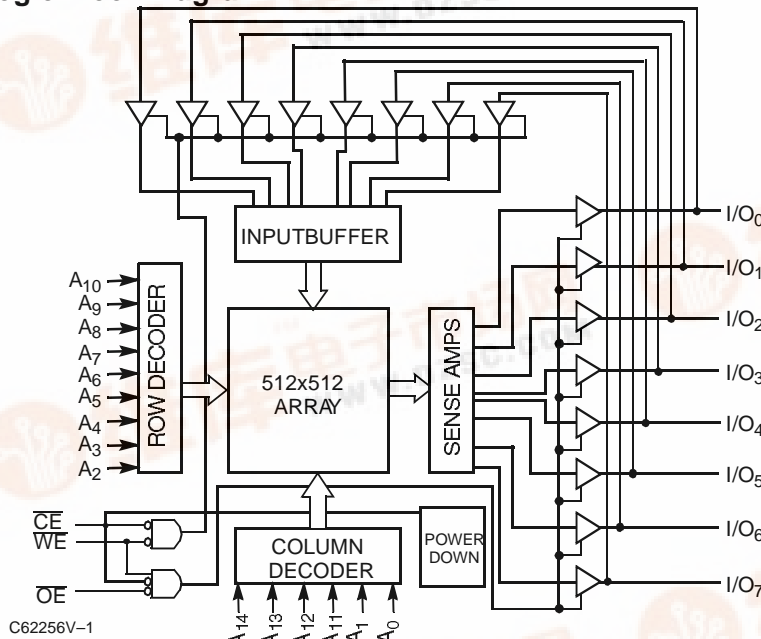
The CY62256V family is composed of three high-performance CMOS static RAM's organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE) and active LOW output enable (OE) and three-state driv-

ers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected. The CY62256V family is available in the standard 450-mil-wide (300-mil body width) SOIC, TSOP, and reverse TSOP packages.

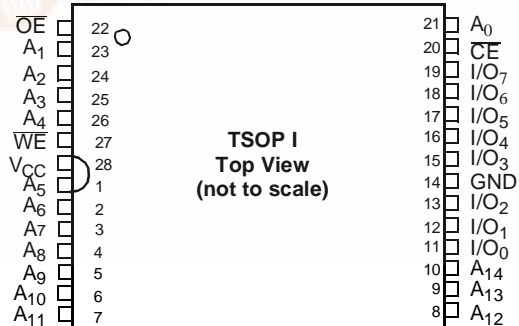
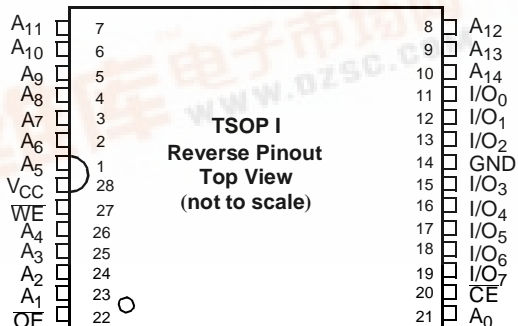
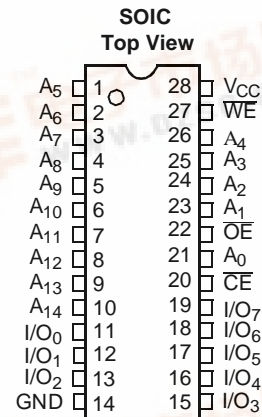
An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the memory location addressed by the address present on the address pins (A<sub>0</sub> through A<sub>14</sub>). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH.

## Logic Block Diagram



## Pin Configurations





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**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to + 150°C

Ambient Temperature with Power Applied ..... 0°C to + 70°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... -0.5V to + 4.6V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	1.6V to 3.6V
Industrial	-40°C to +85°C	1.6V to 3.6V

Note:

1. V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.

**Product Portfolio**

Product	Vcc Range			Speed	Power Dissipation ( LL Devices)			
					Operating(I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
	Min.	Typ.	Max.		Typical	Maximum	Typical	Maximum
CY62256V	2.7V	3.0	3.6V	70 ns	11 mA	30 mA	0.1 uA	5 uA
CY62256V25	2.3V	2.5V	2.7V	100 ns	9 mA	15 mA	0.1 uA	4 uA
CY62256V18	1.6V	1.8V	2.0V	200 ns	5 mA	10 mA	0.1 uA	3 uA

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62256V-70					
			Min.	Typ. <sup>[2]</sup>	Max.	Unit		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.4			V		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 2.1 mA			0.4	V		
V <sub>IH</sub>	Input HIGH Voltage		2.2		V <sub>CC</sub> + 0.3V	V		
V <sub>IL</sub>	Input LOW Voltage		-0.5		0.8	V		
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	uA		
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	uA		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		Com'l Std/L /LL	11 30	mA		
I <sub>SB1</sub>	Automatic CE Power-Down Current— TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		Com'l Std/L /LL	100 300	uA		
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		Com'l Std/ L	0.1 50	uA		
				LL			5	uA
				Ind'l LL			10	uA

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62256V25-100			
			Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -0.1 mA	2			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 0.1 mA			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.7		V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage		-0.3		0.7	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	uA



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**CY62256V**

**Electrical Characteristics** Over the Operating Range (continued)

Parameter	Description	Test Conditions			CY62256V25-100			Unit
					Min.	Typ. <sup>[2]</sup>	Max.	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled			-1		+1	uA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l	Std/L /LL		14	23	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l	Std/L /LL		75	225	uA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	Std/L	0.1	40	4	uA
				LL			4	uA
			Ind'l	LL			8	uA

**Electrical Characteristics** Over the Operating Range

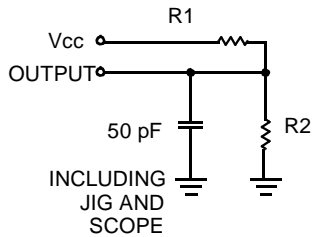
Parameter	Description	Test Conditions			CY62256V18-200			Unit
					Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -0.1 mA			0.8*V <sub>CC</sub>			V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 0.1 mA					0.2	V
V <sub>IH</sub>	Input HIGH Voltage				0.7*V <sub>CC</sub>		V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input LOW Voltage				-0.5		0.2*V <sub>CC</sub>	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>			-1		+1	uA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled			-1		+1	uA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l	Std/L /LL		10	17	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l	Std/L /LL		56	165	uA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	Std/L	0.1	30	3	uA
				LL			3	uA
			Ind'l	LL			6	uA

**Capacitance<sup>[3]</sup>**

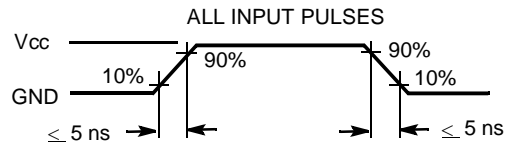
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.0V	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Notes:**

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ., T<sub>A</sub> = 25°C, and t<sub>AA</sub> = 70ns.
- Tested initially and after any design or process changes that may affect these parameters.

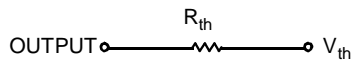
**AC Test Loads and Waveforms**


C62256V-5



C62256V-6

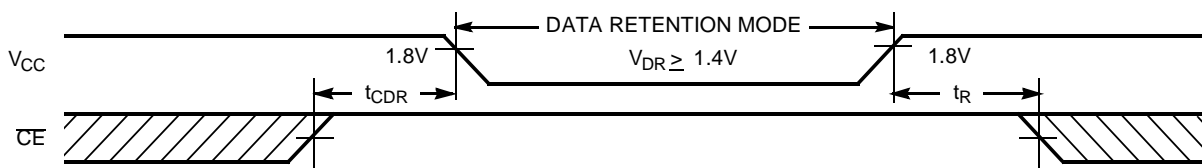
Equivalent to: THÉVENIN EQUIVALENT



AC Test Load			
Vcc	3.3 V	2.5V	1.8V
R1	1103	16.6K	13.6K
R2	1554	15.4K	11.4K
RTH	645	8K	6.2K
VTH	1.75V	1.2V	0.82V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions <sup>[4]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.4			V
I <sub>CCDR</sub>	Data Retention Current	Com1 Std/L LL	V <sub>CC</sub> = 1.6 C <sub>E</sub> ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V	0.1	30	uA
					3	uA
		Ind. LL			6	uA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[3]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform**


C62256V-7



Switching Characteristics Over the Operating Range<sup>[5]</sup>

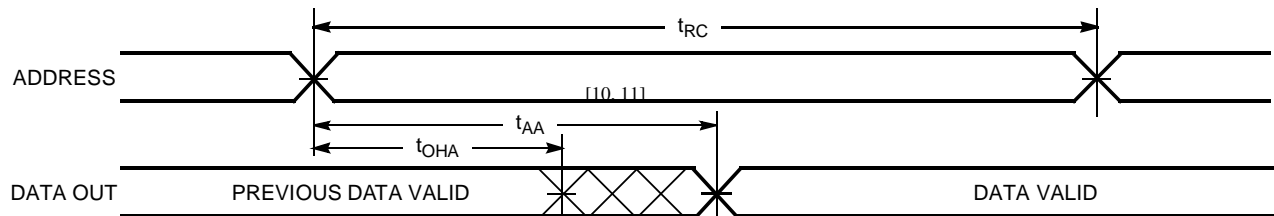
Parameter	Description	CY62256V-70		CY62256V25-100		CY62256V18-200		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	70		100		200		ns
t <sub>AA</sub>	Address to Data Valid		70		100		200	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		70		100		200	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		35		75		125	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	5		5		10		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		25		50		75	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	10		10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		25		50		75	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		70		100		200	ns
<b>WRITE CYCLE<sup>[8,9]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	70		100		200		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	60		90		180		ns
t <sub>AW</sub>	Address Set-Up to Write End	60		90		180		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	50		80		160		ns
t <sub>SD</sub>	Data Set-Up to Write End	30		60		100		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		25		50		100	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	10		10		10		ns

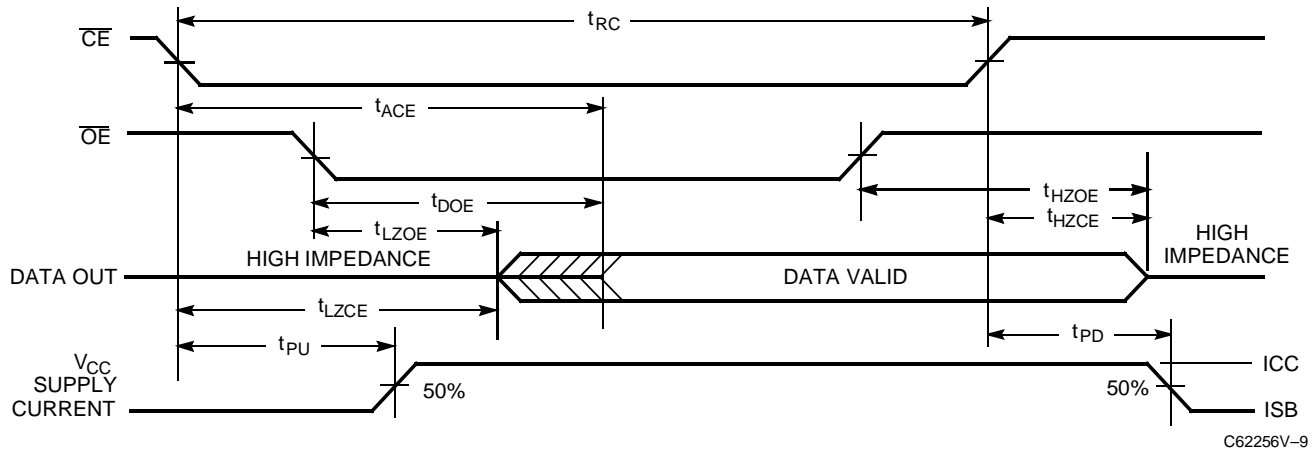
Notes:

- No input may exceed V<sub>CC</sub>+0.3V.
- Test conditions assume signal transition time of 5 ns or less timing reference levels of V<sub>CC</sub>/2, input pulse levels of 0 to V<sub>CC</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 100-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.

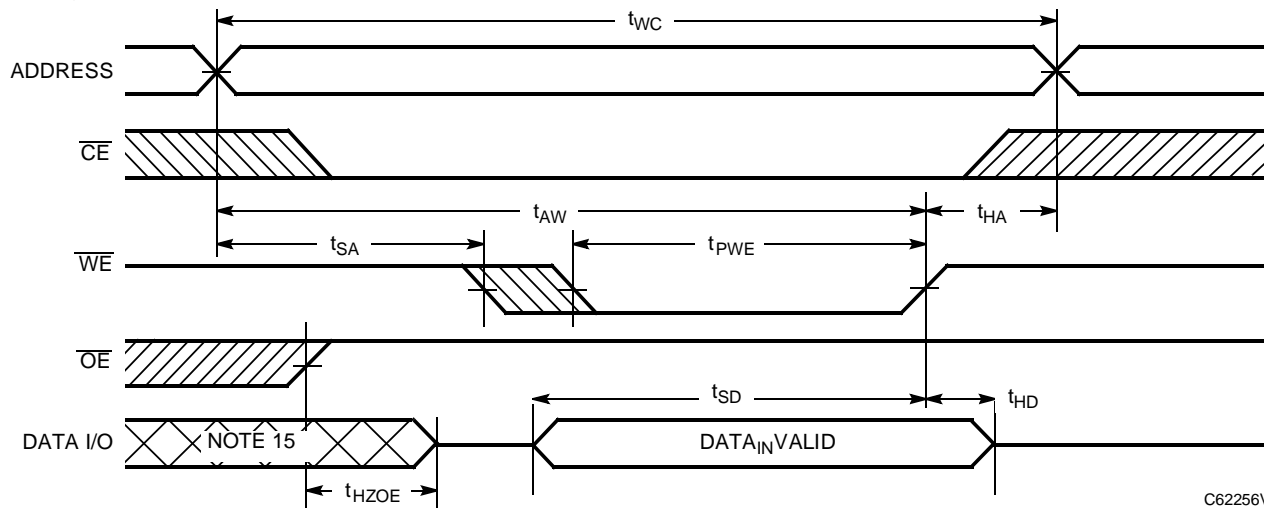
Switching Waveforms

Read Cycle No. 1<sup>[10, 11]</sup>



**Switching Waveforms (continued)**
**Read Cycle No. 2** <sup>[11, 12]</sup>


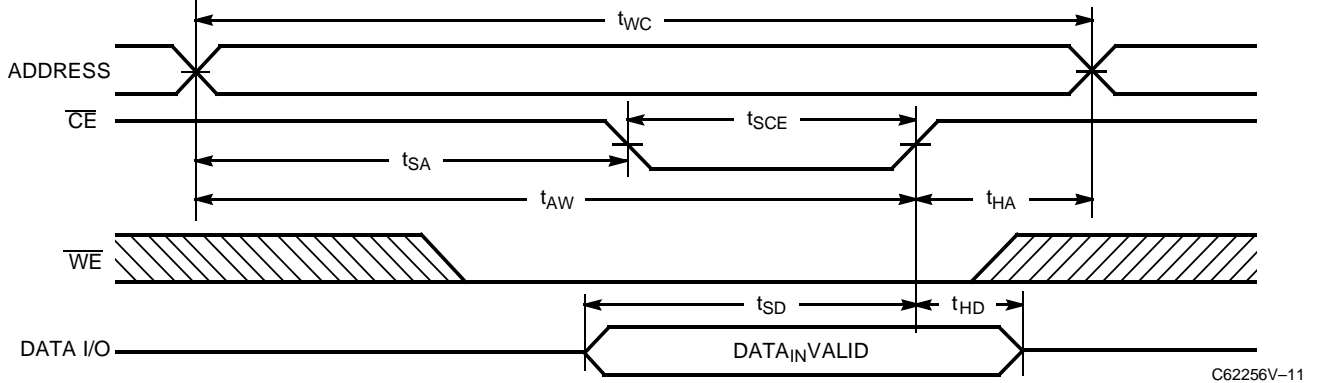
C62256V-9

**Write Cycle No. 1 (WE Controlled)** <sup>[8, 13, 14]</sup>


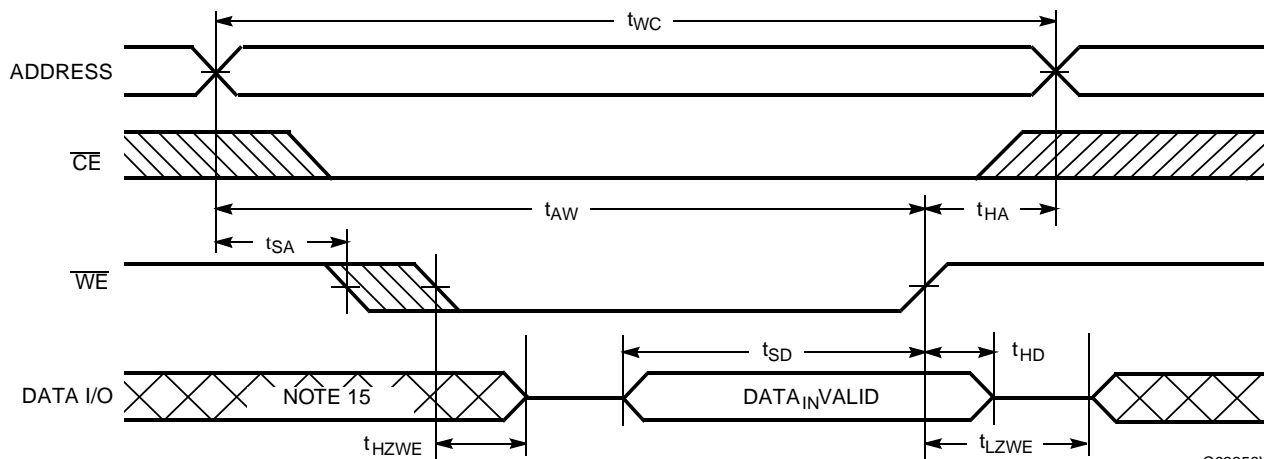
C62256V-10

**Notes:**

8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)<sup>[8, 13, 14]</sup>**


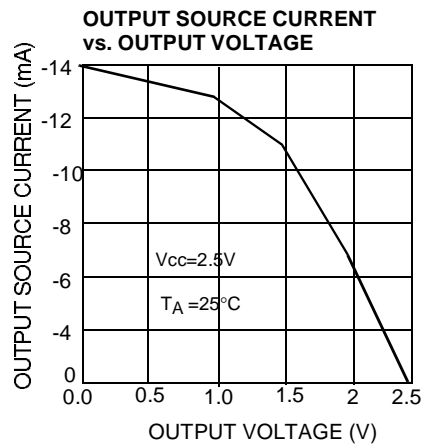
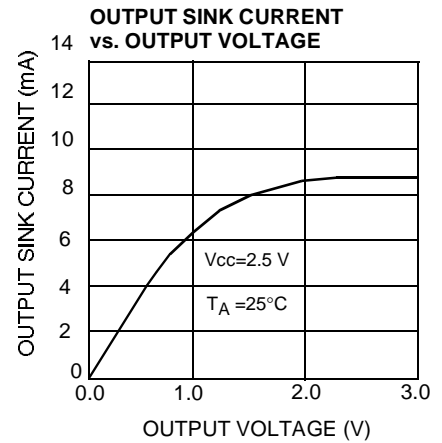
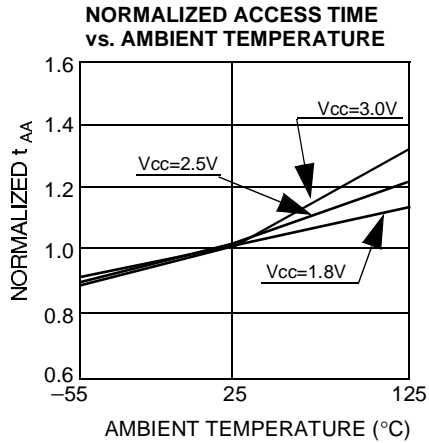
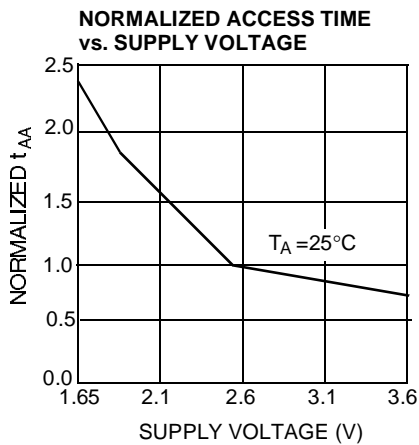
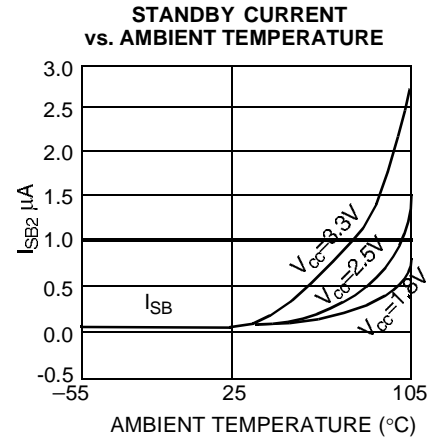
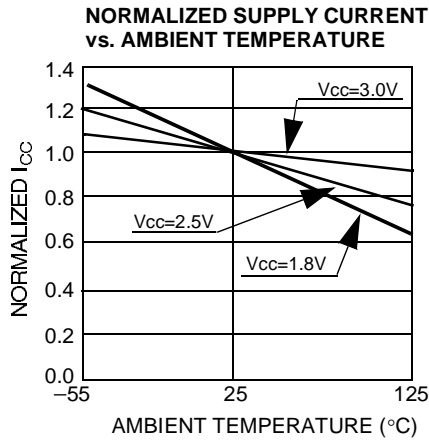
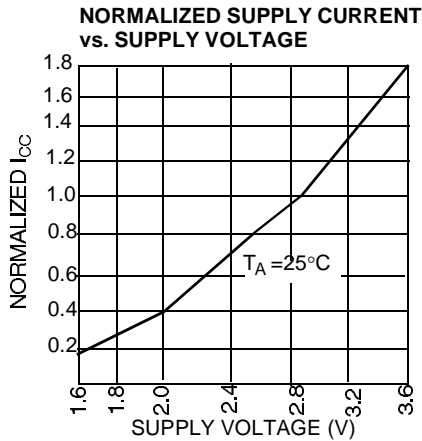
C62256V-11

**Write Cycle No. 3 (WE Controlled,  $\overline{\text{OE}}$  LOW)<sup>[9, 14]</sup>**


C62256V-12

**Notes:**

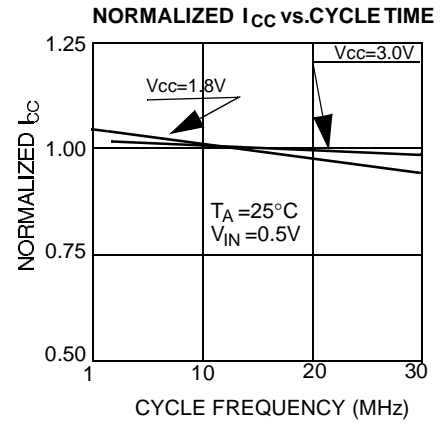
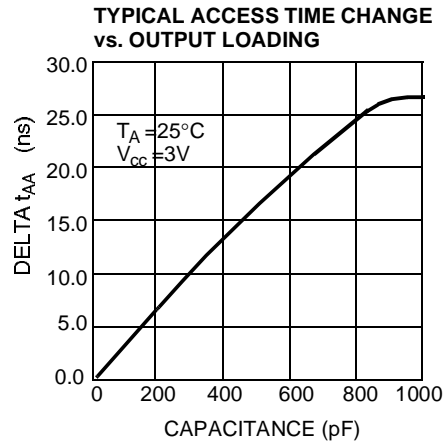
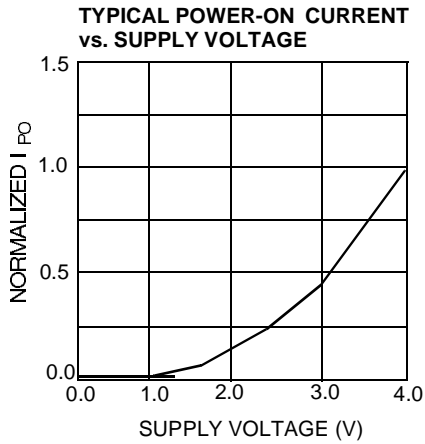
13. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
14. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Typical DC and AC Characteristics**






Typical DC and AC Characteristics (continued)





**PRELIMINARY**

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**Truth Table**

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
L	H	L	Data Out	Read	Active (I <sub>CC</sub> )
L	L	X	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Deselect, Output Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range	
70	CY62256V -70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	<b>Commercial</b>	
	CY62256V L-70SNC				
	CY62256V LL-70SNC				
	CY62256V -70ZRC	ZR28	28-Lead Reverse Thin Small Outline Package		
	CY62256V L-70ZRC				
	CY62256V LL-70ZRC				
	CY62256V -70ZC	Z28	28-Lead Thin Small Outline Package		
	CY62256V L-70ZC				
	CY62256V LL-70ZC				
	CY62256V -70ZI	Z28	28-Lead Thin Small Outline Package		<b>Industrial</b>
	CY62256V L-70ZI				
	CY62256V LL-70ZI				
	CY62256V -70SNI	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC		
	CY62256VL -70SNI				
	CY62256VLL -70SNI				
	CY62256V -70ZRI	ZR28	28-Lead Reverse Thin Small Outline Package		
CY62256V L-70ZRI					
CY62256V LL-70ZRI					
100	CY62256V25-100SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	<b>Commercial</b>	
	CY62256V25L-100SNC				
	CY62256V25LL-100SNC				
	CY62256V25-100ZRC	ZR28	28-Lead Reverse Thin Small Outline Package		
	CY62256V25L-100ZRC				
	CY62256V25LL-100ZRC				
CY62256V25-100ZC	Z28	28-Lead Thin Small Outline Package			
100	CY62256V25L-100ZC	Z28	28-Lead Thin Small Outline Package	<b>Commercial</b>	
	CY62256V25LL-100ZC				
200	CY62256V18-200SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	<b>Commercial</b>	
	CY62256V18L-200SNC				
	CY62256V18LL-200SNC				
	CY62256V18-200ZRC	ZR28	28-Lead Reverse Thin Small Outline Package		
	CY62256V18L-200ZRC				
	CY62256V18LL-200ZRC				
	CY62256V18-200ZC	Z28	28-Lead Thin Small Outline Package		
CY62256V18LL-200ZC					
200	CY62256V18L-200ZC	Z28	28-Lead Thin Small Outline Package	<b>Commercial</b>	

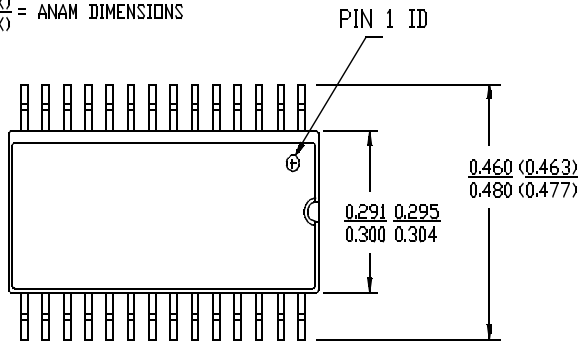
Shaded area contains advanced information.  
Document #: 38-00519-A

**Package Diagrams**

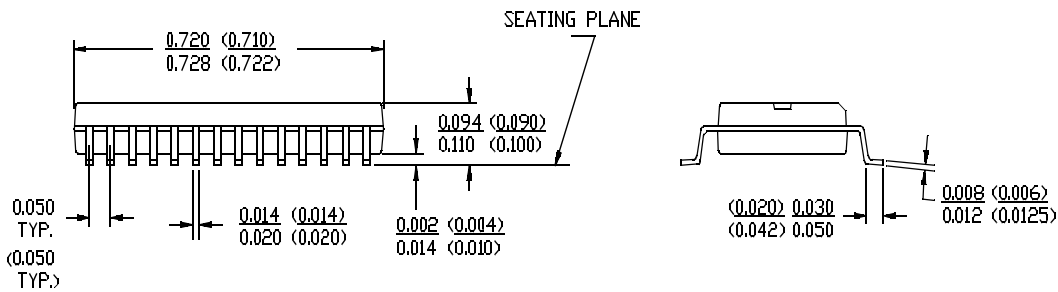
**28-Lead 450-Mil (300-Mil Body Width) SOIC S22**

ΔXXX = HYUNDAI DIMENSIONS  
 ,XXX

(XXX) = ANAM DIMENSIONS  
 <XXX>



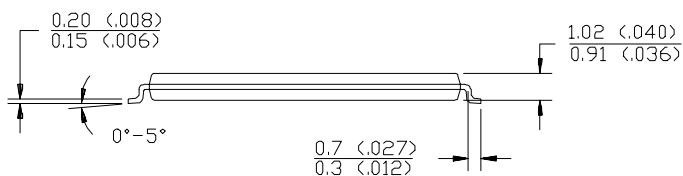
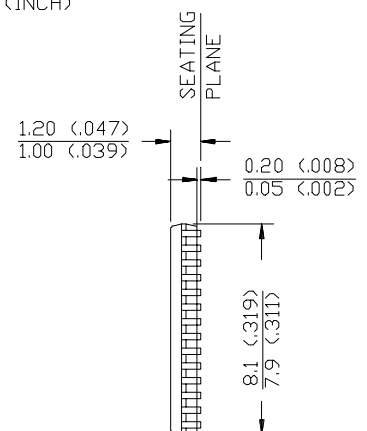
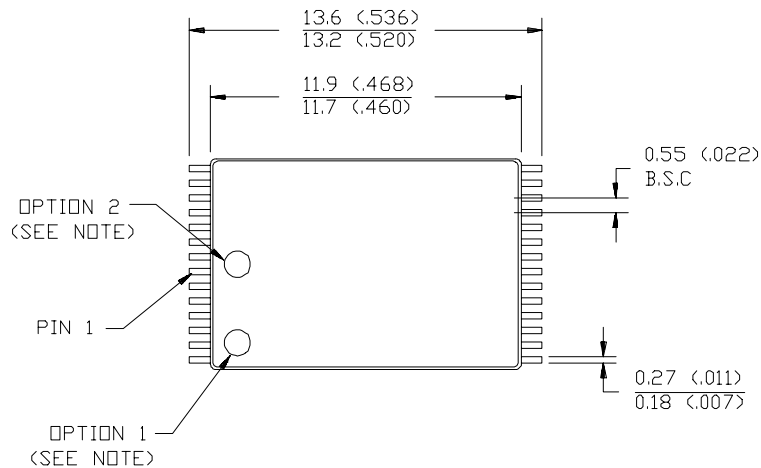
DIMENSIONS IN INCHES MIN.  
MAX.  
 LEAD COPLANARITY 0.004 MAX.



**28-Lead Reverse Thin Small Outline Package ZR28**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)  
 MAX.  
 MIN.



**Package Diagrams (continued)**
**28-Lead Thin Small Outline Package Z28**

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)  
MAX.  
MIN.

