TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS225A

CD54/74AC04, CD54/74ACT04, CD54/74AC05, CD54/74ACT05

September 1998 - Revised May 2000

Hex Inverters

Features

- ’AC04, ’ACT04. . . . . Active Outputs
- ’AC05, ’ACT05. . . . . Open-Drain Outputs
- Buffered Inputs
- Typical Propagation Delay
  - 3.5ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Exceeds 2kV ESD Protection Per MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- ±24mA Output Drive Current
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω Transmission Lines

Description

The ’AC04, ’ACT04, ’AC05 and ’ACT05 are hex inverters that utilize Advanced CMOS Logic technology.

Ordering Information

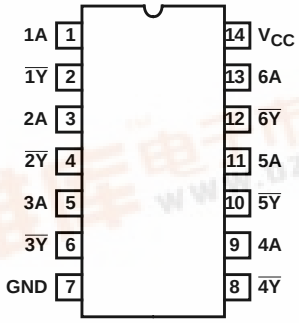
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54AC04F3A	-55 to 125	14 Ld CERDIP
CD74AC04E	-55 to 125	14 Ld PDIP
CD74AC04M	-55 to 125	14 Ld SOIC
CD54ACT04F3A	-55 to 125	14 Ld CERDIP
CD74ACT04E	-55 to 125	14 Ld PDIP
CD74ACT04M	-55 to 125	14 Ld SOIC
CD54AC05F3A	-55 to 125	14 Ld CERDIP
CD74AC05E	-55 to 125	14 Ld PDIP
CD74AC05M	-55 to 125	14 Ld SOIC
CD54ACT05F3A	-55 to 125	14 Ld CERDIP
CD74ACT05E	-55 to 125	14 Ld PDIP
CD74ACT05M	-55 to 125	14 Ld SOIC

NOTES:

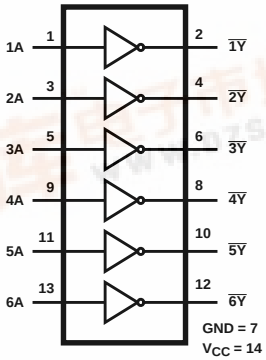
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales ofice or customer service for ordering information.

Pinout

CD54AC04, CD54ACT04, CD54AC05, CD54ACT05
(CERDIP)
CD74AC04, CD74ACT04, CD74AC05, CD74ACT05
(PDIP, SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

AC/ACT04		AC/ACT05	
INPUT	OUTPUT	INPUT	OUTPUT
L	H	L	Z
H	L	H	L

Z = High Impedance

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±50mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±50mA
DC V_{CC} or Ground Current, $I_{CC\ or}$ I_{GND} (Note 3) . . . . . ±100mA

Operating Conditions

Temperature Range, T_A . . . . . -55^{o}C to 125^{o}C
Supply Voltage Range, V_{CC} (Note 4)
AC Types. . . . . 1.5V to 5.5V
ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V . . . . . 50ns (Max)
AC Types, 3.6V to 5.5V. . . . . 20ns (Max)
ACT Types, 4.5V to 5.5V. . . . . 10ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (^{o}C/W)
PDIP Package	90
SOIC Package	175

Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add ±25mA for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25^{o}C		-40^{o}C TO 85^{o}C		-55^{o}C TO 125^{o}C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage (04)	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current, SSI	I_{CC}	V_{CC} or GND	0	5.5	-	4	-	40	-	80	µA
ACT TYPES											
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage (04)	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75	5.5	-	-	3.85	-	-	-	V
			-50	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current, SSI	I_{CC}	V_{CC} or GND	0	5.5	-	4	-	40	-	80	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

INPUT	UNIT LOAD
nA	0.18

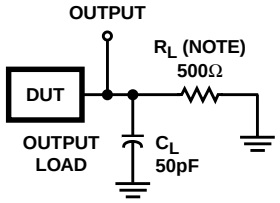
NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, Input to Output (AC/ACT04)	t_{PLH}, t_{PHL}	1.5	-	-	74	-	-	81	ns
		3.3 (Note 9)	2.3	-	8.3	2.3	-	9.1	ns
		5 (Note 10)	1.7	-	5.9	1.6	-	6.5	ns
Propagation Delay, High Z to Output Low (AC/ACT05)	t_{PZL}	1.5	-	-	74	-	-	81	ns
		3.3	2.3	-	8.3	2.3	-	9.1	ns
		5	1.7	-	5.9	1.6	-	6.5	ns
Propagation Delay, Output Low to High Z (AC/ACT05)	t_{PLZ}	1.5	-	-	94	-	-	103	ns
		3.3	3	-	10.4	2.9	-	11.5	ns
		5	2.2	-	7.5	2.1	-	8.2	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	105	-	-	105	-	pF
ACT TYPES									
Propagation Delay, Input to Output (AC/ACT04)	t_{PLH}, t_{PHL}	5 (Note 10)	2.4	-	8.5	2.3	-	9.3	ns
Propagation Delay, Output Low to High Z	t_{PLZ}	5	2.8	-	9.8	2.7	-	10.8	ns
Propagation Delay, High Z to Output Low (AC/ACT05)	t_{PZL}	5	2.4	-	8.5	2.3	-	9.3	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	105	-	-	105	-	pF

NOTES:

8. Limits tested at 100%.
9. 3.3V Min at 3.6V, Max at 3V.
10. 5V Min at 5.5V, Max at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per gate.
    AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
    ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.



NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

FIGURE 1. PROPAGATION DELAY TIMES

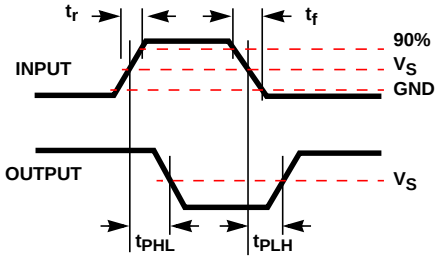


FIGURE 2. WAVEFORMS

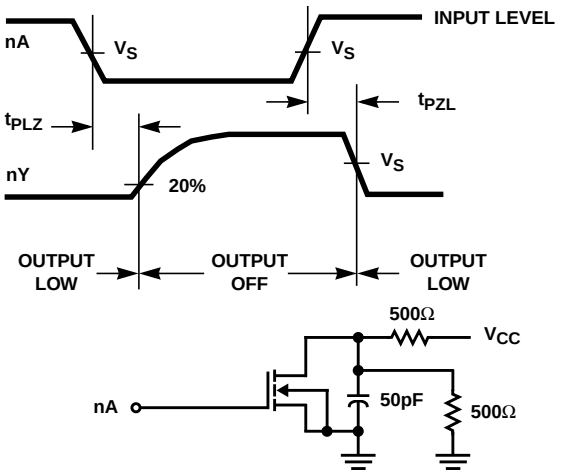


FIGURE 3. PROPAGATION DELAY TIMES AND TEST CIRCUIT

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