8-CHANNEL, 12/10/8-BIT, 2.7-V TO 5.5-V LOW POWER DIGITAL-TO-ANALOG CONVERTERS WITH POWER DOWN

SLAS268A – MAY 2000 – REVISED JUNE 2000

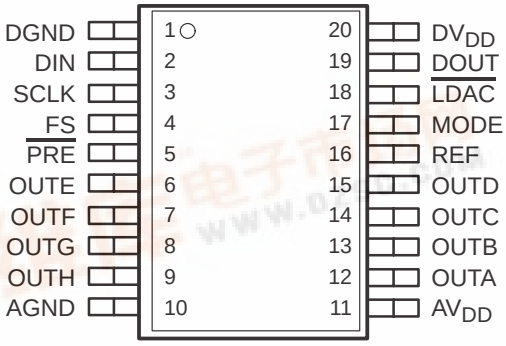
features

- Eight Voltage Output DACs in One Package
  - TLV5610† . . . 12-Bit
  - TLV5608† . . . 10-Bit
  - TLV5629 . . . 8-Bit
- Programmable Settling Time vs Power Consumption
  - 1 μs in Fast Mode at 5 V
  - 3 μs in Slow Mode at 5V
- Compatible With TMS320 and SPI Serial Ports
- Monotonic Over Temperature
- Low Power Consumption:
  - 15 mW in Slow Mode at 3 V
  - 45 mW in Fast Mode at 3 V
- Power Down Mode
- Buffered, High Impedance Reference Inputs
- Data Output for Daisy Chaining

applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

DW OR PW PACKAGE
(TOP VIEW)



description

The TLV5610†, TLV5608†, and TLV5629 are pin compatible eight channel 12/10/8-bit voltage output DACs each with a flexible serial interface. The serial interface allows glueless interface to TMS320 and SPI, QSPI, and Microwire serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

Additional features are a power-down mode, an $\overline{\text{LDAC}}$ input for simultaneous update of all eight DAC outputs, and a data output which can be used to cascade multiple devices.

The resistor string output voltage is buffered by a rail-to-rail output amplifier with a programmable settling time to allow the designer to optimize speed vs power dissipation. The buffered, high-impedance reference input can be connected to the supply voltage.

Implemented with a CMOS process, the DACs are designed for single supply operation from 2.7 V to 5.5 V. The devices are available in 20 pin SOIC and TSSOP packages.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SOIC (DW)	TSSOP (PW)	RESOLUTION
–40°C to 85°C	TLV5610IDW†	TLV5610IPW†	12
	TLV5608IDW†	TLV5608IPW†	10
	TLV5629IDW	TLV5629IPW	8

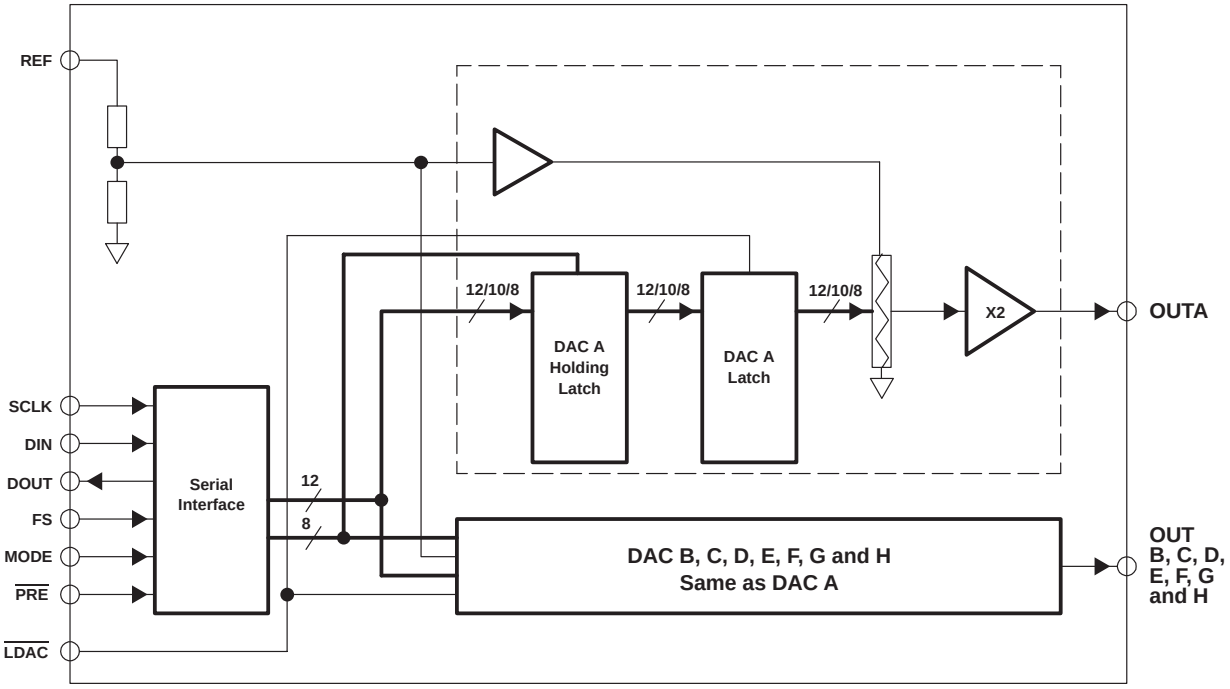
† Product Preview

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

TEXAS INSTRUMENTS

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	10	P	Analog ground
AV_{DD}	11	P	Analog power supply
DGND	1	P	Digital ground
DIN	2	I	Digital serial data input
DOUT	19	O	Digital serial data output
DV_{DD}	20	P	Digital power supply
FS	4	I	Frame sync input
$\overline{\text{LDAC}}$	18	I	Load DAC. The DAC outputs are only updated, if this signal is low. It is an asynchronous input.
MODE	17	I	DSP/µC mode pin. High = µC mode, NC = DSP mode.
$\overline{\text{PRE}}$	5	I	Preset input
REF	16	I	Voltage reference input
SCLK	3	I	Serial clock input
OUTA–OUTH	12–15, 6 – 9	O	DAC outputs A, B, C, D, E, F, G and H

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, (AV_{DD}, DV_{DD} to GND) . . . . . 7 V
Reference input voltage range . . . . . – 0.3 V to AV_{DD} + 0.3
Digital input voltage range . . . . . – 0.3 V to DV_{DD} + 0.3
Operating free-air temperature range, T_A: TLV5629I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, AV_{DD}, AV_{DD}	5 V operation	4.5	5	5.5	V
	3 V operation	2.7	3	3.3	V
High level digital input, V_{IH}	DV_{DD} = 2.7 V to 5.5 V	2			V
Low level digital input, V_{IL}	DV_{DD} = 2.7 V to 5.5 V			0.8	V
Reference voltage, V_{REF}	AV_{DD} = 5 V	GND	2.048	AV_{DD}	V
	AV_{DD} = 3 V	GND	1.024	AV_{DD}	
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Clock frequency, FCLK				30	MHz
Operating free-air temperature, T_A		–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, Vref = 2.048 V, All inputs = DV_{DD} or GND	Fast		15	20	mA
			Slow		5	7	
	Power-down supply current				10		nA
POR	Power on threshold				2		V
PSRR	Power supply rejection ratio	Full scale, See Note 1			60		dB

NOTE 1: Power supply rejection ratio at full scale is measured by varying AV_{DD} and is given by:
$PSRR = 20 \log [(E_G(AV_{DD}max) – E_G(AV_{DD}min))/V_{DD}max]$

electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

static DAC specifications

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution	TLV5610†			12		Bits
		TLV5608†			10		Bits
		TLV5629			8		Bits
INL	Integral nonlinearity	TLV5610†	Ref = 2 V, 4 V		±1.2	±6	LSB
		TLV5608†	Ref = 2 V, 4 V		±1	±2	LSB
		TLV5629	Ref = 2 V, 4 V		±0.3	±1	LSB
DNL	Differential nonlinearity	TLV5610†	Ref = 2 V, 4 V		±0.3	±1	LSB
		TLV5608†	Ref = 2 V, 4 V		±0.3	±1	LSB
		TLV5629	Ref = 2 V, 4 V		±0.1	±1	LSB
E_{ZS}	Zero scale error (offset error at zero scale)					±27	mV
E_{ZS} TC	Zero scale error temperature coefficient				30		µV/°C
E_G	Gain error					±1	%Full Scale V
E_GTC	Gain error temperature coefficient				10		ppm/°C

† Product Preview

output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ	0		AV_{DD}–0.4	V
	Output load regulation accuracy	R_L = 2 kΩ vs 10 kΩ			±0.3	%Full Scale V

reference input

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			0		AV_{DD}	V
R_I	Input resistance				100		kΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REF = 0.4V_{pp} + 2.048Vdc, Input code = 0x800	Fast		2.2		MHz
			Slow		1.9		MHz
	Reference feedthrough	REF = 2 V_{pp} at 1 kHz + 2.048 Vdc (see Note 2)			–84		dB

NOTE 2: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = DV_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0 V	–1			µA
C_I	Input capacitance			8		pF

digital output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level digital output voltage	R_L = 10 kΩ	2.6			V
V_{OL}	Low-level digital output voltage	R_L = 10 kΩ			0.4	V
	Output voltage rise time	R_L = 10 kΩ, C_L = 20 pF, Includes propogation delay		7	20	ns

electrical characteristics over recommended operating conditions (unless otherwise noted) (continued)

analog output dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_S(FS)	Output settling time, full scale	R_L = 10 kΩ,	C_L = 100 pF, See Note 3	Fast		1	3.5	µs
				Slow		3	7	
t_S(CC)	Output settling time, code to code	R_L = 10 kΩ,	C_L = 100 pF, See Note 4	Fast		0.5	1	µs
				Slow		1	2	
SR	Slew rate	R_L = 10 kΩ,	C_L = 100 pF, See Note 5	Fast	6	10		V/µs
				Slow	3	1.7		
	Glitch energy	Code transition from 0x7FF to 0x800				4		nV–s
SNR	Signal-to-noise ratio	f_S = 400 kSPS, R_L = 10 k, f_B = 20 kHz	f_{out} = 1 kHz, C_L = 100 pF,	TLV5629	48	53		dB
SINAD	Signal-to-noise + distortion				48	53		
THD	Total harmonic distortion					–52	–50	
	Channel crosstalk	10 kHz sine, 4V_{PP}				–90		dB

NOTES: 3. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively. Assured by design; not tested.
4. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count. The max time applies to code changes near zero scale or full scale. Assured by design; not tested.
5. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full scale voltage.

digital input timing requirements

PARAMETER		MIN	TYP	MAX	UNIT
t_{su}(FS–CK)	Setup time, FS low before first negative SCLK edge	8			ns
t_{su}(C16–FS)	Setup time, 16th negative edge after FS low on which bit D0 is sampled before rising edge of FS. µC mode only	10			ns
t_{wH}(LDAC)	$\overline{\text{LDAC}}$ width low	10			ns
t_{wH}	SCLK pulse width high	16			ns
t_{wL}	SCLK pulse width low	16			
t_{su}(D)	Setup time, data ready before SCLK falling edge	8			ns
t_H(D)	Hold time, data held valid after SCLK falling edge	5			ns
t_{wH}(FS)	FS width high	10			ns
t_{wL}(FS)	FS width low	10			ns
t_S	Settling time	See AC specs			

TYPICAL CHARACTERISTICS

TLV5629
OUTPUT LOAD REGULATION

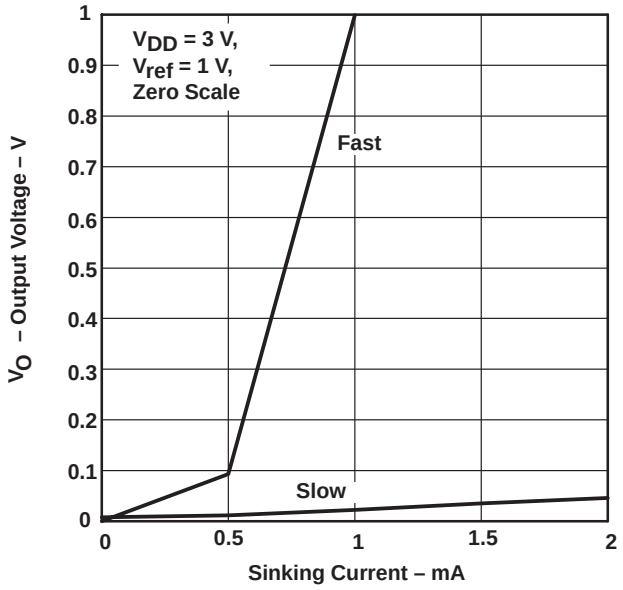


Figure 1

TLV5629
OUTPUT LOAD REGULATION

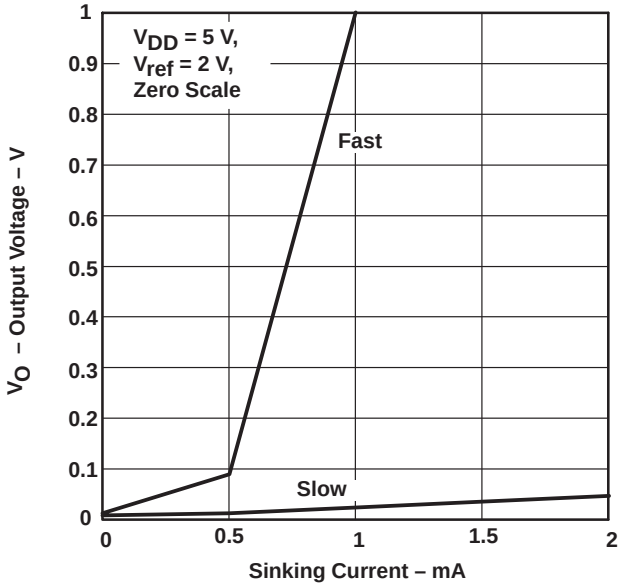


Figure 2

TLV5629
OUTPUT LOAD REGULATION

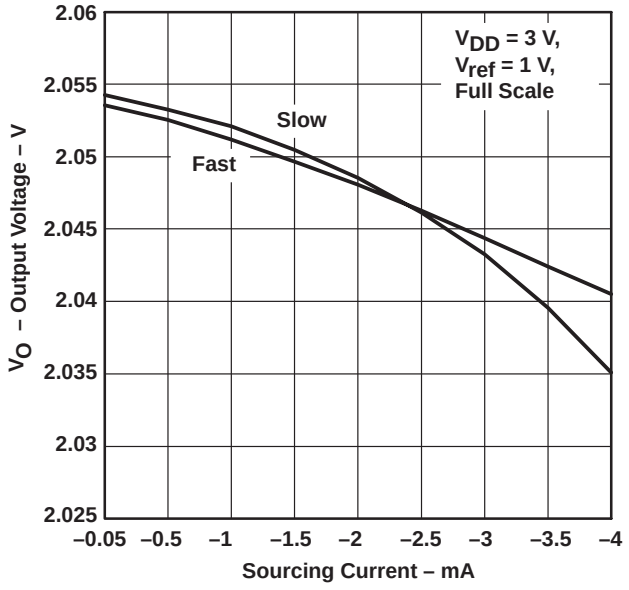


Figure 3

TLV5629
OUTPUT LOAD REGULATION

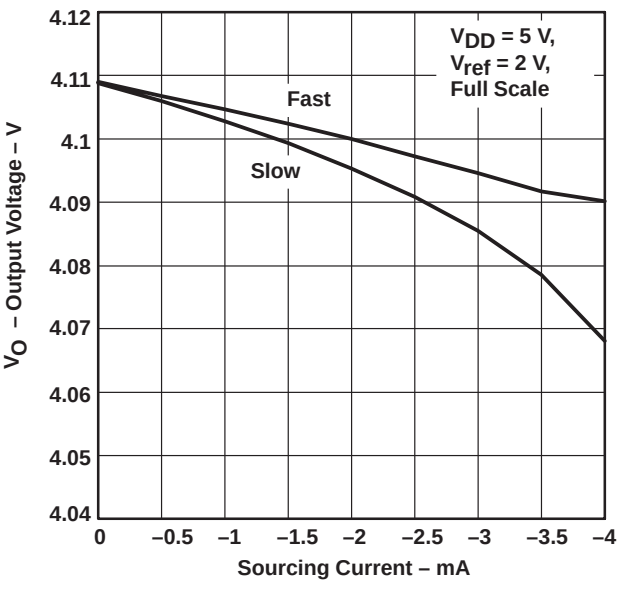


Figure 4

TYPICAL CHARACTERISTICS

TLV5629
TOTAL HARMONIC DISTORTION AND NOISE
vs
INPUT FREQUENCY

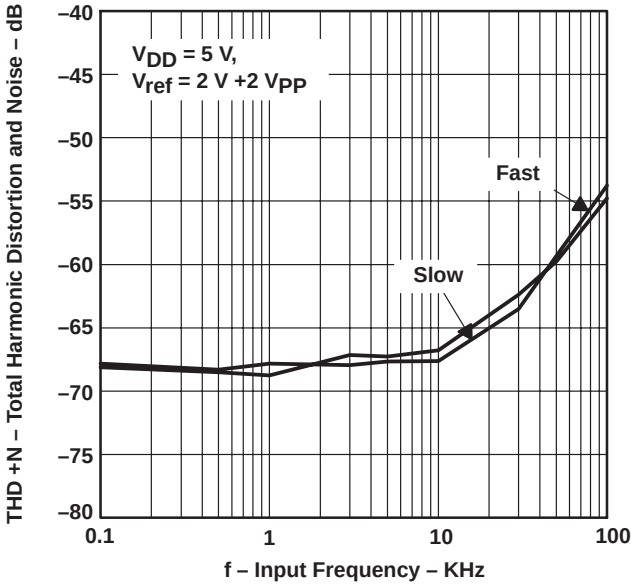


Figure 5

TLV5629
TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

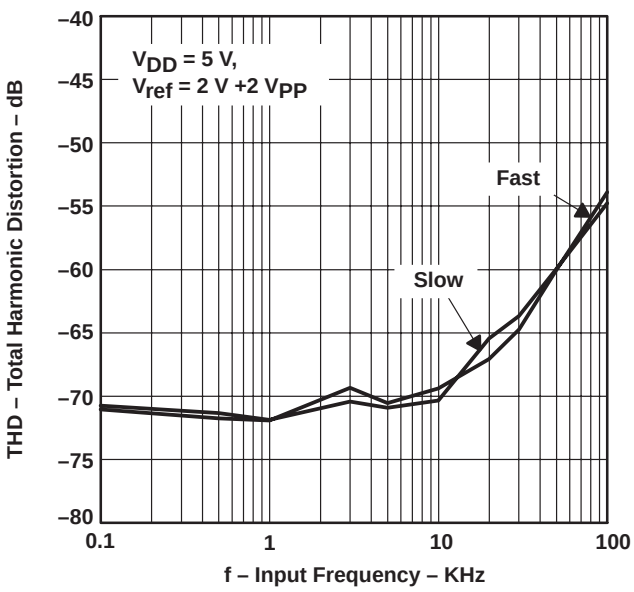


Figure 6

TYPICAL CHARACTERISTICS

TLV5629
DIFFERENTIAL NONLINEARITY
vs
CODE

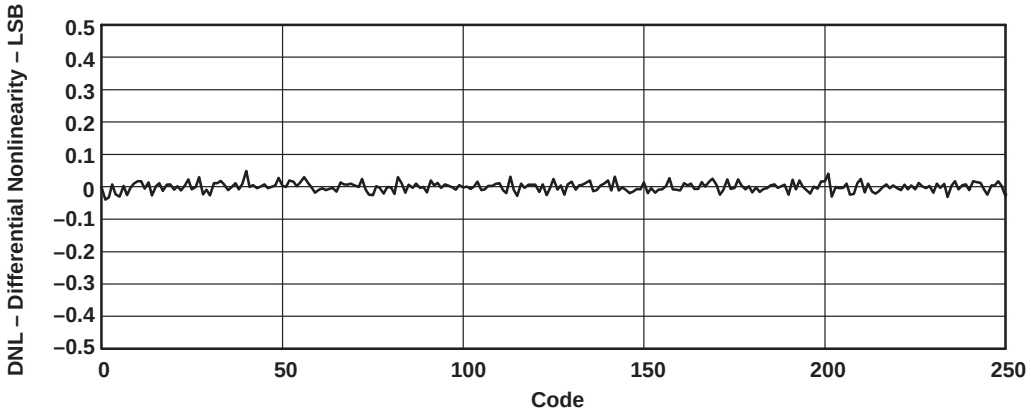


Figure 7

TLV5629
INTEGRAL NONLINEARITY
vs
CODE

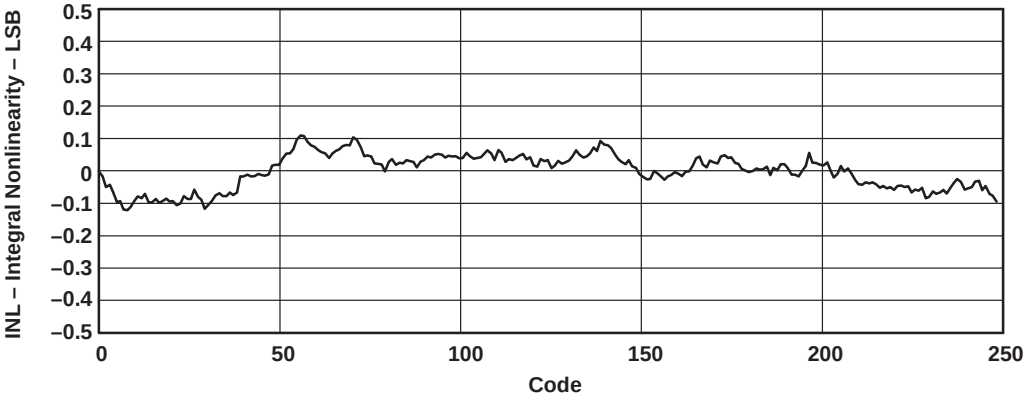
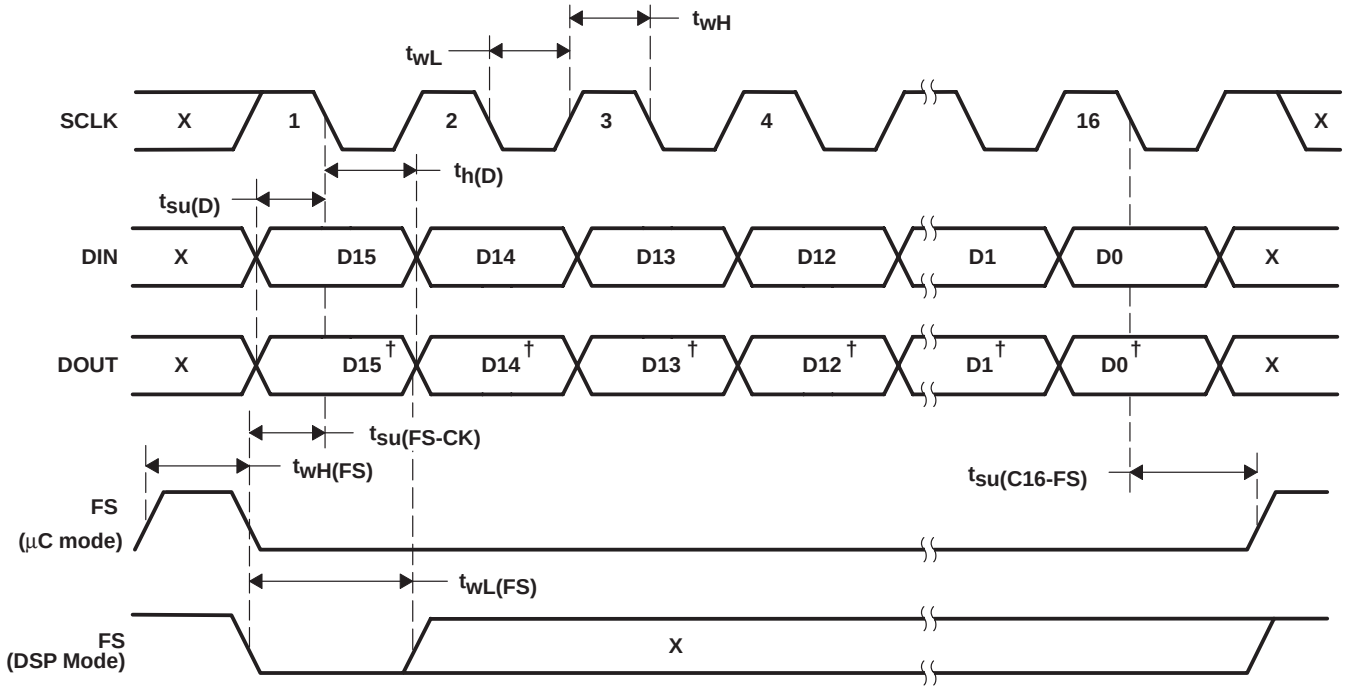


Figure 8

PARAMETER MEASUREMENT INFORMATION



† Previous input data

Figure 9. Serial Interface

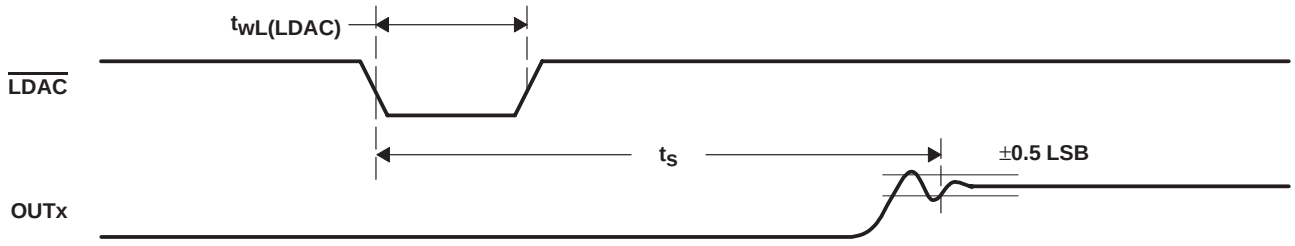


Figure 10. Output

APPLICATION INFORMATION

general function

The TLV5610†, TLV5608†, and TLV5629 are 8-channel, 12-bit, single supply DACs, based on a resistor string architecture. They consist of a serial interface, a speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) for each channel is given by:

$$\text{REF}\ \frac{\text{CODE}}{0\text{x}1000}\ [\text{V}]$$

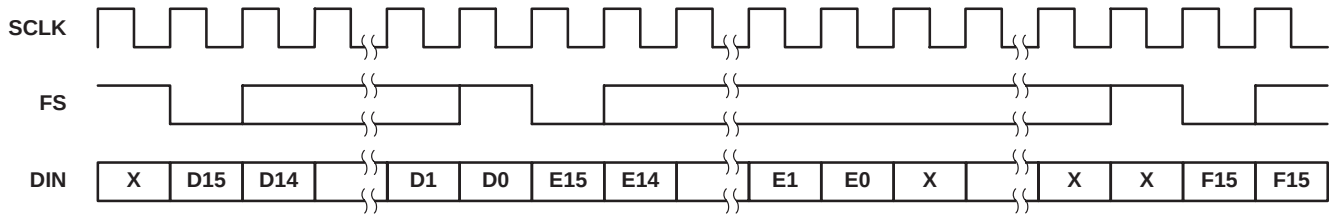
Where REF is the reference voltage and CODE is the digital input value, range 0x000 to 0xFFF. A power on reset initially puts the internal latches to a defined state (all bits zero).

serial interface

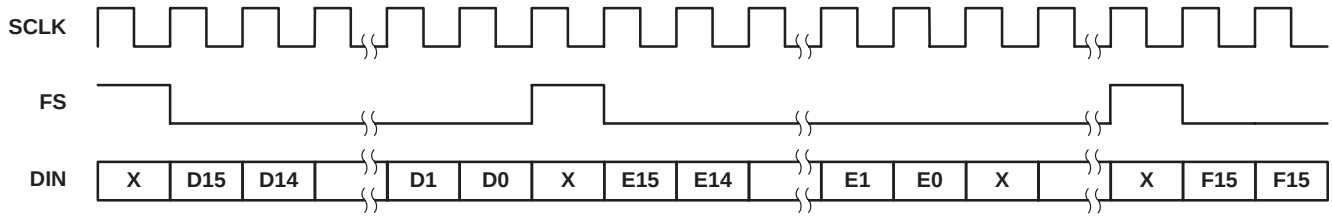
A falling edge of FS starts shifting the data on DIN starting with the MSB to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the content of the shift register is moved to one of the DAC holding registers depending on the address bits within the data word. A logic 0 on the $\overline{\text{LDAC}}$ pin is required to transfer the content of the DAC holding register to the DAC latch and to update the DAC outputs. $\overline{\text{LDAC}}$ is an asynchronous input. It can be held low if a simultaneous update of all eight channels is not needed.

For daisy-chaining, DOUT provides the data sampled on DIN with a delay of 16 clock cycles.

DSP Mode:



µC Mode:



Difference between DSP mode (MODE = N.C. or 0) and µC (MODE = 1) mode:

- In µC mode FS needs to be held low until all 16 data bits have been transferred. If FS is driven high before the 16th falling clock edge the data transfer is cancelled.
- In DSP mode FS only needs to stay low for 20 ns and can go high before the 16th falling clock edge.

APPLICATION INFORMATION

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 30 \text{ MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16 \left(t_{whmin} + t_{wlmin}\right)} = 1.95 \text{ MHz}$$

Note, that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the DAC has to be considered also.

data format

The 16 bit data word consists of two parts:

- Address bits (D15…D12)
- Data bits (D11…D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	Data											

Ax: Address bits. See table.

register map

A3	A2	A1	A0	FUNCTION
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	0	0	0	CTRL0
1	0	0	1	CTRL1
1	0	1	0	Preset
1	0	1	1	Reserved
1	1	0	0	DAC A and $\overline{B}$
1	1	0	1	DAC C and $\overline{D}$
1	1	1	0	DAC E and $\overline{F}$
1	1	1	1	DAC G and $\overline{H}$

APPLICATION INFORMATION

DAC A–H and two-channel registers

Writing to DAC A–H sets the output voltage of channel A–H. It is possible to automatically generate the complement of one channel by writing to one of the four two-channel registers (DAC A and $\overline{B}$ etc.).

The TLV5610† decodes all 12 data bits. The TLV5608† decodes D11 to D2 (D1 and D0 are ignored). The TLV5629 decodes D11 to D4 (D3 to D0 are ignored).

Preset

The outputs of all DAC channels can be driven to a predefined value stored in the Preset register by driving the $\overline{PRE}$ input low. The $\overline{PRE}$ input is asynchronous to the clock.

CTRL0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	PD	DO	X	X	IM

PD :Full device power down 0 = normal 1 = power down
DO :Digital output enable 0 = enable 1 = disable
IM :Input mode 0 = straight binary 1 = twos complement
X :Reserved

If DOUT is enabled, the data input on DIN is output on DOUT with a 16 cycle delay. That makes it possible to daisy-chain multiple DACs on one serial bus.

CTRL1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	P_{GH}	P_{EF}	P_{CD}	P_{AB}	S_{GH}	S_{EF}	S_{CD}	S_{AB}

P_{XY} : Power Down DAC_{XY} 0 = normal 1 = power down
S_{XY} : Speed DAC_{XY} 0 = slow 1 = fast
XY : DAC pair AB, CD, EF or GH

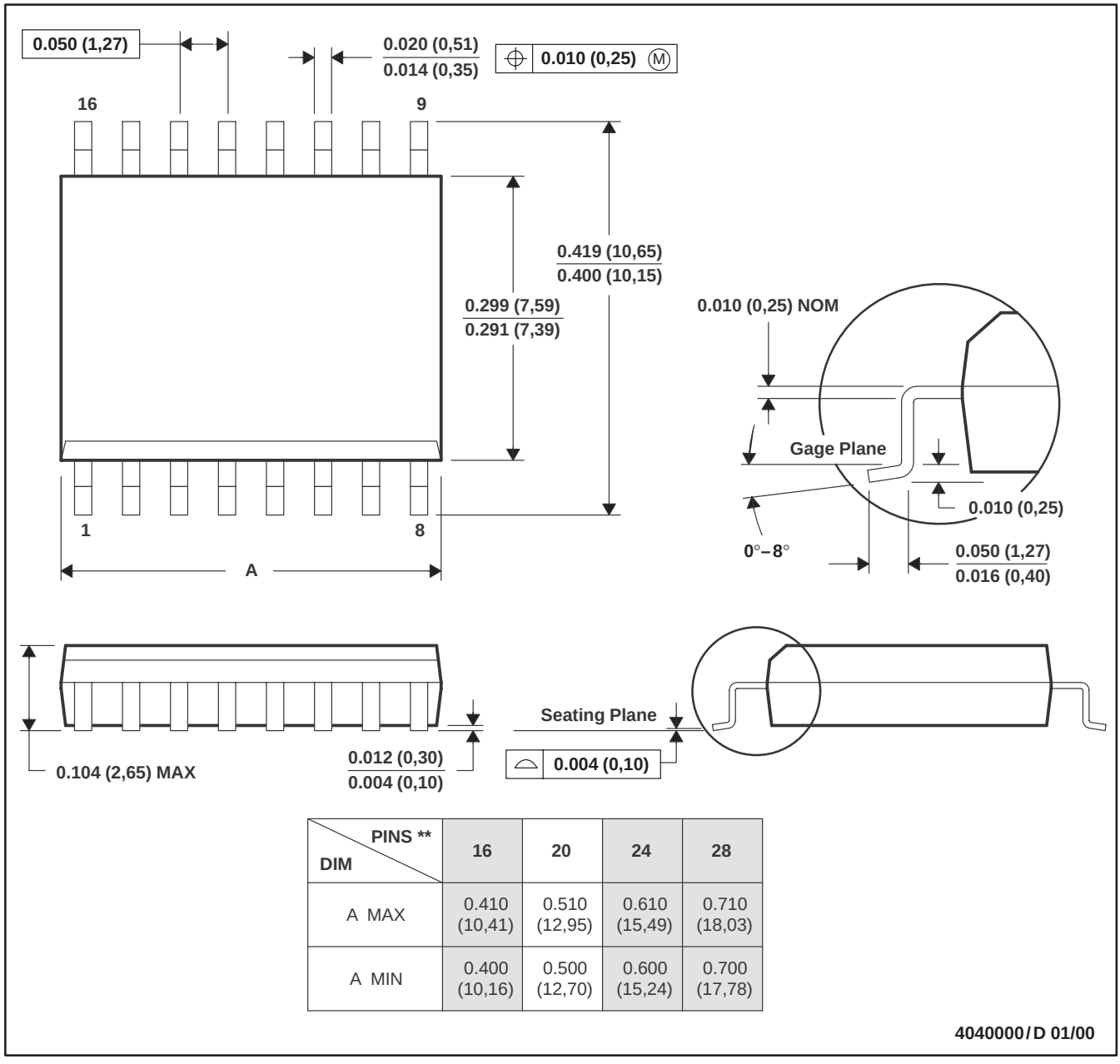
In power-down mode, the amplifiers of the selected DAC pair within the device are disabled and the total power consumption of the device is significantly reduced. Power-down mode of a specific DAC pair can be selected by setting the PXY bit within the data word to 1.

There are two settling time modes: fast and slow. Fast mode of a DAC pair is selected by setting S_{XY} to 1 and slow mode is selected by setting S_{XY} to 0.

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

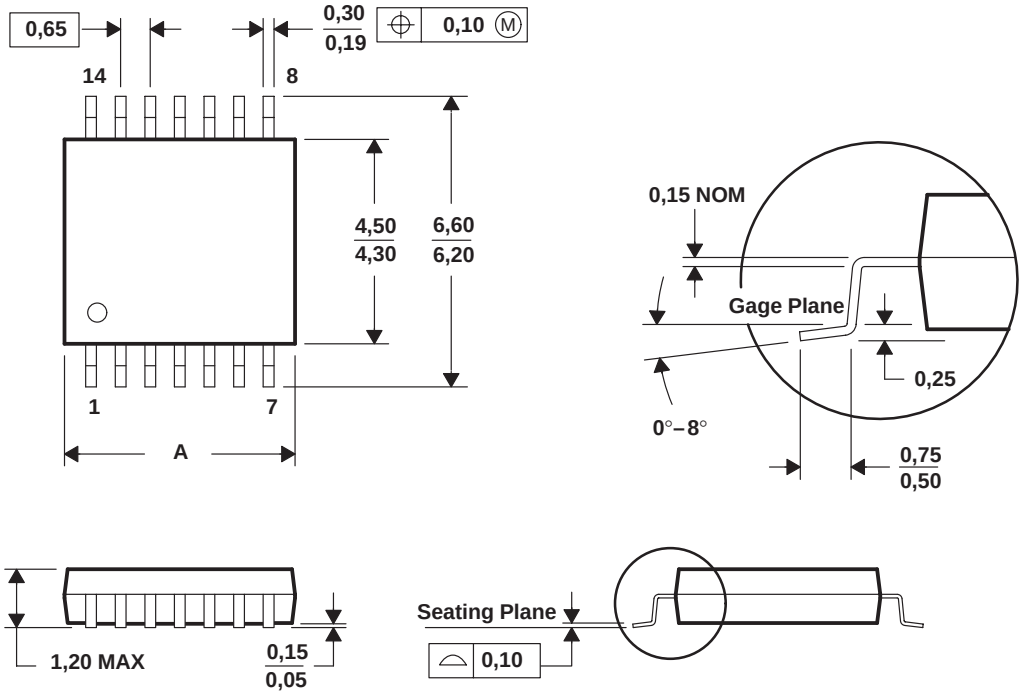
4040000/D 01/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.